CMOS Logic Gate Fabricated on Hybrid Crystal Orientations and Method of Forming Thereof

ABSTRACT OF THE DISCLOSURE

In preferred embodiments of the present invention, a method of forming CMOS devices using SOI and hybrid substrate orientations is described. In accordance with a preferred embodiment, a substrate may have multiple crystal orientations. One logic gate in the substrate may comprise at least one N-FET on one crystal orientation and at least one P-FET on another crystal orientation. Another logic gate in the substrate may comprise at least one N-FET and at least one P-FET on the same orientation. Alternative embodiments further include determining the preferred cleavage planes of the substrates and orienting the substrates relative to each other in view of their respective preferred cleavage planes. In a preferred embodiment, the cleavage planes are not parallel.

Fig. 3