MULTILAYER SUBSTRATE METALLIZATION FOR IC INTERCONNECTION

Technical Field

This invention relates to what is known as "flip chip technology" in the packaging of integrated circuits and relates in particular to a new multilayer substrate metallization for use with eutectic SnPb and Pb-free solders on a microchip.

Background of the Invention

According to Semiconductor Roadmap, the number of input/output (***I/O***) interconnections on silicon chips will increase significantly in the next decade. In order to meet this requirement, flip chip technology is expected to dominate the IC packaging market in the future.

Flip chip technology is an advanced form of surface mount technology which generally involves deposition of a plurality of solders (ie. solder bumps) on semiconductor chips, then directly bonding them to a printed circuit board or chip carrier substrate. The solder bumps are typically formed of SnPb.

Each solder is generally deposited on a thin film under-bump-metallization (***UBM***). Thin film UBMs which have been used commercially include Cr/Cr-Cu/Cu/Au and Al/Ni(V)/Cu thin films.

In flip chip technology, a silicon chip with a solderable UBM is flipped over and directly connected to a substrate through the bonding pad metallization. Flip chip technology is applied to area arrays which allow for high I/O counts at smaller pitches and reduced die size because solder bumps can be put over active device areas on ICs.

Development of solder flip chip interconnections was pursued so as to avoid the low productivity of the earlier manual wirebonding processes. Whereas in wirebonding processes, the bonds are formed sequentially (which is time-

consuming), the flip chip technique allows high I/O and also all I/Os to be connected simultaneously.

Flip chip technology typically uses lead-containing solder, such as 93% Pb/7%Sn, 95%Pb/5%Sn or eutectic 63%Sn/37%Pb solder bumps deposited upon solder wettable metal terminals on the active surface of the semiconductor chip that connect to matching wettable pads on the substrate. The solder bumps are aligned to the corresponding substrate metal pads and then reflowed at a temperature above their melting points to simultaneously form electrical and mechanical connections. During reflow, the wetting action of the solder, driven by surface tension forces, will align the chip's bump pattern to the corresponding substrate pad.

In flip chip technology, the solder interconnection system can be divided into the following areas:

- the under-bump-metallization (***UBM***);
- the solder bump; and
- the substrate pad metallization.

The UBM structure is typically designed to perform several functions, including:

- adhesion to the chip metallization;
- forming a barrier to solder diffusion and reaction; and
- wetting the solder and protecting the solder from oxidation.

In the deposition and formation of solder bumps, the assembly of the chip to the substrate (to form packaged components) and the assembly of the components to the board, the solder bump interconnections undergo a series of heating processes in which the solder is re-flowed to form metallurgical joints. The mechanical strength of the solder interconnections is governed by the strength of the solder bump and the strength of the interfaces, which in turn are influenced by the metallurgical and microstructural structures at the interfaces between the solder and the surface metallizations.

Over the last 20 years, only two substantial flip-chip thin film UBM systems have been in significant commercial use. The first such system is a Cr/Cr-Cu/Cu/Au system developed by IBM. The second such system is an Al/Ni(V)/Cu system developed by Delco. These UBM systems have proven to be effective for high-Pb and eutectic SnPb solders, respectively.

There are, however, a number of problems with the above-mentioned solder/thin film systems. For instance, eutectic SnPb has a low melting temperature (about 183°C) but is known to be incompatible with the Cr/Cr-Cu/Cu/Au UBM, owing to the rate and extent of spalling of the Cu_6Sn_5 intermetallic compounds (***IMCs***). Nickle-based UBMs have been used as alternatives to Cr/Cr-Cu/Cu/Au thin films owing largely to the fact that they have a much slower reaction rate with solders formed of SnPb so that, therefore, the spalling of the IMCs is slower.

For example, a trilayer UBM of Al/Ni(V)/Cu has been used with a Sn/Pb solder. It has been found that, in such a system, the IMCs (typically Cu_6Sn_5) adhere well to the Ni(V) surface and far less spalling occurs than has been observed in UBM structures consisting of Cr/Cr-Cu/Cu/Au thin films.

However, one of the problems with the above SnPb solders is that they are environmentally unfriendly. The toxic effects of lead on human beings, animals and the environment are well documented and there is a concern that the disposal of electronic products incorporating SnPb solders can result in environmental contamination. There is, therefore, a strong international push to eliminate lead from solders and to develop efficient lead-free solders for use in IC packaging.

Recent developments have shown that a eutectic SnAgCu solder bonded to a trilayer Al/Ni(V)/Cu thin film structure works reasonably well, although spalling of the IMCs was observed after about 20 reflow cycles which adversely affected the adhesion between the solder and the UBM. It is noted that this lowering of adhesion is greater than that observed when the solder is formed of eutectic SnPb after a similar number of reflow cycles. It has also been observed that when using Pb-free solders (eg. SnAgCu solder) on commercial substrate metallizations (such as Cu/Ni/Au and Cu/OSP) substantial reliability problems

are encountered. For example, when Cu/OSP substrate metallization is used under Pb-free soldering conditions, rapid growth of Cu-Sn intermetallic compounds was observed. This results in degradation of the fatigue properties of solder joints.

The use of Cu/Ni/Au substrate metallization results in slower reaction between the Sn and Ni and is therefore somewhat more reliable. However, this substrate metallization has also been found to have significant reliability issues for flip chip packages using Delco Al/Ni (V)/Cu UBM. It was found that fast IMC spalling could occur after only 3 ~ 5 reflows when SnAgCu solder was used. While in the case eutectic SnPb solder was applied, Ni (V) UBM consumed rapidly during thermal aging.

Accordingly, the present invention is directed to an improved substrate metallization which can be used effectively with Pb-free solders (but which is not necessarily limited to use with such solders).

Summary of the Invention

According to a first aspect of this invention, there is provided a substrate metallization for soldering, with a Pb-free solder or a eutectic SnPb solder, to a thin film under-bump-metallization (UBM) of a Si die, comprising:

- a substrate;
- a layer of Cu formed on a portion of the substrate;
- a layer of Ni formed on the Cu layer;
- an oxidation protection layer; and
- a Ni-barrier layer, between the Ni layer and the oxidation protection layer, adapted to inhibit diffusion of Ni from the Ni layer to the solder during a reflow process or during high temperature storage.

The Ni-barrier layer also serves as a wetting layer during the soldering process.

The Ni-barrier layer generally comprises a thin metallic film which may be formed of a single metal or an alloy. Particularly preferred metals in this regard

include copper, or an alloy like Cu_6Sn_5. Other metals, such as palladium, may also be able to be used.

The oxidation protection layer is preferably formed of Sn, Au, Ag, or Pd. Alternatively, the oxidation protection layer may be formed of Organic Solderable Preservative (***OSP***).

It is generally preferred that the Cu layer, the Ni layer and the Ni-barrier layer have (approximately) the following thicknesses:

- Cu layer – 5 μm to 10 μm
- Ni layer – 1 μm to 5 μm
- Ni-barrier layer – up to 1 μm

The Cu and Ni layers could be electroless or electrolytic plated. The metallic thin Ni-barrier layer can be plated or sputtered to the Ni surface.

Throughout this specification, unless the context requires otherwise, the word "comprise" or variations such as "comprises" or "comprising", will be understood to imply the inclusion of a stated element, integer or step, or group of elements, integers or steps, but not the exclusion of any other element, integer or step, or group of elements, integers or steps.

Any discussion of documents, acts, materials, devices, articles or the like, which has been included in the present specification, is solely for the purpose of providing a context for the present invention. It is not to be taken as an admission that any or all of these matters form part of the prior art base or were common general knowledge in the field relevant to the present invention as it existed before the priority date of each claim of this application.

In order that the present invention may be more clearly understood, the prior art and preferred forms of the invention will be described with reference to the following drawings and examples.

Brief Description of the Drawings

Figure 1 is a schematic illustration of a known commercial substrate metallization with a solder bump thereon.

Figure 2 is a multi-layer substrate metallization, according to a preferred embodiment of this invention, with a solder bump thereon.

Figure 3 is a SEM image of Delco UBM morphology after 5 reflows at 250°C with a SnAgCu Pb-free solder using a Cu/Ni(P)/Au commercial substrate metallization.

Figure 4 is a SEM image showing Delco UBM morphology after 5 reflows at 250°C with a SnAgCu Pb-free solder using the substrate metallization of the present invention.

Figure 5 is a SEM image showing Delco UMB morphology after 10 reflows at 220°C with a eutectic SnPb solder using a commercial Cu/Ni(P)/Au substrate metallization.

Figure 6 is a SEM image showing Delco UBM morphology after 10 reflows at 220°C with a eutectic SnPb solder using the substrate metallization of the present invention.

Figure 7a is a SEM image showing Delco UBM morphology after 500 hours aging at 150°C with a eutectic SnPb solder using the commercial Cu/Ni(P)/Au substrate metallization .

Figure 7b is a SEM image showing Delco UBM morphology after 500 hours aging at 150°C with a eutectic SnPb solder using the substrate metallization of the present invention.

Figure 7c is a graph showing electrical resistance changes over the 500 hours aging at 150°C referred to in Figure 7a.

Detailed Description of the Invention

A new substrate metallization has been invented for soldering on a Si die having a thin film UBM, such as Delco's Al/Ni(V)/Cu thin film UBM. Known substrate metallizations include Cu/Ni (P)/Au and Cu/OSP. A typical Cu/Ni (P)/Au substrate metallization is shown in Figure 1. Such a substrate metallization includes a substrate 1 on which is located a multi-layer metallization 2. This multi-layer metallization 2 consists of three layers. The first layer is a

copper layer 20. The second layer is a Ni (P) layer 21 and the third layer is an immersion Au layer 22. This immersion Au layer 22 forms an interface 3 with a solder 4.

The substrate metallization of this invention is a multi-layer metallization containing a layer of Cu, a layer of Ni, a Ni-barrier layer (eg. a film of Cu, or other metals or alloy film of Cu_6Sn_5 etc), and an oxidation protection layer (eg. a film of Sn, Au, Ag, Pd or OSP).

This multi-layer metallization is shown schematically in Figure 2. As can be seen, the substrate metallization includes a substrate 1 and a multi-layer metallization 2. This multi-layer metallization contains a Cu layer 20 on the substrate 1. On top of this, there is a Ni layer 21. On top of the Ni layer 21 is a Ni-barrier layer 23 which underlies an oxidation protection layer 22. This oxidation protection layer 22 forms an interface 3 with a solder 4.

Research undertaken indicates that the inclusion of the Ni-barrier layer in the substrate metallization reduces the amount of Ni which undergoes any reaction during the reflow process. This barrier layer successfully inhibits the involvement of Ni in the interfacial reactions occurring during the reflow process. Accordingly, the solder joint reliability is greatly improved.

Experiments have been undertaken in order to compare the results achieved when using a Cu/Ni(P)/Au as the substrate metallization and using the substrate metallization of the present invention. The results of these comparisons are shown in Figures 3 and 4, respectively.

A layer of metallic Cu film of less than 1 μm was formed on top of Ni (P) substrate. Si dies with Delco UBM and bumped with SnAgCu and eutectic SnPb solders were assembled to the modified substrate metallization. Multiple reflows and thermal aging were conducted after assembly. Samples were cross-sectioned and observed under SEM to study the evolution of Delco UBM under different conditions.

As can be seen from Figure 3, when Cu/Ni(P)/Au is used as the substrate metallization, a substantial degree of spalling of intermetallic compounds occurred after 5 reflows at 250°C in SnAgCu system. This spalling of the

intermetallic compounds substantially destroys the effectiveness of the UBM. It has also been found that when using the Cu/Ni(P)/Au substrate metallization, porous structure appeared in the UBM during thermal aging in the eutectic SnPb system (Fig. 7a). However, when the substrate metallization of this invention was used, the intermetallic compounds remained well-adhered to the UBM thin film (ie. there was no substantial spalling) after the same 5 reflows (Fig. 4). The use of the substrate metallization of the subject invention appeared to protect the UBM from cracking and to maintain its usefulness. During long time of thermal aging, Delco UBM also showed integrity structure after 500 hours of aging at 150°C using the present invented metallization as shown in Fig. 7b, as compared to the porous structure in Fig. 7a using commercial Cu/Ni (P)/Au substrate metallization.

The substrate metallization of the present invention does appear to function well with such known UBMs, such as Al/Ni(V)/Cu, with both Pb-free and eutectic SnPb solders after multiple reflows and long time of thermal aging. The arrangement of this substrate metallization inhibits Ni from interacting in the solder-UBM system. It also tends to avoid spalling of the intermetallic compounds and retards consumption of the UBM. The present invention also prevents the formation of porous structure in Delco UBM during the long time thermal aging in both SnAgCu and eutectic SnPb systems.

The present invention will have particular use in the field of flip chip packaging. However, it also has potential for use in CSP packaging (where thin film UBMs are used) and in BGA packaging which is presently the mainstream form of packaging in the IC packaging industry, without modification of solder compositions.

It will be appreciated by persons skilled in the art that numerous variations and/or modifications may be made to the invention as shown in these specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive.

Claims

The claims defining this invention are as follows:

1. A substrate metallization for soldering, with a Pb-free solder or a eutectic SnPb solder, to a thin film under-bump-metallization (UBM) of a Si die, comprising:
   - a substrate;
   - a layer of Cu formed on a portion of the substrate;
   - a layer of Ni formed on the Cu layer;
   - an oxidation protection layer; and

   a Ni-barrier layer, formed of a copper-tin alloy, between the Ni layer and the oxidation protection layer, adapted to inhibit diffusion of Ni from the Ni layer to the solder during a reflow process or during high temperature storage.

2. The substrate metallisation according to Claim 1, wherein the copper-tin alloy is Cu_6Sn_5.

3. The substrate metallisation according to Claim 1 or Claim 2, wherein the Ni-barrier layer comprises a thin film of the copper-tin alloy.

4. The substrate metallization according to any one of Claims 1 to 3, wherein the oxidation protection layer is formed of Sn, Au, Ag, Pd, or Organic Solderable Preservative (OSP).

5. The substrate metallization according to any one of Claims 1 to 4, wherein the Cu layer has a thickness of between about 5 μm and 10 μm.

6. The substrate metallization according to any one of Claims 1 to 5, wherein the Ni layer has a thickness of between about 1 μm and 5 μm.

7. The substrate metallization according to any one of Claims 1 to 6, wherein the Ni-barrier layer has a thickness of up to about 1 μm.

8. A packaged integrated circuit comprising the substrate metallization according to any one of Claims 1 to 7.

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