[68] The voltage level of the bit-line BL of each of the bit combinations “00”, “01”, “10”, and “11” in accordance with the first charge sharing operation thus may be captured as the MSB voltage V_{MSB} of about 0.35 V, 0.45 V, 0.55 V, or 0.65 V, respectively. At this time, the complementary bit-line BLB maintains the pre-charge voltage VPRE of 0.5 V. A prescribed voltage difference, that is, -150 mV, -50 mV, 50 mV, or 150 mV, may lie between the MSB voltage V_{MSB} of the bit-line BL and a complementary bit-line voltage V_{BLB} of 0.5 V, with the different prescribed voltage differences corresponding respectively to the bit combinations “00”, “01”, “10”, and “11”.

[69] In the sense amplifier 280 for sensing the LSB of the memory cell MC, when the second charge sharing operation is performed including charge sharing generated between the charges stored in the bit-line BL and the holding bit-line HBL and the charges stored in the first sensing bit-line SBL1, and also charge sharing generated between the charges stored in the complementary bit-line BLB and the complementary holding bit-line HBLB and the charges stored in the first complementary sensing bit-line SBLB1, the bit-line BL is captured as a prescribed LSB voltage V_{LSB}. The bit-line BL may be transited from the MSB voltage V_{MSB} to the LSB voltage V_{LSB}.

[70] For example, for the bit combination “00”, the voltage level of the bit-line BL having the MSB voltage V_{MSB} of about 0.35 V may be captured as the LSB voltage V_{LSB} of about 0.45 V in the second charge sharing operation. At this time, the voltage level of the complementary bit-line BLB may be captured as the complementary bit-line voltage V_{BLB} of about 0.5 V. For the bit combination “01”, the voltage level of the bit-line BL having the MSB voltage V_{MSB} of about 0.45 V may be captured as the LSB voltage V_{LSB} of about 0.5 V in the second charge sharing operation, and the complementary bit-line voltage V_{BLB} may be captured as 0.45 V. For the bit combination “10”, the voltage level of the bit-line BL having the MSB voltage V_{MSB} of 0.55 V may be captured as the LSB voltage V_{LSB} of about 0.5 V in

the second charge sharing operation, and the complementary bit-line voltage V_{BLB} may be captured as 0.55 V. For the bit combination “11”, the voltage level of the bit-line BL having the MSB voltage V_{MSB} of 0.65 V may be captured as the LSB voltage V_{LSB} of about 0.55 V in the second charge sharing operation, and the complementary bit-line voltage V_{BLB} may be captured as 0.5 V.

[71] The voltage level of the bit-line BL of each of the bit combinations “00” and “01” in accordance with the second charge sharing operation is captured as the LSB voltage V_{LSB} of about 0.45 V and 0.5 V, respectively, and the level of the complementary bit-line voltage V_{BLB} is captured as about 0.5 V and 0.45 V, respectively. The voltage level of the bit-line BL of each of the bit combinations “10” and “11” is captured as the LSB voltage V_{LSB} of about 0.5 V and 0.55 V, respectively, and the level of the complementary bit-line voltage V_{BLB} is captured as about 0.55 V and 0.5 V, respectively. A prescribed voltage difference, corresponding to each of the bit combinations “00”, “01”, “10”, and “11”, that is, -50 mV, 50 mV, -50 mV, or 50 mV, lies between the LSB voltage V_{LSB} of the bit-line BL and the complementary bit-line voltage V_{BLB}, which means that the LSB voltage V_{LSB} corresponding to each of the bit combinations “00”, “01”, “10”, and “11” operates as a self-reference that does not require an additional reference voltage for sensing the LSB voltage V_{LSB}.

[72] FIG. 5 is a circuit diagram illustrating an example of the sense amplifier in FIG. 3 according to according to example embodiments.

[73] Referring to FIG. 5, the sense amplifier 280 may include a sense amplifying circuit 280, a latch circuit 283 and a switching circuit including a bit-line switch SWa, a complementary bit-line switch SWb, a power witch SW10, and first to sixth switches SW1 to SW6.

[74] In some embodiments, the latch circuit 283 operates with a second power supply voltage, for example, VINTA2 applied to LA2 and with a third voltage level, which