WHAT IS CLAIMED IS:

1. A system for executing, by at least one computational device, a software program comprising a plurality of portions of program code, the system comprising:

a plurality of processing cores, connected to the at least one computational device, comprising a plurality of computation groups each comprising some of the plurality of processing cores; and

at least one processing circuitry adapted for configuring the plurality of processing cores to execute at least some of the plurality of portions of program code by, in each of a plurality of configuration iterations:

accessing at least one program code pattern comprising two or more portions of program code of the plurality of portions of program code, each pattern indicative of an association in occurrence of the respective two or more portions of program code when executing the software program; and

for each of the at least one program code pattern, configuring at least some of the plurality of computation groups to each execute at least part of one of the respective two or more portions of program code according to the at least one program code pattern.

2. The system of claim 1, wherein executing the software program by the at least one computational device comprises executing thereby a first set of portions of program code selected from the plurality of portions of program code while the plurality of processing cores execute a second set of portions of program code selected from the plurality of portions of program code.

3. The system of claim 1, wherein the at least one processing circuitry is further adapted for at least one of:

receiving, in at least one of the plurality of configuration iterations, the at least one program code pattern from at least one other processing circuitry; and

computing, in at least one other of the plurality of configuration iterations, the at least one program code pattern by:

receiving a plurality of calls, each for executing one of the plurality of portions of program code; and

identifying in the plurality of calls the at least one program code pattern.

4. The system of claim 1, wherein the at least one program code pattern comprises at least one of:

a first program code pattern having a first portion of code of the respective two or more portions of program code and a second portion of code of the respective two or more portions of code where a first frequency, in the plurality of calls, of an occurrence one after another of the first portion of program code and the second portion of program code exceeds a predetermined threshold frequency;

a second program code pattern having a third portion of code of the respective two or more portions of program code and a fourth portion of code of the respective two or more portions of code where a second frequency, in the plurality of calls, of the third portion of code invoking the fourth portion of code exceeds the predetermined threshold frequency; and

a third code pattern and a fourth code pattern, each having a fifth portion of code of the respective two or more portions of program code.

5. The system of claim 4,

wherein the plurality of processing cores is organized in at least one computation grid; and

wherein configuring at least some of the plurality of computation groups comprises for the first program code pattern configuring at least one first computation group of the plurality of computation groups to execute the first portion of program code where the at least one first computation group is located in the at least one computation grid in topological proximity to at least one second computation group configured to execute the second portion of program code.

6. The system of claim 4,

wherein the plurality of processing cores is organized in at least one computation grid; and

wherein configuring at least some of the plurality of computation groups comprises for the second program code pattern configuring at least one third computation group of the plurality of computation groups to execute the third portion of program code where the at least one third computation group is located in the at least

one computation grid in topological proximity to at least one fourth computation group configured to execute the fourth portion of program code.

7. The system of claim 4, wherein configuring at least some of the plurality of computation groups comprises configuring at least two computation groups of the plurality of computation groups to execute the fifth portion of program code.

8. The system of claim 1, wherein the plurality of processing cores is organized in at least one computation grid; and

wherein configuring at least some of the plurality of computation groups comprises for at least one of the at least one program code pattern:

identifying at least two of the plurality of computation groups each configured to execute at least part of one of the respective two or more portions of program code;

selecting at least two other of the plurality of computation groups such that the at least two other computation groups are located in the computation grid in topological proximity to each other; and

configuring each of the at least two other computation groups to execute at least part of one of the respective two or more portions of program code the at least two computation groups were configured to execute.

9. The system of claim 1, wherein the plurality of processing cores is organized in at least one computation grid; and

wherein configuring at least some of the plurality of computation groups comprises for at least one of the at least one program code pattern:

identifying at least one first of the plurality of computation groups configured to execute a first portion of program code of the respective two or more portions of program code; and

configuring at least one second of the plurality of computation groups to execute a second portion of program code of the respective two or more portions of program code where the at least one second of the plurality of computation groups is located in the computation grid in topographical proximity to the at least one first computation group.

10. The system of claim 1, wherein configuring at least some of the plurality of computation groups further comprises:

releasing at least one computation group of the plurality of computation groups not accessed by any other of the plurality of computation groups and not accessed by the computational device.

11. The system of claim 1, wherein the at least one processing circuitry is adapted for configuring the plurality of processing cores while the software program is executed by the at least one computational device and the plurality of processing cores.

12. The system of claim 1, wherein the at least one computational device is any one of: a multi-core central processing unit (CPU), a field-programmable gate array (FPGA), a graphics processing unit (GPU), a coarse-grained configurable architecture (CGRA), an intelligence processing unit (IPU), a neural-network accelerator, an application-specific integrated circuit (ASIC), and a quantum computer.

13. The system of claim 1, further comprising a plurality of configurable data routing junctions;

wherein the plurality of processing cores is a plurality of logical elements organized in at least one computational grid, such that each of the plurality of computation groups comprises some of the plurality of logical elements connected by some of the plurality of configurable data routing junctions.

14. A method for executing, by at least one computational device, a software program comprising a plurality of portions of program code, comprising:

configuring a plurality of processing cores to execute at least some of the plurality of portions of program code, the plurality of processing cores comprising a plurality of computation groups, each comprising some of the plurality of processing cores, by, in each of a plurality of configuration iterations:

accessing at least one program code pattern comprising two or more of the plurality of portions of program code, each pattern indicative of an

association in occurrence of the respective two or more portions of program code when executing the software program; and

for each of the at least one program code pattern, configuring at least some of the plurality of computation groups to each execute at least part of one of the respective two or more portions of program code according to the at least one program code pattern.

15. A non-transitory computer readable medium having stored thereon instructions for causing a processing unit to execute a process for executing, by at least one computational device, a software program comprising a plurality of portions of program code, the process comprising:

configuring a plurality of processing cores to execute at least some of the plurality of portions of program code, the plurality of processing cores comprising a plurality of computation groups, each comprising some of the plurality of processing cores, by, in each of a plurality of configuration iterations:

accessing at least one program code pattern comprising two or more of the plurality of portions of program code, each pattern indicative of an association in occurrence of the respective two or more portions of program code when executing the software program; and

for each of the at least one program code pattern, configuring at least some of the plurality of computation groups to each execute at least part of one of the respective two or more portions of program code according to the at least one program code pattern.