

Description

Background of the invention

This invention relates, in general, to programmable read only memories (PROM) and more particularly, to an erase detector for those programmable read only memories which are erasable.

Read only memories are well known and widely used in digital systems. More recently, programmable read only memories (PROM) have come into use. Some of these memories are programmable by the use of high voltage to program a predetermined cell within the memory after the memory is made. These programmed memories can also be altered or erased. Some times the erasure is accomplished by exposure to radiation such as ultraviolet radiation.

One of the conveniences of this type of memory is that it can be programmed after it is manufactured instead of requiring programming by a mask operation during the manufacturing process. Many times once the memory is programmed it is desirable to maintain the program without modifications, and in such cases it is important to determine whether the data within the memory has been tampered with, altered, or erased. Patent documents FR-A-2311360 and US-A-4092524 describe a programmable and erasable memory coupled to a data bus via gates for reading and writing. These documents further describe an additional memory cell which may be programmed to allow or inhibit access to the programmable memory via the gates. The article of ELANDER "External EAROM Content Change Sensor" in IBM Technical Disclosure Bulletin, Volume 22, No. 9, February 1980, pages 4113-4114, describes a method for detecting erasure of programmable read only memory using two erasable memory cells and a fusible link wherein after programming one of the memory cells the link is burned and further programming is not possible. If the memory is erased the two memory cells will have the same state and the erasure is therefore detected.

Accordingly, it is an object of the present invention to provide a new and improved erase detector for a programmable read only memory.

Another object of the present invention is to provide a method for detecting whether a programmable read only memory has been erased.

Yet a further object of the present invention is to provide a substantially fool-proof circuit for determining whether a programmable read only memory has been erased.

Summary of the invention

In accordance with a first aspect of the present invention there is provided an erase detector for a programmable read only memory having a data bus to detect when the memory has been erased, said erase detector including a latch having an input coupled to said data bus and having an output; a programmable memory cell having a control input coupled to the output and having a

node coupled to said data bus, so that, when said programmable memory cell is in a programmed state, the state of said latch may be read out to said data bus, but when said programmable memory cell is in the erased state, the output of said latch is inhibited; programming pads coupled to program said programmable memory cell and means to sever said programming pads said programming pads being severed after said programmable memory cell has been programmed, so that, in case said programmable read only memory and said programmable memory cell are erased, said programmable memory cell cannot be reprogrammed and the state of said latch cannot be read out, indicating that said programmable read only memory has been erased.

In accordance with a second aspect of the present invention there is provided a method for detecting erasure of a programmable read only memory, including providing latching means for storing a data bit from a bus; providing a programmable memory cell coupled to an output of said latching means; and disabling programming pads to said programmable memory cell after said programmable memory cell has been programmed so that if said programmable read only memory is erased, said programmable memory cell is erased also and may not be reprogrammed; said latching means providing a predetermined state to the data bus independently of the data bit stored in said latching means when said programmable memory cell is not programmed, and providing the state stored in said latching means when said programmable memory cell is programmed.

Brief description of the drawings

Fig. 1 illustrates the invention in one form thereof; and

Fig. 2 illustrates a flow diagram of a method of how the erase detector circuit is interrogated.

Detailed description of the drawings

Latch 10 has its D input controllably coupled to data bus 11 by transistor 12. Transistor 12 is controlled by a write signal which is generated by a processor unit associated with the programmable read only memory (PROM) near which the circuitry of Fig. 1 is located. The output Q of latch 10 is coupled by high voltage protection circuit 13 to gate electrodes 14 and 22 of transistors 17 and 21 respectively. Transistor 21 is a programmable transistor and can be identical to the programmable transistors located in the programmable read only memory. The drain of transistor 17 is connected to a voltage terminal 16 which receives voltage V_{DD} . The source electrode of transistor 17 is coupled by high voltage protection circuit 18 to node 19. Transistor 21 has its drain electrode connected to node 19 and has its source electrode connected to a reference terminal 23 illustrated as ground. Programming pads 26 and 27 are coupled to node 19 and to control electrode 22 respectively.

a preferred embodiment, programming pads 26 and 27 are severed from node 19 and electrode 22 respectively. Lines 28 illustrate means for severing contact pads 26 and 27. These contact pads can be severed by laser burning of the connecting lines, by having fusible links within the lines at 28 which are destroyed once transistor 22 is programmed, or the connecting lines can be severed during scribing. It is well known by those persons of skill in the art that a plurality of integrated circuits are made on one wafer. Scribe lines are used between the integrated circuits to weaken the wafer so that the wafer can be broken or cut along the scribe lines thereby separating the plurality of integrated circuits. In the present embodiment if the scribe line is used to sever programming pads 26 and 27 from node 19 and control electrode 22 then the connecting lines must extend across the scribe line adjacent to the integrated circuit on which transistor 21 is located. A certain critical code can be entered in the PROM during wafer test and then the connecting lines will be severed during separation of the integrated circuit containing transistor 21 from the wafer.

Node 19 is coupled to transistor 32 and to amplifier 34 by high voltage protection circuits 31 and 33 respectively. Transistor 32 has its control electrode connected to voltage V_{DD} , its source connected to voltage terminal 23, and its drain electrode coupled to sense line 29 by high voltage protection circuit 31. Line 29 is coupled to the input of amplifier 34 by high voltage protection circuit 33. The output of amplifier 34 is coupled to data bus 11 by transistor 36. Transistor 36 is controlled by a read signal which is generated by the associated processor.

High voltage protection circuits 13, 18, 31 and 33 are all identical, and in a preferred embodiment, have one transistor whose control electrode is connected to voltage V_{DD} . The arrangement of this single transistor is illustrated in conjunction with high voltage protection circuit 13. The purpose of the high voltage protection circuits is to keep the programming voltage applied to transistor 21 from damaging PN regions of the other devices. The other devices include transistors 17 and 32, latch 10 transistors, and amplifier 34 transistors. The failure mode is breakdown caused by very high electric fields on the depletion region between the P and N junction of the field effect transistors.

Latch 10, in a preferred embodiment, includes two series connected inverters with the first inverter having its input connected to D its output connected to the input of the second inverter and the second inverter having its output connected to Q. A feedback path is then supplied from the output Q to the input D by any suitable means such as by a feedback resistor or the like.

Before transistor 21 is programmed, and assuming latch 10 is providing a zero logic level at its Q output, transistors 17 and 21 will be in a nonconducting state since the zero logic level is not high enough to overcome the threshold volt-

age of transistors 17 and 21. Node 19 and sense line 29 will then be held to a zero logic level by transistor 32. Transistor 32 is to prevent sense line 29 from floating when transistors 17 and 21 are nonconducting.

If the output Q of latch 10 is a logic level 1 then both transistors 17 and 21 will be conductive. However, when transistor 21 is unprogrammed it will exhibit a much lower impedance than does transistor 17 and transistor 32 will exhibit a much higher impedance than does transistor 17. With transistors 17 and 21 both conducting, transistor 21 will tend to pull node 19 towards ground which is the lowest potential in the circuit and corresponds to a logic level 0 which is coupled to amplifier 34. The output of amplifier 34 is coupled back to bus 11 by transistor 36. In summary, when transistor 21 is unprogrammed the output of amplifier 34 will remain at a logic level 0 regardless of the output of latch 10.

Transistor 21 can be programmed by applying a high voltage at programming pads 26 and 27. This voltage can be in the order of 20 to 25 volts and will cause the threshold of transistor 21 to change from approximately 2 volts to some value above the normal supply voltage, V_{DD} . Therefore, when a typical logic level 1 is applied to control electrode 22 transistor 21 will not be enabled. However, a logic level 1 will cause transistor 17 to be enabled which causes node 19 to rise to a logic level 1 which is amplified by amplifier 34 and coupled back to data bus 11. When latch 10 provides a logic level 0 output transistor 17 is not enabled nor is transistor 21. In this case transistor 32 will maintain sense line 29 and node 19 at a logic low level which will be amplified by amplifier 34 and coupled to data bus 11. Therefore when transistor 21 is programmed the output of latch 10 is reflected at node 19 and coupled by amplifier 34 to data bus 11.

Once transistor 21 becomes programmed it will always be in an "off" or non-conducting state and will exhibit a much higher impedance than does transistor 32, and it is noted hereinbefore that transistor 32 exhibits a higher impedance than does transistor 17. In a preferred embodiment, the drain of transistor 21 as well as sense line 29 are made in the diffusion of the integrated circuit and the diffusion is covered by metal lines. This affords a greater protection to the integrity of transistor 21 by making it almost impossible for someone to program transistor 21 by probing down to node 19 or sense line 29.

Also provided is a method of detecting when a PROM is erased. As an example, transistor 21 is placed adjacent to a PROM and if someone attempts to erase the PROM by providing a mask over all the circuitry (except the PROM) to protect the circuitry outside the PROM from being bombarded with radiation, transistor 21 will still be erased, since in a typical configuration the transistor as well as the PROM are covered by a layer of silicon dioxide which in turn has a passivation layer on top of it. Therefore as the radiation penetrates through the passivation layer and the

silicon die to reach the PROM it begins to bounce back and forth between the passivation layer and the silicon substrate and travels beneath the mask to the programmable transistor thereby unprogramming or erasing it also. This mechanism is commonly called total internal reflection.

Once a desired code is entered into the PROM and programmable transistor 21 is programmed the memory is then ready for use in a system. Each time before a program is executed using the PROM a check can be made to determine whether the PROM has been erased or not. A flowchart for this check is illustrated in Fig. 2. At the start of the program the circuitry is reset. A logic level 1 is then read into the erase protection (EPR) latch (illustrated as latch 10 in Fig. 1). The output of the latch is then read and if the logic level read is not a logic level 1 the program can be aborted, however, if a logic level 1 is read then a zero will be written into the erase protection latch and an attempt will be made to read this logic level 0. If a logic level 0 is not read the program will be aborted but if a logic level 1 is read then the program shall continue. This procedure will also detect the case where a potential defrauder hardwires the output of amplifier 34 in an attempt to bypass the security afforded by the erase detection circuit.

By now it should be appreciated that there has been provided an erase detector circuit for a PROM which requires only one programmable transistor and is virtually tamper proof.

Claims

1. An erase detector for a programmable read only memory having a data bus (11) to detect when the memory has been erased, said erase detector including a latch (10) having an input (D) coupled to said data bus (11) and having an output (Q); a programmable memory cell (21) having a control input coupled to the output (Q) and having a node (19) coupled to said data bus (11), so that, when said programmable memory cell (21) is in a programmed state, the state of said latch (10) may be read out to said data bus (11), but when said programmable memory cell (21) is in the erased state, the output (Q) of said latch (10) is inhibited; programming pads (26, 27) coupled to program said programmable memory cell (21) and means (28) to sever said programming pads (26, 27) said programming pads being severed after said programmable memory cell (21) has been programmed, so that, in case said programmable read only memory and said programmable memory cell (21) are erased, said programmable memory cell (21) cannot be reprogrammed and the state of said latch (10) cannot be read out, indicating that said programmable read only memory has been erased.

2. The erase detector circuit of claim 1 further characterized by a first transistor (17) coupled between a first supply voltage terminal (16) and said node (19), and having a control terminal coupled to the output (Q) of said latch (10).

3. The erase detector of claim 1 or 2 further characterized by an amplifier (34) coupled between said node (19) and said data bus (11).

4. The erase detector of claim 3 further characterized by a second transistor (12) coupled between said data bus (11) and said latch input (D) and having a control terminal coupled to a write signal, and a third transistor (36) coupled between said data bus (11) and the output of said amplifier (34) and having a control terminal coupled to a read signal.

5. The erase detector of claim 2, 3 or 4 further characterized by a fifth transistor (32) coupled between said node (19) and a second supply voltage terminal (23) and having a control terminal coupled to said first supply voltage terminal (16).

6. The erase detector of claim 5 when dependent from claim 3 or 4 further characterized by first, second, third, and fourth high voltage protection means (13, 18, 31, and 33) to protect said latch (10), said first transistor (17), said fifth transistor (32), and said amplifier (34), respectively.

7. The erase detector of claim 6 wherein said first high voltage protection means (13) is further characterized by a transistor coupled between the output (Q) and both the control electrodes of said programmable memory cell (21) and said first transistor (17), and having its control electrode coupled to said first supply voltage terminal (16), said second, third, and fourth high voltage protection means (18, 31, 33) are further characterized by transistors coupled between the node (19) and said first transistor (17), said fifth transistor (32), and said amplifier (34), respectively each of said transistors having a control terminal coupled to said first supply voltage terminal (16).

8. A method for detecting erasure of a programmable read only memory, including providing latching means (10) for storing a data bit from a bus (11); providing a programmable memory cell (21) coupled to an output (Q) of said latching means; and disabling programming pads (26, 27) to said programmable memory cell after said programmable memory cell has been programmed so that if said programmable read only memory is erased, said programmable memory cell is erased also and may not be reprogrammed; said latching means providing a predetermined state to the data bus (11) independently of the data bit stored in said latching means when said programmable memory cell is not programmed, and providing the state stored in said latching means when said programmable memory cell is programmed.

Patentansprüche

1. Löschdetektor für einen programmierbaren Nur-Lese-Speicher, mit einem Datenbus (11), um zu ermitteln, wenn der Speicher gelöscht worden ist, welcher Löschdetektor eine Verriegelungsschaltung (10) mit einem Eingang (D) aufweist, der mit dem Datenbus (11) verbunden ist, und einen Ausgang (Q) aufweist; einer programmierbaren Speicherzelle (21), die einen Steuereingang hat,

silicon dioxide to reach the PROM it begins to bounce back and forth between the passivation layer and the silicon substrate and travels beneath the mask to the programmable transistor thereby unprogramming or erasing it also. This mechanism is commonly called total internal reflection.

Once a desired code is entered into the PROM and programmable transistor 21 is programmed the memory is then ready for use in a system. Each time before a program is executed using the PROM a check can be made to determine whether the PROM has been erased or not. A flowchart for this check is illustrated in Fig. 2. At the start of the program the circuitry is reset. A logic level 1 is then read into the erase protection (EPR) latch (illustrated as latch 10 in Fig. 1). The output of the latch is then read and if the logic level read is not a logic level 1 the program can be aborted, however, if a logic level 1 is read then a zero will be written into the erase protection latch and an attempt will be made to read this logic level 0. If a logic level 0 is not read the program will be aborted but if a logic level 1 is read then the program shall continue. This procedure will also detect the case where a potential defrauder hardwires the output of amplifier 34 in an attempt to bypass the security afforded by the erase detection circuit.

By now it should be appreciated that there has been provided an erase detector circuit for a PROM which requires only one programmable transistor and is virtually tamper proof.

Claims

1. An erase detector for a programmable read only memory having a data bus (11) to detect when the memory has been erased, said erase detector including a latch (10) having an input (D) coupled to said data bus (11) and having an output (Q); a programmable memory cell (21) having a control input coupled to the output (Q) and having a node (19) coupled to said data bus (11), so that, when said programmable memory cell (21) is in a programmed state, the state of said latch (10) may be read out to said data bus (11), but when said programmable memory cell (21) is in the erased state, the output (Q) of said latch (10) is inhibited; programming pads (26, 27) coupled to program said programmable memory cell (21) and means (28) to sever said programming pads (26, 27) said programming pads being severed after said programmable memory cell (21) has been programmed, so that, in case said programmable read only memory and said programmable memory cell (21) are erased, said programmable memory cell (21) cannot be reprogrammed and the state of said latch (10) cannot be read out, indicating that said programmable read only memory has been erased.

2. The erase detector circuit of claim 1 further characterized by a first transistor (17) coupled between a first supply voltage terminal (16) and said node (19), and having a control terminal coupled to the output (Q) of said latch (10).

3. The erase detector of claim 1 or 2 further characterized by an amplifier (34) coupled between said node (19) and said data bus (11).

4. The erase detector of claim 3 further characterized by a second transistor (12) coupled between said data bus (11) and said latch input (D) and having a control terminal coupled to a write signal, and a third transistor (36) coupled between said data bus (11) and the output of said amplifier (34) and having a control terminal coupled to a read signal.

5. The erase detector of claim 2, 3 or 4 further characterized by a fifth transistor (32) coupled between said node (19) and a second supply voltage terminal (23) and having a control terminal coupled to said first supply voltage terminal (16).

6. The erase detector of claim 5 when dependent from claim 3 or 4 further characterized by first, second, third, and fourth high voltage protection means (13, 18, 31, and 33) to protect said latch (10), said first transistor (17), said fifth transistor (32), and said amplifier (34), respectively.

7. The erase detector of claim 6 wherein said first high voltage protection means (13) is further characterized by a transistor coupled between the output (Q) and both the control electrodes of said programmable memory cell (21) and said first transistor (17), and having its control electrode coupled to said first supply voltage terminal (16), said second, third, and fourth high voltage protection means (18, 31, 33) are further characterized by transistors coupled between the node (19) and said first transistor (17), said fifth transistor (32), and said amplifier (34), respectively each of said transistors having a control terminal coupled to said first supply voltage terminal (16).

8. A method for detecting erasure of a programmable read only memory, including providing latching means (10) for storing a data bit from a bus (11); providing a programmable memory cell (21) coupled to an output (Q) of said latching means; and disabling programming pads (26, 27) to said programmable memory cell after said programmable memory cell has been programmed so that if said programmable read only memory is erased, said programmable memory cell is erased also and may not be reprogrammed; said latching means providing a predetermined state to the data bus (11) independently of the data bit stored in said latching means when said programmable memory cell is not programmed, and providing the state stored in said latching means when said programmable memory cell is programmed.

Patentansprüche

1. Löschedetektor für einen programmierbaren Nur-Lese-Speicher, mit einem Datenbus (11), um zu ermitteln, wenn der Speicher gelöscht worden ist, welcher Löschedetektor eine Verriegelungsschaltung (10) mit einem Eingang (D) aufweist, der mit dem Datenbus (11) verbunden ist, und einen Ausgang (Q) aufweist; einer programmierbaren Speicherzelle (21), die einen Steuereingang hat,



mit dem Ausgang (Q) verbunden ist, und mit einem Verbindungspunkt (19), der mit dem Datenbus (11) verbunden ist, so daß, wenn die programmierbare Speicherzelle (21) sich in einem programmierten Zustand befindet, der Zustand der Verriegelungsschaltung (10) zum Datenbus (11) ausgelesen werden kann, jedoch wenn die programmierbare Speicherzelle (21) sich in dem gelöschten Zustand befindet, der Ausgang (Q) der Verriegelungsschaltung (10) gesperrt ist; mit Programmieranschlüssen (26, 27), die verbunden sind, um die programmierbare Speicherzelle (21) zu programmieren, und mit Einrichtungen (28), um die Programmieranschlüsse (26, 27) zu trennen, welche Programmieranschlüsse getrennt werden, nachdem die programmierbare Speicherzelle (21) programmiert worden ist, so daß im Falle, daß der programmierbare Nur-Lese-Speicher und die programmierbare Speicherzelle (21) gelöscht sind, die programmierbare Speicherzelle (21) nicht neu programmiert werden kann und der Zustand der Verriegelungsschaltung (10) nicht ausgelesen werden kann, was anzeigt, daß der programmierbare Nur-Lese-Speicher gelöscht worden ist.

2. Löschdetektorschaltung nach Anspruch 1, weiterhin gekennzeichnet durch einen ersten Transistor (17), der zwischen einen ersten Versorgungsspannungsanschluß (16) und den Verbindungspunkt (19) geschaltet ist und der einen Steueranschluß hat, der mit dem Ausgang (Q) der Verriegelungsschaltung (10) verbunden ist.

3. Löschdetektor nach Anspruch 1 oder 2, weiterhin gekennzeichnet durch einen Verstärker (34), der zwischen den genannten Verbindungspunkt (19) und den Datenbus (11) geschaltet ist.

4. Löschdetektor nach Anspruch 3, weiterhin gekennzeichnet durch einen zweiten Transistor (12), der zwischen den Datenbus (11) und den Verriegelungsschaltungseingang (D) geschaltet ist und der einen Steueranschluß hat, der an ein Schreibsignal angeschlossen ist, und einen dritten Transistor (36), der zwischen den Datenbus (11) und den Ausgang des Verstärkers (34) geschaltet ist und der einen Steueranschluß hat, der mit einem Lesesignal verbunden ist.

5. Löschdetektor nach Anspruch 2, 3 oder 4, weiterhin gekennzeichnet durch einen fünften Transistor (32), der zwischen den genannten Verbindungspunkt (19) und einen zweiten Versorgungsspannungsanschluß (23) geschaltet ist und der einen Steueranschluß hat, der mit dem ersten Versorgungsspannungsanschluß (16) verbunden ist.

6. Löschdetektor nach Anspruch 5, wenn abhängig von den Ansprüchen 3 oder 4, weiterhin gekennzeichnet durch erste, zweite, dritte und vierte Hochspannungsschutzeinrichtungen (13, 18, 31 und 33) zum Schutz der Verriegelungsschaltung (10), des ersten Transistors (17), des fünften Transistors (32) bzw. des Verstärkers (34).

7. Löschdetektor nach Anspruch 6, bei dem die erste Hochspannungsschutzeinrichtung (13) weiterhin gekennzeichnet ist durch einen Transistor, der zwischen den Ausgang (Q) und sowohl die

Steuerelektroden der programmierbaren Speicherzelle (21) und den ersten Transistor (17) geschaltet ist und dessen Steuerelektrode mit dem ersten Versorgungsspannungsanschluß (16) verbunden ist, und daß die zweiten, dritten und vierten Hochspannungsschutzeinrichtungen (18, 31, 33) weiterhin durch Transistoren gekennzeichnet sind, die zwischen den Verbindungspunkt (19) und den ersten Transistor (17), den fünften Transistor (32) bzw. den Verstärker (34) geschaltet sind, wobei jeder der Transistoren einen Steueranschluß hat, der mit dem ersten Versorgungsspannungsanschluß (16) verbunden ist.

8. Verfahren zur Ermittlung der Löschung eines programmierbaren Nur-Lese-Speichers, enthaltend: Vorkehrung einer Verriegelungseinrichtung (10) zum Speichern eines Datenbits von einem Bus (11); Vorkehrung einer programmierbaren Speicherzelle (21), die mit einem Ausgang (Q) der Verriegelungseinrichtung verbunden ist; und Sperren von Programmieranschlüssen (26, 27) zu der programmierbaren Speicherzelle, nachdem die programmierbare Speicherzelle programmiert worden ist, so daß, wenn der programmierbare Nur-Lese-Speicher gelöscht wird, die programmierbare Speicherzelle ebenfalls gelöscht wird und nicht neu programmiert werden kann; wobei die Verriegelungseinrichtung einen vorbestimmten Zustand an den Datenbus (11) unabhängig von dem in der Verriegelungseinrichtung gespeicherten Datenbit liefert, wenn die programmierbare Speicherzelle nicht programmiert ist, und den in der Verriegelungseinrichtung gespeicherten Zustand liefert, wenn die programmierbare Speicherzelle programmiert ist.

Revendications

1. Détecteur d'effacement pour mémoire morte programmable possédant un bus de données (11), qui permet de déterminer si la mémoire a été effacée, ledit détecteur d'effacement comportant un circuit de verrouillage (10) qui possède une entrée (D) couplée audit bus de données (11) ainsi qu'une sortie (Q); une cellule de mémoire programmable (21) comportant une entrée de commande couplée à la sortie (Q) et comportant un noeud (19) couplé audit bus de données (11), de sorte que, lorsque ladite cellule de mémoire programmable (21) est dans un état programmé, l'état dudit circuit de verrouillage (10) peut être lu sur ledit bus de données (11), mais, lorsque ladite cellule de mémoire programmable (21) est dans l'état effacé, la sortie (Q) dudit circuit de verrouillage (10) est invalidée; des plots de programmation (26, 27) couplés de manière à programmer ladite cellule de mémoire programmable (21) et un moyen (28) permettant de couper lesdits plots de programmation (26, 27), lesdits plots de programmation étant coupés après que ladite cellule de mémoire programmable (21) a été programmée, de sorte que, dans le cas où ladite mémoire morte programmable et ladite cellule de mémoire programmable (21) ont été effacées, ladite cellule de mémoire programmable (21) ne peut pas être



rer programmée et l'état dudit circuit de verrouillage (10) ne peut pas être lu, ce qui indique que la mémoire morte programmable a été effacée.

2. Détecteur d'effacement selon la revendication 1, caractérisé en outre par un premier transistor (17) couplé entre une première borne (16) d'alimentation électrique et ledit noeud (19), et comportant une borne de commande couplée à la sortie (Q) dudit circuit de verrouillage (10).

3. Détecteur d'effacement selon la revendication 1 ou 2, caractérisé en outre par un amplificateur (34) couplé entre ledit noeud (19) et ledit bus de données (11).

4. Détecteur d'effacement selon la revendication 3, caractérisé en outre par un deuxième transistor (12) couplé entre ledit bus de données (11) et ladite entrée (D) du circuit de verrouillage et comportant une borne de commande couplée à un signal d'écriture, et par un troisième transistor (36) couplé entre ledit bus de données (11) et la sortie dudit amplificateur (34) et comportant une borne de commande couplée à un signal de lecture.

5. Détecteur d'effacement selon la revendication 2, 3 ou 4, caractérisé en outre par un cinquième transistor (32) couplé entre ledit noeud (19) et une deuxième borne (23) d'alimentation électrique et comportant une borne de commande couplée à ladite première borne d'alimentation électrique (16).

6. Détecteur d'effacement selon la revendication 5 prise en dépendance avec la revendication 3 ou 4, caractérisé en outre par un premier, un deuxième, un troisième et un quatrième moyen de protection contre les tensions élevées (13, 18, 31 et 33) servant à respectivement protéger ledit circuit de verrouillage (10), ledit premier transistor (17), ledit cinquième transistor (32), et ledit amplificateur (34).

7. Détecteur d'effacement selon la revendica-

tion 6, où ledit premier moyen (13) de protection contre les tensions élevées est en outre caractérisé par un transistor couplé entre la sortie (Q) et les deux électrodes de commande de ladite cellule de mémoire programmable (21) et dudit premier transistor (17), et par le fait que l'électrode de commande de ce transistor est couplée à ladite première borne (16) de tension d'alimentation électrique, où lesdits deuxième, troisième et quatrième moyens (18, 31, 33) de protection contre les tensions élevées sont en outre caractérisés par des transistors respectivement couplés entre le noeud (19) et ledit premier transistor (17), ledit cinquième transistor (32), et ledit amplificateur (34), chacun desdits transistors possédant une borne de commande couplée à ladite première borne de tension d'alimentation (16).

8. Procédé permettant de détecter l'effacement d'une mémoire morte programmable, qui comporte les opérations consistant à prévoir un moyen de verrouillage (10) servant à emmagasiner un bit de donnée en provenance d'un bus (11); à prévoir une cellule de mémoire programmable (21) couplée à une sortie (Q) dudit moyen de verrouillage; et à invalider des plots de programmation (26, 27) de ladite cellule de mémoire programmable après que ladite cellule de mémoire programmable a été programmée, de sorte que, si ladite mémoire morte programmable est effacée, ladite cellule de mémoire programmable est effacée également et ne peut pas être reprogrammée; ledit moyen de verrouillage produisant un état prédéterminé sur le bus de données (11) indépendamment du bit de donnée emmagasiné dans ledit moyen de verrouillage lorsque ladite cellule de mémoire programmable n'est pas programmée, et produisant l'état emmagasiné dans ledit moyen de verrouillage lorsque ladite cellule de mémoire programmable est programmée.

