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Semiconductor Integrated Circuit Device

5 The present invention relates to a semiconductor integrated circuit device including ECL (Emitter Coupled Logic).

 In semiconductor integrated circuit
10 devices including ECL (or CML: Current Mode Logic), it is well known in the art from Japanese Patent Laid-Open No. 134780 / 1975 that an internal logic amplitude may be made smaller than an external one so as to speed up the internal operation
15 and reduce the power consumption of the semiconductor integrated circuit device.

 Such a semiconductor integrated circuit device has its output circuit formed by a conventional logic circuit which operates at a normal logic amplitude.
20 As a result, the operating margin of the output signal is enlarged and it can be fed out to external wiring outside the integrated circuit which has a high noise induction or the like. On the contrary, an internal ECL circuit inside the integrated circuit is formed
25 by a minor amplitude ECL circuit (i.e. one which

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operates at a smaller amplitude) so as to ensure the
aforementioned speed-up and reduction in the power
consumption because it is hardly influenced by the
noises or the like.

5 In the semiconductor integrated circuit
thus far described, the inside ECL circuit is
made to have its lower logic signal level set at a
relatively high voltage level. Accordingly the integrated circuit
device is equipped with an input circuit for
10 receiving an external input signal having a
normal level.

The input circuit is has a con-
struction, similar to that of the usual ECL circuit,
such that it has a threshold
15 voltage when it is supplied with a suitable
reference voltage which is suitable for the external
input signal. Moreover, the input circuit solves the
following problems which are caused when the
external input signal is fed directly to the
20 inside ECL circuit.

Specifically, the inside ECL circuit
has its logic threshold voltage set at a relatively

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high level. Accordingly, the difference between the high level of the external input signal and the logic threshold voltage of the inside ECL circuit is made relatively small whereas the difference between the low level of the external input signal and the logic threshold voltage is made large. As a result, both the response time of the inside ECL circuit when the external input signal is changed from the high level to the low level and the response time of the inside ECL circuit when the external input signal is changed from the low level to the high level are varied. Moreover, since the difference between the high level of the external input signal and the threshold voltage of the inside ECL circuit is so small, the noise margin of the circuit device is reduced. This problem concerning the noise margin is considered serious because generally relatively high noises are imparted to the outside wirings through which the external input signal is fed.

The input circuit is allowed to solve that problem by having its threshold voltage set at a proper level. However, this input

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circuit itself establishes a relatively large signal delay. It becomes accordingly difficult to shorten the response time of the integrated circuit device as a whole.

5 In order to solve the new problem which is invited by the provision of the input circuit, we, the Inventors, have examined the inside ECL circuit which has such a relatively low logic threshold voltage that the external input
10 signal may be fed to the minor amplitude inside ECL circuit.

 In this case, however, the number of the circuit elements in each minor amplitude inside ECL circuit is increased, as will be
15 explained in the following, so that the integration of the integrated circuit is deteriorated.

 Especially in a large scale integration device having several thousand gates of the ECLs in one chip, the deterioration in the
20 integration leads to remarkable increase in the occupied area on the chip thereby producing a remarkable disadvantage.

 Fig. 1 is a block diagram showing, by two-dotted chain lines, an ECL integrated circuit
25 (i.e., ECL LSI) which is constructed without

incorporating any especial input circuit. In addition to minor amplitude ECL circuits ECL_1 to ECL_n , there are provided output circuits OB_1 to OB_l for enlarging the logic amplitudes of the inside ECL circuits to a normal logic amplitude. As the minor amplitude inside ECL circuits, one might use a circuit which is shown in Fig. 2A. In this circuit, the ratios R_{CN}/R_E and R_{CO}/R_E of a pair of load resistances, which are connected to the respective collectors of paired differential transistors Q_3 and Q_4 constructing the ECL circuit to a constant-current resistance R_E connected to the common emitter of the paired differential transistors are set at lower level than those of the case of the normal ECL circuit.

By those settings of the resistance ratios, the constant current which flows through the aforementioned collector resistance R_{CN} or R_{CO} is set at a relatively low level. As a result, the voltage drop at the load resistance R_{CN} or R_{CO} by the aforementioned constant current is relatively reduced so that an output signal V_{out} has its lower logic level shifted higher. As a result, the output signal V_{out} or $\overline{V_{out}}$

can have its amplitude made smaller than that of an input signal V_{in} .

Moreover, the circuit under consideration is especially provided with a level shifting resistance R_l . This level shifting resistance R_l is required, as will be described hereinafter, for making the center level of the minor amplitude output signal V_{out} substantially equal to that of the normal amplitude input signal V_{in} .

Fig. 2B is a diagram illustrating the input/output transmitting characteristics of the ECL circuit of Fig. 2A.

An input/output transmission characteristic curve V_{co} indicates the relationship between the normal amplitude input signal V_{in} and the collector voltage V_{co} of the transistor Q_4 .

An input/output transmission characteristic curve V_{co}' indicates that in the case without the level shifting resistance R_l the collector voltage V_{co} of the aforementioned transistor Q_4 is shifted to the high level side until it takes the value V_{co}' .

An input/output transmission characteristic curve V_{out}' indicates the relationship between the normal amplitude input signal V_{in} and the

minor amplitude output signal V_{out} .

The input/out transmission characteristic curve V_{out}' indicates that in the case without the level shifting resistance R_L the minor amplitude
5 output signal V_{out} is shifted to the high level side until it takes the value V_{out}' .

Thanks to the provision of the level shifting resistance R_L in that way, the output signal of the ECL circuit can be shifted to
10 the low level side by the voltage drop (e.g., 0.1 V) at that resistance R_L .

For example, the minor amplitude output signal V_{out} has its high output level shifted from $V_{out}(H)'$ (- 0.9 V) to $V_{out}(H)$ (- 1.0V)
15 and its low output level from $V_{out}(L)'$ (- 1.5 V) to $V_{out}(L)$ (- 1.6 V).

As a result, the center level V_{tho} of the output signal V_{out} can be deduced from the following Equation (1):

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$$\begin{aligned} V_{tho} &= (V_{out}(H) + V_{out}(L))/2 \\ &= \{(- 1.0) + (- 1.6)\}/2 \\ &= - 1.3 (V) \text{ - - - - - (1).} \end{aligned}$$

Thus, the minor amplitude output signal
25 V_{out} can have its center level V_{tho} (- 1.3) made

substantially equal to the center level V_{thi}
(i.e., a logic threshold voltage: e.g., - 1.32 V)
of the normal amplitude input signal V_{in} .

In this case, however, there arises a defect
5 in that the integration of the integrated circuit
is lowered because each minor amplitude inside
ECL circuit requires a level shifting resistance
 R_l , as has been described in the above.

From the viewpoint of lowering the power
10 consumption, moreover, a disadvantage arises because
useless power is consumed by the aforementioned
level shifting resistance R_l .

In the ECL integrated circuit device
(ECL LSI) having a lower internal logic amplitude
15 than an external logic amplitude, as has been
described hereinbefore, an especial input circuit
for receiving the input signal of the former
is required separately of the minor amplitude
inside ECL circuit.

20 Now, the experiments of the Inventors
have revealed that the transmission delay time
of that input circuit is innegligibly high in
comparison with the time required for the logic
operations in the ECL LSI. The operating speed
25 of this ECL LSI as a whole is considerably restricted.

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For example, where the input circuit is constructed of the normal ECL circuit, as has been described in the foregoing Japanese Patent Laid-Open No. 134780 / 1975, its transmission delay time is about 0.3 nano secs.

On the other hand, the transmission delay time of the minor amplitude inside ECL circuit for one gate is about 0.35 to 0.8 nanosecs. About four gates are connected in cascade to perform one logic operation. Therefore, the time necessary for the logic operation inside of the LSI is about 1.4 (i.e., $0.35 \times 4 = 1.4$) nanosecs at the minimum.

In the worst case, therefore, the time (e.g., 0.3 nanosecs) required by the input circuit reaches a value as high as 21 ($0.3/1.4 \approx 0.21$) % of the time (e.g., 1.4 nanosecs) necessary for the actual logic operation.

Therefore, the reduction in the transmission delay time of that input circuit is indispensable for the improvement in the operating speed of the ECL LSI as a whole.

It is, therefore, desirable to provide an ECL semiconductor integrated circuit device which is intended to have its operating speed improved.

It is also desirable to provide an input circuit having a high speed.

An ECL semiconductor integrated circuit device according to the present invention has
5 its input circuit including a first transistor having its base fed with an input signal, a second transistor coupled to said first transistor for current switching operations therewith, a load element connected with the collector
10 of said second transistor, and a bias circuit for generating a bias voltage, which is to be fed to the base of said second transistor, in response to the collector output of said second transistor. In accordance with this construction,
15 the capacity between the collector and base of the aforementioned second transistor can be substantially neglected. As a result, the operating speed (i.e., the transmission delay time) is improved.

20 In the accompanying drawings:

Fig. 1 is a block diagram showing the ECL integrated circuit device which has been conceived prior to the present invention;

Fig. 2A is a circuit diagram showing
5 one example of the inside ECL circuit of that circuit device;

Fig. 2B is a diagram showing the input/output transmission characteristics of that inside ECL circuit;

10 Fig. 3 is a block diagram showing a semiconductor integrated circuit device according to one embodiment of the present invention;

Fig. 4A is a circuit diagram showing one specific embodiment of the circuit device;

15 Fig. 4B is a diagram showing the input/output transmission characteristics of the input circuit of Fig. 4A;

Fig. 4C is a diagram showing the input/output transmission characteristics of the output
20 circuit of Fig. 4A;

Fig. 5A is a circuit diagram showing another embodiment of the output circuit;

Fig. 5B is a diagram showing the input/output transmission characteristics of the circuit
25 of Fig. 5A; and

Figs. 6 to 9 are circuit diagrams showing other embodiments of the input circuit.

5 The present invention will be described in detail in the following in connection with the embodiments thereof.

Fig. 3 is a block diagram showing one embodiment of the ECL semiconductor integrated
10 circuit device according to the present invention.

In this Figure, the portion ECL LSI, which is enclosed by two-dotted chain lines, is formed on a single semiconductor substrate by the well-known semiconductor integrated circuit
15 technique.

Terminals T_{in1} to T_{ink} and terminals T_{out1} to T_{outl} are used as the external terminals of that portion ECL LSI. There are also provided power terminals V_{CC} (at 0 V), V_{EE} (at
20 - 4.5 V) and V_{TT} (at - 2.0 V) for supplying the semiconductor integrated circuit device ECL LSI with the supply voltages (although they are not shown).

The aforementioned terminals T_{in1} to
25 T_{ink} are used as external input terminals, which

are to be fed with input signals at the normal ECL level. The input signals to be fed from those terminals T_{in1} to T_{ink} are applied to the input terminals of input circuits IB_1 to IB_k according to the present invention, respectively. These input circuits IB_1 to IB_k generate output signals, which have their logic amplitudes reduced by shifting the low level of the aforementioned normal ECL signal to the high level side while leaving the high level of the same signal as it is, and transmit those output signals to the predetermined input terminals of minor amplitude inside ECL circuits ECL_1' to ECL_n' .

These minor amplitude inside ECL circuits ECL_1' to ECL_n' are operated by a logic threshold voltage V_{th}' according to that center value of the internal ECL signal, which has its level converted into the minor amplitude by those input circuits IB_1 to IB_k .

Moreover, the circuit for generating the signal to be fed out of that ECL LSI is constructed of the output circuits OB_1 to OB_l . These output circuits OB_1 to OB_l perform the predetermined logic operations in response to the aforementioned minor amplitude internal

ECL signal and amplifies and converts that signal into the aforementioned normal ECL signal level until they feed the converted signal out of external terminals T_{out1} to T_{out2} .

5 Fig. 4A shows the circuit diagram of one embodiment of the aforementioned input circuit IB_1 , minor amplitude inside ECL circuit ECL_1 and output circuit OB_1 .

 The input circuit IB_1 according to the
10 present invention is constructed of a differential transistor circuit of negative feedback type so as to especially speed up the operation thereof.

 The constant current resistance R_E is connected between the common emitter of differential
15 transistors Q_{10} and Q_{11} and the power terminal V_{EE} . The collector resistors R_{CN} and R_{CO} are connected between the collectors of those transistors Q_{10} and Q_{11} and the power terminal V_{CC} , respectively.

20 The aforementioned transistor Q_{10} is used as an input transistor and has its base connected with the external terminal T_{in1} .

 On the other hand, the aforementioned transistor Q_{11} is used as a reverse input tran-
25 sistor and has its collector output voltage

V_{CC} transmitted to the base of an emitter follower transistor Q_{12} . Dividing resistances R_1 and R_2 are connected between the emitter of that transistor Q_{12} and the power terminal V_{TT} . The
 5 output voltage V_{out1} obtained from the emitter of the aforementioned transistor Q_{12} is divided by the aforementioned dividing resistances R_1 and R_2 , and the divided voltages are fed back to the base of the aforementioned reverse input
 10 transistor Q_{11} .

The relationship between the collector output voltage V_{CC} of the reverse input transistor Q_{11} and a voltage V_{F1} to be fed back to the base of the same is expressed by the following
 15 Equations (2) and (3):

$$\begin{aligned}
 V_{F1} &= V_{OUT1} - \frac{R_1}{R_1 + R_2} (V_{OUT1} - V_{TT}) \\
 &= V_{OUT1} \left(1 - \frac{R_1}{R_1 + R_2} \right) + \frac{R_1}{R_1 + R_2} \cdot V_{TT} \\
 &= \frac{R_2}{R_1 + R_2} \cdot V_{OUT1} + \frac{R_1}{R_1 + R_2} \cdot V_{TT} \\
 &= \frac{R_2}{R_1 + R_2} (V_{CC} - V_{BE}) + \frac{R_1}{R_1 + R_2} \cdot V_{TT} \dots (2)
 \end{aligned}$$

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$$\therefore \Delta V_{F1} = \Delta V_{CO} \frac{R_2}{R_1 + R_2} \dots (3)$$

As is apparent from the Equation

(3) the ratio (i.e., the feedback ratio) $\Delta V_{F1} / \Delta V_{CO}$ of the change ΔV_{F1} of the base feedback voltage V_{F1} to the change ΔV_{CO} of the collector output voltage V_{CO} of the transistor Q_{11} can be controlled by the divided voltage ratio $R_2 / (R_1 + R_2)$ of the emitter follower transistor Q_{12} by the emitter dividing resistances R_1 and R_2 .

As a result, it is possible to prevent a difficulty resulting from the feedback ratio being excessively high. More specifically, it is possible to prevent the difficulty that when the input voltage V_{in1} applied to the base of the input transistor Q_{10} is at the high or low level the voltage difference $|V_{in1} - V_{F1}|$ between that input voltage V_{in1} and the base feedback voltage V_{F1} of the reverse input transistor Q_{11} is not so sufficient that the switching operations of the paired differential transistors Q_{10} and Q_{11} are not completely effected so that the output voltage V_{CO} is unstable or incapable of acquiring a desired level.

The input circuits IB_1 to IB_k according to the present invention use the differential transistor circuits of negative feedback type, as has been described hereinbefore. To the
5 base of the reverse input transistor Q_{11} , more specifically, there is not applied a fixed reference voltage but the voltage which corresponds to the collector output voltage V_{CO} of the reverse input transistor Q_{11} .

10 As a result, as illustrated in the input/output transmission characteristic diagram of Fig. 4B, the voltage difference $|V_{CO} - V_{F1}|$ between the base and collector of the reverse input transistor Q_{11} is held at a substantially constant
15 level. Therefore, the parasitic capacity C_C between the base and collector of that transistor Q_{11} can be equivalently neglected. As a result, it is unnecessary to charge or discharge that parasitic capacity when the collector voltage
20 V_{CO} rises or breaks.

Thus, it is possible to shorten the transmission delay time, i.e., the time from when the input signal V_{in1} rises (or breaks) to when the output signal V_{out} accordingly rises
25 (or breaks).

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A high effect is obtained especially considering the fact that the capacity which can be neglected may be the relatively high parasitic capacity of a bipolar transistor.

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According to the experiments of the Inventors, the input circuit IB_1 of the present embodiment has a transmission delay time of about 0.1 nanosecs. When the normal
10 ECL circuit (having its reference voltage fixed) is used as that input circuit, the transmission delay time is about 0.3 nanosecs, as has been described hereinbefore. Thus, by applying the present circuit,
15 the time required in the input circuit is shortened to one third of the prior art.

Thanks to the provision of the negative feedback loop, moreover, that input circuit has another advantage that it can stand
20 disturbances such as fluctuations in the power source or the dispersion of the element characteristics, in other words, that it is hardly subjected to those influences.

In case, still moreover, the input voltage
25 V_{in1} to be applied to the base of the input

transistor Q_{10} takes the center value V_{th} between the high level $V_{inl}(H)$ and the low level $V_{inl}(L)$, the output voltage V_{outl} can be set at the center value V_{th} between the high level $V_{outl}(H)$ and the low level $V_{outl}(L)$. The effect obtained from satisfying that relationship is as follows:

When the input voltage V_{inl} is at the low (or high) level side from the center value V_{th} between its high level $V_{inl}(H)$ and low level $V_{inl}(L)$, the output voltage V_{outl} is likewise shifted to the low (or high) level side from the center value V_{th} between its high level $V_{outl}(H)$ and low level $V_{outl}(L)$. As a result, the signal to be judged to be at the low (or high) level side from the standpoint of the input side is prevented from being misjudged as being at the high (or low) level side from the standpoint of the output side. In short, the noise margin can be made proper so that malfunctions due to noises can be reduced.

Although not limitative, the signal level conversion (i.e., to the minor amplitude) at the aforementioned input circuit IB_1 is so set as is illustrated in the input/output transmission characteristic diagram of Fig. 4B.

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The external ECL signal V_{in1} has a high level $V_{in1}(H)$ of -0.9 V, a low level $V_{in1}(L)$ of -1.75 V and a center value of about -1.32 V. In response to that signal V_{in1} , as shown in 5 thick solid line in the same Figure, there is generated the output signal V_{out1} which has such a minor amplitude such that its center value (i.e., the internal logic threshold voltage V_{th}') is -1.2 V, such that its high level $V_{out1}(H)$ 10 is -0.9 V and such that its low level $V_{out1}(L)$ is -1.5 V.

In the same Figure, the difference in the gradients between the the characteristic curves of the base feedback voltage V_{F1} of the 15 reverse input transistor, as shown in a thin solid line, and the aforementioned output voltage V_{out1} , as indicated in the thick solid line, is determined by the aforementioned dividing resistance ratio $R_2/(R_1 + R_2)$.

20 The signal V_{out1} having had its level converted by the aforementioned input circuit IB_1 is transmitted to the input terminal T_1 of the inside ECL circuit ECL_1 .

The construction of this inside ECL circuit 25 ECL_1 is similar to that of the well-known ECL

circuit except the following points so that its explanation is omitted here.

This inside ECL circuit ECL_1 receives a signal which has its amplitude made minor by the aforementioned input circuit. The circuit according to the embodiment under consideration has its output signal amplitude and signal level made coincident with those of the aforementioned minor amplitude signal V_{out1} by making the ratios R_{CN}/R_E and R_{CO}/R_E of the paired load resistances R_{CN} and R_{CO} , which are connected to the respective collectors of paired differential transistors Q_{15} and Q_{16} constructing the ECL logic block, to the constant current resistance R_E , which is connected with the common emitter of the aforementioned paired differential transistors Q_{15} and Q_{16} , rather smaller than those of the normal ECL circuit.

In accordance with this, the logic threshold voltage V_{th} is set at the center value (i.e., - 1.2 V) of the aforementioned minor amplitude signal V_{out1} , which is different from the logic threshold voltage V_{th} (e.g., about - 1.32 V) of the aforementioned external ECL signal. The output signals of the Inside ECL circuits ECL_1

to ECL_n have their amplitudes made minor by shifting the low level of the external ECL signal V_{in1} or the like to the high level side while leaving the high level (i.e., - 0.9 V) of the same as it is. Thus, the inside ECL circuits ECL_1 to ECL_n need not be provided with the level shifting resistance R_l , as shown in Fig. 2A.

Moreover, the output circuit OB_1 for generating the normal ECL signal to be fed out of the LSI is constructed of an ECL circuit which has an additional function to enlarge the amplitude of the internal ECL signal V_{in2} to that of the external ECL signal V_{out2} .

This output circuit OB_1 is operated by the internal logic threshold voltage V_{th} because it receives the aforementioned minor amplitude internal ECL signal.

Still moreover, in order that the center value and the low level of that output signal V_{out2} may be shifted (or enlarged) to the low level side, as illustrated in Fig. 4C, the ratios $(R_{CN1} + R_{CN2})/R_E'$ and $(R_{CO1} + R_{CO2})/R_E'$ of the collector load resistances $(R_{CN1} + R_{CN2})$ and $(R_{CO1} + R_{CO2})$ of paired differential transistors Q_{22} and Q_{23} to the constant current resistance

R_E' which is connected to the common emitter of those transistors are set at relatively high levels, as compared with those of the normal ECL circuit.

5 Incidentally, the reason why the collector load resistances are respectively divided into R_{CN1} and R_{CN2} , and R_{CO1} and R_{CO2} is to enable the use of the divided voltages, which are generated by those dividing resistances, as signals for
10 the inside ECL circuits. The divided voltages thus generated are applied to the bases of emitter follower transistors Q_{24} and Q_{25} , respectively, from which the minor amplitude signals $\overline{V_{out2}}$ and V_{out2}' for the inside ECL circuits are obtained at
15 the emitter output terminals T_9 and T_{10} of those transistors Q_{24} and Q_{25} . That signal V_{out2}' is illustrated in a thin solid line in Fig. 4C.

 The semiconductor integrated circuit (ECL LSI) thus far described uses the differential
20 transistor circuits of negative feedback type as its input circuits IB_1 to IB_k so that its fabrication speed can be remarkably improved.

 More specifically, the time from when the input signal is applied to the input circuit
25 of that ECL LSI to when the signal corresponding

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to that input signal is applied to the output circuit of the same is about 1.5 (0.1 + 1.4 = 1.5) nanosecs, as has been described hereinbefore.

5 In the case of the prior art circuit, on the other hand, the time corresponding to the aforementioned one is about 1.7 (0.3 + 1.4 = 1.7) nanosecs, as has also been described.

As a result, the operating speed of the
10 ECL LSI can be improved by at least about 12% ((1.7 - 1.5)/1.7 $\approx$ 0.12).

Thanks to the provisions of the input circuits IB_1 to IB_k , furthermore, the signal amplitude is reduced by shifting the center
15 value V_{th} and the low level $V_{inl}(L)$ of the external ECL signal to the high level side while leaving the high level $V_{inl}(H)$ the same as it is. As a result, the minor amplitude internal ECL circuits ECL_1 to ECL_n can generate the output
20 signals, which are coincident with the aforementioned minor amplitude internal ECL signals, without any provision of the level shifting resistance R_l . Thus, it is possible to realize the remarkable improvement in the integration
25 because the level shifting resistance R_l for

each of the numeral ECL gate circuits can be eliminated.

Furthermore, the power consumption can also be reduced by reducing the useless power which has been consumed by the level shifting resistors R_l . Incidentally, it goes without saying that the inside ECL circuits can realize the speed-up of the operations by reducing their signal amplitudes.

10 In the inside ECL circuits, incidentally, the circuit of the present embodiment can have its power consumption reduced by the elimination of the aforementioned level shifting resistances R_l . If the power consumption is made similar
15 to that when the aforementioned resistances R_l are provided, however, the operating current of each inside ECL circuit can be increased. As a result, if the power consumption is made equal to that in case the level shifting resistances
20 R_l are provided, the operating speed of the inside ECL circuit can be further accelerated.

Fig. 5A is a circuit diagram showing another example of the output circuit.

In this embodiment, the output circuit
25 is intended to have its operation speeded up

by adopting the differential transistor circuit of negative feedback type similarly to the input circuit IB_1 .

In the present embodiment, specifically,
5 a feedback voltage V_{F2} is applied to the base of the reverse input transistor Q_{23} , as is different from the output circuit OB_1 of Fig. 4A, which is operated by the fixed reference voltage V_{th}' . The dividing resistances R_{CO1} and R_{CO2} are connected
10 with the collector of the reverse input transistor Q_{23} . Moreover, the divided voltage V_{CO1} prepared by those dividing resistances is applied to the base of an emitter follower transistor Q_{25}' . Dividing resistances R_1' and R_2' are
15 connected between the emitter of that transistor Q_{25}' and the power terminal V_{TT} . The emitter output voltage V_{CO1}' of that emitter follower transistor Q_{25}' is divided by the dividing resistances R_1' and R_2' and is applied as the
20 feedback voltage V_{F2} to the base of the reverse input transistor Q_{23} .

Incidentally, that normal amplitude output signal V_{out3} for the outside ECL circuit, which is to be fed out of the external terminal T_{out1}' ,
25 is generated through an emitter follower transistor

Q_{26} which is made receptive of the collector voltage V_{CO2} of the aforementioned reverse input transistor Q_{23} .

The circuit of this embodiment can have
5 its output signal V_{out3} converted into the normal ECL signal by suitably setting the aforementioned respective dividing resistance ratios.

Specifically, in order that the output signal V_{out3} may be the normal ECL signal, as
10 illustrated in the input/output transmission characteristic diagram of Fig. 5B, the center value and the low level are shifted to the low level side while leaving the high level as it is. This reduction in the level can be controlled,
15 as will be described hereinafter, by the resistance ratios of the collector load resistances R_{CO1} and R_{CO2} of the reverse input transistor Q_{23} to the resistances R_1' and R_2' .

The relationship between the collector
20 voltage V_{CO2} of the reverse input transistor Q_{23} and the feedback voltage V_{F2} fed to the base of the same is expressed by the following Equations (4) to (7).

$$V_{CO1} = \frac{R_{CO1}}{R_{CO1} + R_{CO2}} \cdot V_{CO2} \quad - - (4)$$

$$V_{CO1}' = V_{CO1} - V_{BE}$$

$$= \frac{R_{CO1}}{R_{CO1} + R_{CO2}} V_{CO2} - V_{BE} \quad - - (5)$$

$$V_{F2} = V_{CO1}' - \frac{R_1'}{R_1' + R_2'} (V_{CO1}' - V_{TT})$$

$$5 \quad = V_{CO1}' \left(1 - \frac{R_1'}{R_1' + R_2'} \right) + \frac{R_1'}{R_1' + R_2'} \cdot V_{TT}$$

$$= \frac{R_2'}{R_1' + R_2'} \cdot V_{CO1}' + \frac{R_1'}{R_1' + R_2'} \cdot V_{TT}$$

$$= \frac{R_2'}{R_1' + R_2'} \left(\frac{R_{CO1}}{R_{CO1} + R_{CO2}} \cdot V_{CO2} - V_{BE} \right)$$

$$- \frac{R_1'}{R_1' + R_2'} \cdot V_{TT}$$

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$$= \frac{R_2'}{R_1' + R_2'} \cdot \frac{R_{CO1}}{R_{CO1} + R_{CO2}} \cdot V_{CO2} - \frac{R_2'}{R_1' + R_2'} \cdot V_{BE} + \frac{R_1'}{R_1' + R_2'} \cdot V_{TT} \dots \dots \dots (6)$$

$$\therefore \Delta V_{F2} = \Delta V_{CO2} \cdot \frac{R_2'}{R_1' + R_2'} \cdot \frac{R_{CO1}}{R_{CO1} + R_{CO2}} \dots \dots \dots (7)$$

From the Equation (7), it is apparent
 5 that the ratio (i.e., the feedback ratio) $\Delta V_{F2}/\Delta V_{CO2}$ of
 the change ΔV_{F2} in the base feedback voltage
 V_{F2} to the change ΔV_{CO2} in the collector output
 voltage V_{CO2} of the reverse input transistor
 Q_{23} can be controlled by both the voltage dividing
 10 ratio $R_2'/(R_1' + R_2')$ of the emitter resistances
 R_1' and R_2' of the emitter follower transistor
 Q_{25} and the voltage dividing ratio $R_{CO1}/(R_{CO1}$
 $+ R_{CO2})$ of the collector load resistances R_{CO1}
 and R_{CO2} . As a result, it is possible to prevent
 15 the aforementioned difficulty that the feedback
 ratio is excessively high.

As illustrated in Fig. 5B, moreover,
if the voltage of the minor amplitude inside
ECL signal to be applied to the base of an input
transistor Q_{20} or the like is at the center value
5 (i.e., the logic threshold voltage) between the
high level $V_{in3}(H)$ and the low level $V_{in3}(L)$,
the output voltage V_{out3} can be set at the center
value V_{th} between its high level $V_{out3}(H)$ and
low level $V_{out3}(L)$. The effect obtainable from
10 result of satisfying the above-relationship is
similar to the case of the aforementioned input
circuit IB_1 .

On the other hand, the output circuit
 OB'_1 of the present embodiment has its reverse
15 input transistor Q_{23} fed at its base with the
feedback voltage V_{F2} illustrated in Fig. 5B,
as is different from the case in which the reverse
input transistor Q_{23} has its base fed with the
fixed reference voltage V_{th}' , as in the output
20 circuit OB_1 of Fig. 4A. As a result, the varying
range of the voltage difference $|V_{CO2} - V_{F2}|$
between the base and collector of the reverse
input transistor Q_{23} can be reduced. As a result,
since the value of the parasitic capacity C_C
25 between the base and collector of the aforemen-

tioned transistor Q_{23} can be apparently reduced, the rising and breaking speeds of the collector output signal V_{CO2} , accordingly, of the output signal V_{out3} can be accelerated so that the signal transmission delay time at the output circuit OB_1' can be shortened.

As a result, if the output circuit OB_1' of the present embodiment is used in place of the output circuit OB_1 of Fig. 4, those speeds can be further accelerated. Likewise the aforementioned input circuit, moreover, there can be attained another advantage that the circuit of the present embodiment is less influenced by disturbances such as fluctuations in the power source and dispersions in the element characteristics.

As the output circuit, there can be prepared the circuit elements as of the output circuit OB_1 of Fig. 4A, and the connections inbetween can be changed by a master slice system in accordance with the applications. In other words, if the minor amplitude inside ECL signal is to be generated by the output circuit, the circuit elements are so connected as to constitute the output circuit OB_1 shown in Fig. 4A. If,

on the other hand, it is unnecessary to generate the aforementioned minor amplitude inside ECL signal, the high-speed output circuit OB_1' shown in Fig. 5A can be constituted by changing the
5 connections by the master slice system.

To the output circuit OB_1' of Fig. 5A, furthermore, there may be added an emitter follower circuit for generating the minor amplitude inside ECL signal.

10 The present invention should not be limited to the embodiments thus far described.

For example, in the input circuit of Fig. 4A, the collector resistance R_{CN} of the input transistor Q_{10} may be omitted if it is necessary
15 to reduce the number of the circuit elements.

However, it is desired to provide the resistance R_{CN} by the following reasoning.

Specifically, the resistance R_{CN} applies a signal voltage at a suitable level to the collector
20 of the transistor Q_{10} thereby to establish a suitable mirror capacity in the transistor Q_{10} . Thanks to the fact that the transistor Q_{10} has an input capacity corresponding to the mirror capacity, the high-frequency noises which might
25 otherwise be imparted to the input terminal can

be attenuated to an excellent extent. As a result, the circuit can be made substantially insensitive to the noises without having its operating speed substantially decelerated.

5 If the resistor R_{cn} is provided, it is sufficient to generate the inside ECL signal which has been reversed through the emitter follower circuit made receptive of the collector output signal of that transistor Q_{10} .

10 Moreover, the inside ECL circuit may be modified such that a constant-current transistor is connected with the common emitter of the paired differential transistors constructing the ECL circuit.

15 Still moreover, the center value and the low level of the minor amplitude inside ECL signal may be shifted to the higher level side in accordance with the operating margin of the inside ECL circuit thereby to have its
20 amplitude further reduced.

On the other hand, the output circuit OB_1 of Fig. 5A may be used in the output circuit of the ECL integrated circuit device of Fig.

1 so that its high-speed operation can be realized.

25 Figs. 6 to 9 show other embodiments of

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the input circuit according to the principle of the present invention.

The circuit shown in Fig. 6 is modified from the input circuit of Fig. 4A such that

5 the dividing resistances R_1 and R_2 are replaced by a resistance R_{10} and a constant-current source I_1 . This source per se is well known in the art. The constant-current source I_0 in the input circuit is constructed similarly to that in

10 the prior art ECL circuit. Specifically, the constant-current source I_0 is constructed of a constant-current transistor which has its collector connected with the common emitter of the transistors Q_{10} and Q_{11} and its emitter

15 connected with a power terminal through a resistance having a suitable value. The base of the constant-current transistor is fed with the reference voltage which is generated from a suitable reference voltage generating circuit. A constant-current

20 source I_1 is also made to have a similar construction to that of the foregoing constant-current source.

Since, in this circuit, the current I_1 to flow through the resistance R_{10} is constant

the voltage drop at the resistance R_{10} is held constant at all times.

As a result, the voltage between the base and the collector of the reverse input transistor Q_{11} takes such a substantially complete constant value as is determined by both the constant voltage drop $I_1 R_{10}$ at the aforementioned resistor R_{10} and the emitter-base constant voltage of the emitter-follower transistor Q_{12} .

As a result, this circuit can have its operating speed (i.e., the transmission delay time) further improved because the parasitic capacity between the base and collector of the reverse input transistor Q_{11} is substantially completely neglected.

In this circuit, moreover, the switching operations of the paired differential transistors Q_{10} and Q_{11} can be completely performed in response to the input signal V_{in} by properly setting the aforementioned voltage drop $I_1 R_{10}$ and the respective element constants of the circuit. Furthermore, when the input signal V_{in} is at its center level, the output signal V_{out} can be set at that center level.

The circuit shown in Fig. 7 is modified

such that the constant-current source I_1 of the input circuit shown in Fig. 6 is replaced by a specific circuit.

In this circuit, specifically, the aforementioned constant-current source I_1 is constructed of a constant-current transistor Q_{27} and an emitter resistance of the latter. A suitable reference voltage V_R is fed to the base of the aforementioned constant-current transistor Q_{27} .

The input circuit shown in Fig. 8 is modified such that the a resistance R_{17} can be connected in parallel with the voltage dividing resistances R_1 and R_2 of the input circuit shown in Fig. 4A.

The resistance R_{17} is connected in parallel with the dividing resistances R_1 and R_2 , if desired, by the master slice system, for example.

Thanks to the aforementioned connection of the resistance R_{17} , the emitter-follower transistor Q_{12} can have its composite emitter resistance reduced so that its driving capacity can be improved.

As a result, this input circuit can be prevented from having its operating speed decreased

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even if it drives a relatively high load.

The input circuit shown in Fig. 9 is modified such that there is disposed in the input circuit of Fig. 4A an emitter-follower transistor Q_{28} which is made receptive of the collector output signal of the input transistor Q_{10} thereof.

This circuit is enabled to generate the minor amplitude signals V_{out} and $\overline{V_{out}}$ having opposite phases in response to the input signal V_{in} .

Incidentally, a pair of input transistors may be disposed in the input circuit, as shown in Fig. 9.

15 These plural input transistors Q_{10} and Q_{10}' have their collectors and emitters commonly connected with each other and their bases fed with input signals V_{in} and V_{in}' . Thanks to the provision of such plural input transistors,
20 the input circuit can be given a logic function.



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CLAIMS:

1. A semiconductor integrated circuit device comprising:

5 an input terminal:

an input circuit including a first transistor having its base fed with an input signal through said input terminal, a second transistor coupled to said first transistor for current

10 switching operations with said first transistor, a load element connected with the collector of said second transistor, and a bias circuit which receives the collector output of said second transistor and generates a bias voltage in accordance
15 therewith which is fed to the base of said second transistor, so that said input circuit may generate an output signal which has its high level substantially equal to that of said input signal and its low level higher than that of said input signal;

20 and

an ECL circuit for receiving said input signal through said input circuit.

2. A semiconductor integrated circuit device

25 according to Claim 1, wherein said ECL circuit



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includes: a third transistor having a collector,
an emitter and a base adapted to be fed with
said input signal; and a fourth transistor having
a collector, an emitter coupled to the emitter
5 of said third transistor, and a base adapted
to be fed with a threshold voltage which is at a higher
level than such a threshold voltage as would recognize the high
and low levels of the input signal which the input circuit
is adapted to receive from said input terminal.

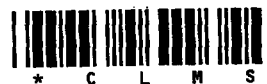
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3. A semiconductor integrated circuit device
according to Claim 1 or 2, wherein said bias circuit
has a level shift element connected between
the collector and base of said second transistor.

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4. A semiconductor integrated circuit device
according to Claim 1 or 2, wherein said input circuit
further includes an emitter follower transistor
having a base coupled to the collector of said
20 second transistor, an emitter coupled to the
base of said third transistor, and a collector,
and wherein said bias circuit is formed
by a level shift circuit which receives the
emitter output of said emitter follower tran-
25 sistor and generates a voltage to be fed to

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the base of said second transistor.

5. A semiconductor integrated circuit device according to Claim 4, wherein said level shift
5 circuit has a first resistance element connected between the emitter of said emitter follower transistor and the base of said second transistor, and a second resistance element connected between the base of said second transistor and
10 one terminal of a power source.

6. A semiconductor integrated circuit device according to Claim 4, wherein a collector load resistance element is connected between the
15 collector of said first transistor and the other terminal of said power source.

7. A semiconductor integrated circuit device according to any one of the preceding claims, further comprising:
20 an output circuit which receives the output signal of said ECL circuit and generates an output signal which has its high and low levels made substantially equal to those of said input signal, respectively; and
25 an output terminal adapted to be fed with



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the output signal of said output circuit.

8. A semiconductor integrated circuit device according to Claim 7, wherein said output circuit
5 includes a fifth transistor for current switching operations, a level shift element coupled to the collector of said fifth transistor, and a collector load resistance element coupled between said level shift element and a power supply
10 terminal, and means for generating a signal which is fed to said ECL circuit from the common connection between said collector load resistance element and said level shift element.

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9. A semiconductor integrated circuit device according to Claim 8, wherein the level shift element of said output circuit is made of a resistance element.

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10. A semiconductor integrated circuit device according to Claim 8 or 9, wherein said output circuit further includes: a first emitter follower transistor having a base coupled to the collector
25 of said fifth transistor and an emitter coupled

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to an outside terminal; and a second emitter follower transistor having a base coupled between said collector load resistance element and said level shift element and an emitter to be coupled to
5 an input node of said ECL circuit.

11. A semiconductor integrated circuit device comprising:

- an input terminal;
- 10 an ECL circuit for generating an output signal which has its high level made substantially equal to that of an input signal to be fed to said input terminal and its low level made higher than that of said input signal;
- 15 an output circuit including a first current switch transistor adapted to be controlled by the output signal of said ECL circuit, a level shift element coupled to the collector of said first current switch transistor, and a resistance element
20 connected between said level shift element and a terminal of a power source; and
an output terminal adapted to be fed with the output signal which is generated at the common connection between the collector
25 of said first current switch transistor and said level shift element.



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12. A semiconductor integrated circuit device substantially as any described herein with reference to Figs. 3 to 9 of the accompanying drawings.
