manufacturing (D. Lederer and J.-P. Raskin, "RF performance of a commercial SOI technology transferred onto a passivated HR silicon substrate," IEEE Transaction on Electron Devices, July 2008). Suppression effect in all of these methods is based on enhanced trapping of charge carriers within the implanted or polysilicon layer on a top of the HRS substrate.

However, all these methods induce additional cost effects, and they pose limitations in HRS-based device processes. These issues have limited the viability of these methods.

Summary

Embodiments of the invention provide a high-resistivity silicon substrate with reduced radio frequency signal losses and, consequenty, higher performance for a radio frequency integrated passive devices build on the substrate.

Embodiments of the invention are fulfilled by providing a high-resistivity silicon substrate, a method, and a radio frequency integrated passive device as defined below.

According to a first aspect of the present invention, there is provided a high-resistivity silicon substrate with a reduced radio frequency loss for a radio frequency integrated passive device, comprising a bulk zone comprising high-resistivity bulk silicon and a preserved sub-surface lattice damage zone, which is processed into a front side of the substrate, wherein the substrate is a silicon wafer and wherein the lattice damage zone comprises fractured silicon above the bulk zone, characterized in that the lattice damage zone forms a front surface of the wafer, wherein the front side is a chemical-mechanical planarization-polished front surface, wherein the lattice damage zone is a thinned lattice-damage zone, and wherein the lattice damage zone is configured to suppress a parasitic surface conduction in order to achieve the RF loss reduction of the substrate.

The term "surface passivation" refers to e.g. a treatment given to a surface of a silicon wafer for inhibiting parasitic surface conduction-enabled stray current generation under an RF excitation.

The term "high-resistivity silicon" refers to semiconductor grade silicon crystal, which has an exceptionally high resistivity, e.g. typically above 100 Ohm-cm or more. Standard silicon resistivities range from below 1 up to 10-20 Ohm-cm.

The term "radio frequency integrated passive device" refers to passive components, e.g. conductors, inductors, notch filters, bulk acoustic wave (BAW) filters, thin film bulk acoustiv wave resonators (FBAR), and other types of filters, which have been integrated on a suitable platform, e.g. on a high resistivity silicon.

According to a second aspect of the present invention, there is provided a method for manufacturing the above high-resistivity silicon substrate with the reduced radio frequency loss for a radio frequency integrated passive device, comprising growing a high-resistivity silicon, processing the grown silicon by slicing a silicon wafer from the grown silicon and by thinning the sliced silicon wafer, wherein the processing achieves a lattice damage zone comprising fractured silicon into a processed silicon wafer, chemical-mechanical planarization-polishing the processed silicon wafer for obtaining the substrate, which comprises a bulk zone comprising high-resistivity bulk silicon, and preserving, by the chemical-mechanical planarization-polishing, at least a part of the lattice damage zone above the bulk zone so that the lattice damage zone forms a chemical-mechanical planarization-polished front surface and comprises fractured silicon above the bulk zone, wherein the substrate is a silicon wafer, wherein the lattice damage zone is a thinned lattice-damage zone, and wherein the lattice damage zone is configured to suppress a parasitic surface conduction in order to achieve the RF loss reduction of the substrate.

According to a third aspect of the present invention, there is provided a radio frequency integrated passive device comprising the above high-resistivity silicon substrate with a reduced radio frequency loss, which substrate comprises a bulk zone comprising high-resistivity bulk silicon and a preserved sub-surface lattice damage zone, which is processed into a front side of the substrate, wherein the substrate is a silicon wafer, wherein the lattice damage zone comprises fractured silicon above the bulk zone, wherein the lattice damage zone forms a front surface of the wafer, wherein the front side is a chemical-mechanical planarization-polished front surface, wherein the lattice damage zone is a thinned lattice-damage zone, and wherein the preserved lattice damage zone is configured to suppress a parasitic surface conduction in order to achieve the RF loss reduction of the substrate.

The verb "to comprise" is used in this document as an open limitation that neither excludes nor requires the existence of also unrecited features. The verbs "to in-clude" and "to have/has" are defined as to comprise.

The terms "a", "an" and "at least one", as used herein, are defined as one or more than one and the term "plurality" is defined as two or more than two.

The term "another", as used herein, is defined as at least a second or more.

The term "or" is generally employed in its sense comprising "and/or" unless the content clearly dictates otherwise.

Claims

1. A high-resistivity silicon substrate with a reduced radio frequency loss for a radio frequency integrated passive device, comprising

a bulk zone comprising high-resistivity bulk silicon and

a preserved sub-surface lattice damage zone, which is processed into a front side of the substrate,

wherein the substrate is a silicon wafer and

wherein the lattice damage zone comprises fractured silicon above the bulk zone,

characterized in that

the lattice damage zone forms a front surface of the wafer,

wherein the front side is a chemical-mechanical planarization-polished front surface,

wherein the lattice damage zone is a thinned lattice-damage zone, and

wherein the lattice damage zone is configured to suppress a parasitic surface conduction in order to achieve the RF loss reduction of the substrate.

2. The substrate of claim 1, wherein the front side is structurally single crystal silicon.

3. The substrate of any of the preceding claims, wherein the preserved lattice damage zone is processed mechanically by slicing, lapping, grinding, brush damaging, laser manipulation, or wet blasting.

4. The substrate of claim 3, wherein the grinding is a rotational fixed abrasive grinding and/or the grinding is executed by a two-step grinding comprising a coarse grinding and a fine grinding.

5. The substrate of any of the preceding claims, which comprises a polysilicon layer on a top of the preserved lattice damage zone.

6. The substrate of claim 5, wherein a thickness of the polysilicon layer is 0,2-8,0 µm.

7. The substrate of claim 5, wherein a thickness of the polysilicon layer is 0,4-6,0 µm.

8. A method for manufacturing the high-resistivity silicon substrate with the reduced radio frequency loss of any of claims 1-7 for a radio frequency integrated passive device, comprising

growing a high-resistivity silicon,

processing the grown silicon by slicing a silicon wafer from the grown silicon and by thinning the sliced silicon wafer,

wherein the processing achieves a lattice damage zone comprising fractured silicon into a processed silicon wafer,

chemical-mechanical planarization-polishing the processed silicon wafer for obtaining the substrate, which comprises a bulk zone comprising high-resistivity bulk silicon, and

preserving, by the chemical-mechanical planarization-polishing, at least a part of the lattice damage zone above the bulk zone so that the lattice damage zone forms a chemical-mechanical planarization-polished front surface and comprises fractured silicon above the bulk zone,

wherein the substrate is a silicon wafer,

wherein the lattice damage zone is a thinned lattice-damage zone, and

wherein the lattice damage zone is configured to suppress a parasitic surface conduction in order to achieve the RF loss reduction of the substrate.

9. A radio frequency integrated passive device comprising the high-resistivity silicon substrate with a reduced radio frequency loss of any of claims 1-7, which substrate comprises

a bulk zone comprising high-resistivity bulk silicon and

a preserved sub-surface lattice damage zone, which is processed into a front side of the substrate,

wherein the substrate is a silicon wafer,

wherein the lattice damage zone comprises fractured silicon above the bulk zone,

wherein the lattice damage zone forms a front surface of the wafer,

wherein the front side is a chemical-mechanical planarization-polished front surface,

wherein the lattice damage zone is a thinned lattice-damage zone, and

wherein the preserved lattice damage zone is configured to suppress a parasitic surface conduction in order to achieve the RF loss reduction of the substrate.