"METHOD OF MAKING A SEMICONDUCTOR DEVICE"

This invention concerns a method of making a semiconductor device.

A method of making a semiconductor device is known which comprises forming a recess in a semiconductor substrate and introducing an insulating film into the recess. The known method is satisfactory if the recess is narrow. Hoswever, if the recess is wide, the insulating film may be provided at the corners only of the recess.

According, therefore, to the present invention, there is provided a method of making a semiconductor device comprising etching a semiconductor substrate to form at least a first recess and a second recess therein, the second recess enclosing a portion of the semiconductor substrate; introducing insulating material into the first and second recesses; and oxidising the said portion of the semiconductor substrate, whereby there is formed in the same semiconductor substrate a relatively narrow element isolating region which is constituted by the insulating material in the first recess and a relatively wide element isolating region which is constituted both by the insulating material in the second recess and by the said oxidised portion.

Preferably, prior to the oxidation of the said portion an anti-oxidation mask is applied over the whole of the semiconductor substrate except for the oxidised portion and an adjacent part of the second recess.

An impurity may be introduced to the base of each of the recesses so as to form a stopper region.

Preferably, the width of the wide element isolating region is several μm.

The said etching is preferably anisotropic etching. Thus the second recess may be formed by forming on said substrate an anti-anisotropic etching film having a recess portion therein, which extends to the substrate so as to expose a portion of the latter, effecting anisotropic etching of the said recess portion, and removing the anti-anisotropic etching film.

The insulating material may be a silicon oxide film.

A polycrystalline silicon film may be introduced into the second recess and is oxidised to form the said silicon oxide film.

Preferably, the polycrystalline silicon film does not completely fill the second recess.

Preferably, after the said silicon oxide film has been formed in the first and second recesses, a further silicon oxide film is formed over the whole substrate so as to contact the silicon oxide film in the first and second recesses, an anti-oxidation mask film being formed on the further silicon oxide film.

The substrate may be a silicon substrate, the further silicon oxide film being formed by thermal oxidation of the silicon substrate.

Insulating material may be introduced into the first recess.

The invention also comprises a semiconductor device comprising semiconductor substrate having at least a first recess and a second recess therein, the second recess enclosing an oxidised portion of the semiconductor substrate, and the first and second recesses containing insulating material, whereby the semiconductor substrate is provided with a relatively narrow element isolating region which is constituted by the insulating material in the first recess and a relatively wide element isolating region which is constituted both by the insulating material in the second recess and by the said oxidised portion.

The invention also comprises a semiconductor device when made by the method described above.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figures 1(a) to (h) illustrate a first embodiment of a method of making a semiconductor device according to the present invention, Figure 1(h) being a section taken on the line A-A' of Figure 2,

Figure 2 is a plan view of the structure, shown in Figure 1(h),

Figures 3(a) to (f) illustrate a second embodiment of a method of making a semiconductor device according to the present invnetion,

Figures 4(a) to (c) illustrate a third embodiment of a method of making a semiconductor device according to the present invention, and

Figures 5(a) to (c) illustrate a known method of making a semiconductor device.

Figures 5(a) to (c) show a method of making a trench type element isolating region of a known semiconductor device.

Firstly,as shown in Figure 5(a), an anti-anisotropic etching film 503 is formed at selected places on a semiconductor substrate 500. The anti-anisotropic etching film 503 is used as a mask for etching. The semiconductor substrate 500 is etched to form recesses 501, 501a having a depth of 7000 Å by anisotropic etching such as reactive ion etching (hereinafter referred to as RIE) using $CBrF_3$. The recess 501 finally becomes a wide element isolating region 507, while the recess 501a finally becomes a narrow element isolating region 502.

Secondly as shown in Figure 5(b), the anti- anisotropic etching film 503 is removed by etching. An insulation film, such as a silicon oxide film 504 having a thickness of 1μm, is deposited by a chemical vapour deposition method (hereinafter

referred to as CVD) on the semiconductor substrate 500 containing the recesses 501, 501a.

Thirdly, as shown in Figure 5(c), most of the silicon oxide film 504 is removed by etching so that the surface of the semiconductor substrate 500 is exposed. As a result, the silicon oxide film 504 remains only in the recess 501a and at the sides of the recess 501 so that the remaining silicon oxide films 505 and 506 form the element isolating regions 502, 507. The element isolating region 502 has a small area and the element isolating region 507 has a large area.

In the known semiconductor device shown in Figure 5(c), the narrow element isolating region 502 functions as a good element isolating region because the silicon oxide film substantially completely fills the recess 501a. However, when a field insulating film is required in a wide area of a semiconductor substrate, the element isolating region 507 does not function satisfactorily because the silicon oxide film 506 does not completely fill the recess 501. Therefore, in a semiconductor device as shown in Figure 5(c) there is an increase in interlayer capacity between a conductor layer and the substrate, and there is liable to be disconnection and short circuiting of the connector pattern formed in later process steps.

In order to try to solve such problems, some improved semiconductor devices have been disclosed in Japanese Laid

Open Applications Nos. 55-78540, 56-94646 and 56-94647. However, in the arrangements shown in these citations, it is impossible to repeatedly form an element isolating region in a submicron semiconductor device.

It is therefore desirable to provide a method of making a semiconductor device which provides a satisfactory element isolating region regardless of the area, configuration and width of the element isolating region.

Referring now to Figure 1(a), a mask (not shown) was first used to form an anti-anisotropic etching film 101 at selected places, i.e. in a predetermined pattern, on a semiconductor substrate such as a P-type silicon substrate 100. The anti-anisotropic etching film 101 was thus formed with recess portions 101a, 101b which extended to the substrate 100 so as to expose portions of the latter.

Secondly, as shown in Figure 1(b), the anti-anisotropic etching film 101 was used as a mask and recesses 102, 102a were formed in the P-type silicon substrate 100 by anisotropic etching such as the use of the RIE method. In detail, recesses 102, 102a, as deep as 7000 Å were formed by the RIE method using $CBrF_3$ gas in the substrate 100 in alignment with the recess portions 101a, 101b. For the fabrication of a wide element isolating region 110, a recess 102 was formed so as to enclose a predetermined location

for the wide element isolating region 110. In Figure 2, a recess 201 corresponds to the recess 102. Each recess 102a was provided for the fabrication of a narrow element isolating region 111.

As will be seen from Figure 2, the recess 201 is annular, the term "annular" being used herein in a wide sense to include a rectangular, ring-like shape as shown.

Thirdly, as shown in Figure 1(c), boron was implanted as necessary by ion implantation in the recesses 102, 102a for forming the element isolating regions 110, 111, the boron ions being indicated at 103. The concentration of boron was $3 \times 10^{15} cm^{-2}$ with respect to 30 KeV. Thus stopper regions 104 were formed at the base of the recesses 102, 102a.

Fourthly, as shown in Figure 1(d), the anti-anisotropic film 101 was removed and a silicon oxide insulating film 105, having a thickness of up to 1μm, was deposited by the CVD method on the P-type silicon substrate 100 having the recesses 102, 102a.

Fifthly, as shown in Figure 1(e), the silicon oxide film 105 was removed by the RIE method using CF_4 + CHF_3 gas so that the silicon oxide film 105 remained only in the recesses 102, 102a. The P-type silicon substrate 100 was exposed except at the recesses 102, 102a. Thus a silicon oxide film 106, constituting an insulating material, was formed in each of the recesses 102, 102a in the P-type silicon substrate 100.

Sixthly, as shown in Figures 1(f) and 1(g), the P-type silicon substrate 100 was thermally oxidized in a dry oxygen atmosphere at 1000°C for about 100 minutes to form a silicon oxide film 107 having a thickness of about 800 Å. The silicon oxide film 107 having a thickness of about 800 Å can be placed on the surface of the P-type silicon substrate 100 by accurately controlling the film thickness of the silicon oxide film 105 shown in Figure 1(d) and by controlling the etching time. The silicon oxide film 107 extends over the whole substrate 100 so as to contact the silicon oxide film 106 in the recesses 102, 102a. A silicon nitride anti-oxidation mask film 108, having a thickness of about 1500 Å, was formed on the silicon oxide film 107 by vapour growth, e.g. by the CVD method. Then, in order to remove the silicon nitride film 108 from substantially the whole of the wide element isolating region 110, a photo resist layer 109 was formed by the use of a mask (not shown) at selected places on the silicon nitride film 108. The photo resist layer 109 was used as a mask and the silicon nitride film 108 was selectively removed by plasma etching using CF_4 gas so that the silicon nitride film 108 remained substantially only around the wide element isolating region 110. Then the photo resist layer 109 was removed by etching.

Seventhly, as shown in Figure 1(g), the silicon nitride

film 108 which remained was used as a mask, and the P-type silicon substrate 100 was selectively oxidized in a wet oxygen atmosphere at 950°C, 8 atm, for 1 hour.Thus, as shown in Figure 1(h), a predetermined oxide film 112 was formed. And then the silicon nitride film 108 was completely removed by etching, thereby forming the required element isolating regions 110 and 111.

Figure 1(h) corresponds to Figure 2 as follows.

In Figure 2, reference numeral 200 shows a P-type silicon substrate. The hatched portion 201 and the dotted portion 203 correspond to the recesses 102, 102a respectively. The reference numerals 202 and 204 respectively show the element isolating region having a large area 110 and the element isolating region having a small area 111. The reference numeral 203 shows the same portion as indicated by the reference numeral 204.

Figures 3(a) to (f) illustrate another method of making a semiconductor device according to the present invention.

Firstly, a semiconductor device as shown in Figure 3(a) was formed by a method similar to that shown in Figures 1(a) to (c). The reference numeral 300 shows a P-type silicon substrate. The reference numeral 301 shows an anti-anisotropic etching film. The reference numerals 302, 302a show recesses. The reference numeral 303 indicates boron ions. The reference numeral 304 shows stopper regions. The reference numerals 313 and 314 show narrow and wide element

isolating regions respectively.

Secondly, as shown in Figure 3(b), a silicon oxide film 305 having a thickness of 800 Å, was formed in a dry oxygen atmosphere on the P-type silicon substrate 300 having the recesses 302, 302a. Then as an anti-oxidation mask film, a silicon nitride film 306 having a thickness of about 1400 Å was formed on the silicon oxide film 305 by vapour growth, e.g. by the CVD method. Further, a polycrystalline silicon film 307 having a thickness of about 3500 Å was also formed on the polycrystalline silicon film 307 by vapour growth, e.g. by the CVD method. A thermoplastic photo resist film 308 having a thickness of 2μm was coated on the polycrystalline silicon film 307. Then the outer surface of the photo-resist film 308 was smoothed by heating at about 200°C for 5 minutes.

Thirdly, as shown in Figure 3(c), most of the photo-resist film 308 was removed from the surface of the polycrystalline silicon film 307 by plasma-etching using oxygen. The termination of etching was detected by the state of the surface of the polycrystalline silicon film 307. In this case, photo resist 308 remained in a part of the recess 302a in the element isolating region 313.

Fourthly, as shown in Figure 3(d), the photo resist 308 which remained in the recess 302a was used as a mask and the polycrystalline silicon film 307 which was exposed on the P-type

silicon substrate 300 was removed by plasma-etching using CF_4 gas so that it remained only in the recesses 302, 302a. As a result, polycrystalline silicon 309 remained in a part of each recess 302, 302a without completely filling the latter. The remaining photo resist 308 was removed by etching.

Fifthly, as shown in Figure 3(e) except for a region substantially corresponding to the wide element isolating region 314, the device was masked by a photo resist layer 310. For example, the silicon nitride film 306 was selectively removed by plasma-etching using CF_4 gas.

Sixthly, as shown in Figure 3(f), after removal of the photo resist layer 310, the P-type silicon substrate 300 was masked by the silicon nitride film 306 as an anti-oxidization mask in a wet oxygen atmosphere and oxidization was accomplished at about 950°C, 8 atm for 2 hours. Thus a predetermined oxide film 311 was formed and the polycrystalline silicon 309 was formed into a silicon oxide insulating film 312. The silicon nitride film 306 exposed on the surface of the P-type silicon substrate 300 was removed by etching. As a result, the narrow element isolating region 313 and the wide element isolating region 314 were formed.

Figures 4(a) to (c) illustrate yet another method for making a semiconductor device according to the present invention.

In this particular embodiment of the invention, the first four steps in the method employed correspond to those illustrated in Figures 3(a), 3(b), 3(c) and 3(d) respectively. Thus Figure 4(a) shows the condition in which the photo resist 308 has been removed after a step corresponding to that of Figure 3(d). The reference numeral 400 shows a P-type silicon substrate corresponding to the substrate 300. The reference numeral 401 shows a narrow element isolation region corresponding to the region 313. The reference numerals 402, 402a show recesses corresponding to the recesses 302, 302a. The reference numeral 403 shows a wide element isolating region corresponding to the region 314. The reference numeral 404 shows stopper regions corresponding to the stopper regions 304. The reference numeral 405 shows a silicon oxide film corresponding to the film 305. The reference numeral 406 shows a silicon nitride film corresponding to the film 306. A silicon oxide film 409 was prepared by a process corresponding to thermally oxidizing the polycrystalline silicon 309 as shown in Figure 3(d), the thermal oxidation being at 950°C, 8atm for 4 hours, for example.

Secondly, as shown in Figure 4(b), the silicon nitride film 406 on the P-type silicon substrate 400 was masked by a pattern of photo resist 407 and the unmasked silicon nitride film 406 was removed by plasma etching using CF_4 gas.

Thirdly, as shown in Figure 4(c), the exposed P-type

silicon substrate 400 was oxidized in a wet oxide atmosphere at 950°C, 8 atm, for 1 hour, for example. Thus a predetermined oxide film 408 was formed. Then the silicon nitride film 406 on the surface of the P-type silicon substrate 400 was removed by etching. As a result, the narrow element isolating region 401 and the wide element isolating region 403 were obtained.

In the embodiments described above, a P-type silicon substrate was used as a semiconductor device, but an N-type silicon substrate can be used if desired. When an N-type silicon substrate is used, phosphorous or arsenic instead of boron can be implanted by stopper ion implantation.

In the embodiment of Figure 3(a) to (f), a photo resist 308 was used which extended into a recess in the polycrystalline silicon film 307. The photo resist 308, however, can be replaced by a BPSG (boron phosphorous silicate glass) film. When such a BPSG film is etched, the RIE method using a mixture of gaseous CF_4 + H_2 can be employed.

Further, in the so-called active region of the device outwardly of the narrow element isolating region and the wide isolating region formed as described above, an MOS type electric field effect transistor or bipolar type transistor may be formed by a normal method.

The "wide element isolating regions" referred to above mean the regions whose areas are enclosed by the recesses

102, 302, 402 and may be several μm in width.

It will be noted that in Figure 3(d) the polycrystalline silicon 309 in the recesses 302, 302a does not completely fill the latter so that parts of the side walls of these recesses are exposed. This is a desirable feature since the thermal oxidation of the polycrystalline silicon 309 which occurs subsequently, as illustrated in Figure 3(f), causes expansion of the polycrystalline silicon 309 so as to fill the recesses 302, 302a therewith. However, it is not essential to provide this feature.

CLAIMS

1. A method of making a semiconductor device comprising etching a semiconductor substrate to form at least a first recess and a second recess therein, the second recess enclosing a portion of the semiconductor substrate; introducing insulating material into the first and second recesses; and oxidising the said portion of the semiconductor substrate, whereby there is formed in the same semiconductor substrate a relatively narrow element isolating region which is constituted by the insulating material in the first recess and a relatively wide element isolating region which is constituted both by the insulating material in the second recess and by the said oxidised portion.

2. A method as claimed in claim 1 in which prior to the oxidation of the said portion, an anti-oxidation mask is applied over the whole of the semiconductor substrate except for the oxidised portion and an adjacent part of the second recess.

3. A method as claimed in claim 1 or 2 in which an impurity is introduced to the base of each of the recesses so as to form a stopper region.

4. A method as claimed in any preceding claim in which the width of the wide element isolating region is several μm.

5. A method as claimed in any preceding claim in which the said etching is anisotropic etching.

6. A method as claimed in claim 5 in which the second recess is formed by forming on said substrate an anti-anisotropic etching film, having a recess portion therein, which extends to the substrate so as to expose a portion of the latter, effecting anisotropic etching of the said recess portion, and removing the anti-anisotropic etching film.

7. A method as claimed in any preceding claim in which the insulating material is a silicon oxide film.

8. A method as claimed in claim 7 in which a polycrystalline silicon film is introduced into the second recess and is oxidised to form the said silicon oxide film.

9. A method as claimed in claim 8 in which the polycrystalline silicon film does not completely fill the second recess.

10. A method as claimed in any of claims 7-9 in which, after the said silicon oxide film has been formed in the first and second recesses, a further silicon oxide film is formed over the whole substrate so as to contact the silicon oxide film in the first and second recesses, an anti-oxidation mask film being formed on the further silicon oxide film.

11. A method as claimed in claim 10 in which the substrate is a silicon substrate, the further silicon oxide film being formed by thermal oxidation of the silicon substrate.

12. A method as claimed in any preceding claim in which insulating material is introduced into the first recess.

13. A semiconductor device when made by the method of any preceding claim.

14. A semiconductor device comprising semiconductor substrate having at least a first recess and a second recess therein, the second recess enclosing an oxidised portion of the semiconductor substrate, and the first and second recesses containing insulating material, whereby the semiconductor substrate is provided with a relatively narrow element isolating region which is constituted by the insulating material in the first recess and a relatively wide element isolating region which is constituted both by the insulating material in the second recess and by the said oxidised portion.

15. A method of making a semiconductor device substantially as hereinbefore described.