PHASE CHANGE MEMORY CELL AND METHOD OF FORMATION

FIELD OF THE INVENTION

[0001] The present invention relates to semiconductor devices, and in particular phase-change memory devices and method of forming the same.

BACKGROUND OF THE INVENTION

[0002] Non-volatile memories are important elements of integrated circuits due to their ability to maintain data absent a power supply. Phase change materials have been investigated for use in non-volatile memory cells. Phase change memory cells include phase change materials, such as chalcogenide alloys, which are capable of stably transitioning between amorphous and crystalline phases. Each phase exhibits a particular resistance state and the resistance states distinguish the logic values of the memory cell. Specifically, an amorphous state exhibits a relatively high resistance, and a crystalline state exhibits a relatively low resistance.

[0003] A typical phase change cell has a layer of phase change material between first and second electrodes. As an example, the phase change material is a chalcogenide alloy, such as $Ge_2Sb_2Te_5$ or SbTeAg. See, e.g., Lankhorst et al., *Low-cost and nanoscale non-volatile memory concept for future silicon chips*, NATURE MATERIALS, vol. 4 pp. 347-352 (April 2005).

[0004] A portion of the phase change material is set to a particular resistance state according to the amount of current applied via the electrodes. To obtain an amorphous state, a relatively high write current pulse (a reset pulse) is applied through the phase change cell to melt a portion of the material for a short period of time. The current is removed and the cell cools rapidly to below the glass transition temperature, which results in the portion of the material having an amorphous phase. To obtain a crystalline state, a lower current write pulse (a set pulse) is applied to the phase change cell for a longer period of time to heat the material to below its melting point. This causes the amorphous portion of the material to re-crystallize to a crystalline phase that is maintained once the current is removed and the cell 10 is rapidly cooled.

[0005] A sought after characteristic of non-volatile memory is low power consumption. Often, however, phase change memory cells require large operating currents. It would therefore be desirable to provide a phase change memory cell with reduced current requirements.

BRIEF SUMMARY OF THE INVENTION

[0006] Embodiments of the invention provide a phase change memory element and methods for forming the same. The memory element includes a first electrode and a chalcogenide comprising phase change material layer over the first

electrode. A metal-chalcogenide layer is over the phase change material layer. The metal chalcogenide layer comprises tin-telluride-telluride. A second electrode is over the metal-chalcogenide layer. The memory element is configured to have reduced power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The foregoing and other advantages and features of the invention will become more apparent from the detailed description of exemplary embodiments provided below with reference to the accompanying drawings in which:

[0008] FIG. 1 depicts a phase change memory element according to an embodiment of the invention;

[0009] FIGS. 2A-2C depict the formation of the memory elements of FIG. 1 at different stages of processing; and

[0010] FIG. 3 is a block diagram of a system including a memory element according to an exemplary embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0011] In the following detailed description, reference is made to various specific embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention. It is to be

understood that other embodiments may be employed, and that various structural, logical and electrical changes may be made without departing from the spirit or scope of the invention.

[0012] The term "substrate" used in the following description may include any supporting structure including, but not limited to, a semiconductor substrate that has an exposed substrate surface. A semiconductor substrate should be understood to include silicon, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is made to a semiconductor substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation. The substrate need not be semiconductor-based, but may be any support structure suitable for supporting an integrated circuit, including, but not limited to, metals, alloys, glasses, polymers, ceramics, and any other supportive materials as is known in the art.

[0013] The invention is now explained with reference to the figures, which illustrate exemplary embodiments and throughout which like reference numbers indicate like features. FIG. 1 depicts an exemplary embodiment of a memory element 100 constructed in accordance with the invention. The device 100 shown in

FIG. 1 is supported by a substrate 10. Over the substrate is a first insulating layer 11. A first electrode 21 overlies the first insulating layer 11 and substrate 10. The first electrode 12 can be any suitable conductive material, and is tungsten (W) in the illustrated embodiment.

[0014] A second insulating layer 14 is over the first electrode 12. A via 42 is within the insulating layer 14 to expose a portion of the first electrode 12. In the illustrated embodiment, the via 42 extends through a portion of the first electrode 12. The second insulating layer 14 can be a nitride, such as silicon nitride (Si_3N_4); a low dielectric constant material; an insulating glass; an insulating polymer; among other materials.

[0015] As shown in FIG. 1, a layer 18 of phase change material, specifically a chalcogenide material layer 18 is deposited within the via 42 and over the first electrode 12. In the illustrated embodiment, the layer 18 is a germanium-telluride layer. Other exemplary chalcogenide compositions for the layer 18 include concentrations of Te below about 70%. The germanium concentration is preferably above about 10%. The layer 18 can include additional elements, for example antimony. The percentages given are atomic percentages which total 100% of the atoms of the constituent elements. In the illustrated example, the germanium-telluride layer 18 is about 300 Å thick and in electrical contact with the underlying

first electrode 12, but less than about 100 Å thick at the edges 42a of the via 42 adjacent the underlying first electrode 12. Over the germanium-telluride layer 18 and within the via 42 is a tin-telluride layer 20. In the illustrated embodiment, the layer 20 is about 50% tin and about 50% tellurium and is about 500 Å thick.

[0016] Although layer 20 is shown over the chalcogenide material layer 18, it should be understood that the orientation of the layers can be altered. For example, the chalcogenide material layer 18 may be over the layer 20.

[0017] Over the tin-telluride layer 20 and within the via 42 is a second electrode 24. The second electrode 24 can be any suitable conductive material, and is tungsten in the illustrated embodiment.

[0018] For operation, a pulse generator 35 is used to apply a reset pulse of about 1.4 V, and a current of less than or about 280 μA is used. The reset pulse melts at least a portion of the germanium-telluride layer 18 leaving the layer 18 in a high resistance, amorphous state. A set pulse of about 1.17 V, and a current of less than or about 200 μA is used. The set pulse crystallizes at least a portion of the tellurium layer 18 leaving the layer 18 in a low resistance state.

[0019] FIGS. 2A-2C are cross sectional views of a wafer depicting the formation of the memory element 100 according to an exemplary embodiment of the

invention. No particular order is required for any of the actions described herein, except for those logically requiring the results of prior actions. Accordingly, while the actions below are described as being performed in a specific order, the order is exemplary only and can be altered if desired. Although the formation of a single memory element 100 is shown, it should be appreciated that the memory element 100 can be one memory element in an array of memory elements, which can be formed concurrently.

[0020] As shown by FIG. 2A, a substrate 10 is initially provided. As indicated above, the substrate 10 can be semiconductor-based or another material useful as a supporting structure as is known in the art. A first insulating layer 11 is formed over the substrate 10 and a first electrode 12 is formed over the insulating layer 11. A second insulating layer 14 is formed over the first electrode 12. The first insulating layer can be, for example silicon dioxide. The second insulating layer 14 can be silicon nitride, a low dielectric constant material, or other suitable insulators known in the art, and may be formed by any method known in the art.

[0021] As illustrated in FIG. 2B, a via 42 is formed, for instance by photolithographic and etching techniques, within the second insulating layer 14 to expose a portion of the first electrode 12. Optionally, the via 42 can extend partially through the first electrode 12.

[0022] As shown in FIG. 2C, a germanium-telluride layer 18 is formed over the first electrode 12 and second insulating layer 14 and within the via 42. Formation of the germanium-telluride layer 18 may be accomplished by any suitable method. The layer 18 is formed having a thickness of about 300 Å.

[0023] A tin-telluride layer 20 is formed over the germanium-telluride layer 18 and within the via 42. The layer 20 can be formed by any suitable method, e.g., physical vapor deposition, chemical vapor deposition, co-evaporation, sputtering, among other techniques. The layer 18 is formed having a thickness of about 500 Å.

[0024] A conductive material is deposited over the tin-telluride layer 20 and within the via 42 to form a second electrode 24. Similar to the first electrode 12, the conductive material for the second electrode 24 may be any material suitable for a conductive electrode, for example, tungsten. In the illustrated embodiment, the layers 18, 20, 24 are formed as blanket layers.

[0025] Additional processing steps can be performed, for example the formation of connections to other circuitry of the integrated circuit (e.g., logic circuitry, sense amplifiers, etc.) of which the memory element 100 is a part, as is known in the art.

[0026] FIG. 3 illustrates a processor system 300 which includes a memory circuit 348, e.g., a memory device, which employs memory array 301, which includes at least one memory element 100 constructed according to the invention. The processor system 300, which can be, for example, a computer system, generally comprises a central processing unit (CPU) 344, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 346 over a bus 352. The memory circuit 348 communicates with the CPU 344 over bus 352 typically through a memory controller.

[0027] In the case of a computer system, the processor system 300 may include peripheral devices such as a floppy disk drive 354 and a compact disc (CD) ROM drive 356, which also communicate with CPU 344 over the bus 352. Memory circuit 348 is preferably constructed as an integrated circuit, which includes a memory array 301 having at least one memory element 100 according to the invention. If desired, the memory circuit 348 may be combined with the processor, for example CPU 344, in a single integrated circuit.

[0028] The above description and drawings are only to be considered illustrative of exemplary embodiments, which achieve the features and advantages of the present invention. Modification and substitutions to specific process

conditions and structures can be made without departing from the spirit and scope of the present invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

CLAIMS

[0029] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory element comprising:

   a first electrode;

   a chalcogenide comprising phase change material layer over the first electrode;

   a metal-chalcogenide layer over the phase change material layer, the metal chalcogenide layer comprising tin-telluride;

   a second electrode over the metal-chalcogenide layer.

2. The memory element of claim 1, further comprising an insulating layer over the first electrode and a via within the insulating layer; wherein the phase change material layer, and the metal-chalcogenide layer are within the via.

3. The memory element of claim 2, wherein the phase change material layer has a thickness of less than or equal to about 100 Å at an edge of the via adjacent the first electrode.

4. The memory element of claim 1, wherein the memory element configured to be set to a first resistance state using a current of less than or about 200 μA.

5. The memory element of claim 3, wherein the memory element is configured to be reset to a second resistance state using a current of less than or about 280 μA.

6. The memory element of claim 1, wherein the memory element is configured to be reset to the second resistance state using a voltage of about 1.4 V.

7. The memory element of claim 6, wherein the memory element is configured to be set to the first resistance state using a voltage of about 1.17 V.

8. The memory element of claim 1, wherein the phase change material layer comprises germanium-telluride.

9. The memory element of claim 1, wherein the phase change material layer has a thickness of about 300 Å.

10. The memory element of claim 1, wherein the metal-chalcogenide layer has a thickness of about 500 Å.

11. The memory element of claim 1, wherein one or both of the first and second electrodes comprise tungsten.

12. A memory array comprising:

a plurality of memory elements, at least one memory element comprising:

a first electrode;

a chalcogenide comprising phase change material layer over the first electrode;

a metal-chalcogenide layer over the phase change material layer, the metal chalcogenide layer comprising tin-telluride;

a second electrode over the metal-chalcogenide layer.

13. The memory array of claim 12, wherein the at least one memory element further comprises an insulating layer over the first electrode and a via within the insulating layer;

wherein the phase change material layer, and the metal-chalcogenide layer are within the via.

14. The memory array of claim 13, wherein the phase change material layer has a thickness of less than or equal to about 100 Å at an edge of the via adjacent the first electrode.

15. The memory array of claim 12, wherein the memory element is configured to be set to a first resistance state using a current of less than or about 200 μA.

16. The memory array of claim 15, wherein the memory element is configured to be set to the first resistance state using a voltage of about 1.17 V.

17. The memory array of claim 12, wherein the memory element is configured to be reset to a second resistance state using a current of less than or about 280 μA.

18. The memory array of claim 17, wherein the memory element is configured to be reset to the first resistance state using a voltage of about 1.4 V.

19. The memory array of claim 12, wherein the phase change material layer has a thickness of about 300 Å.

20. The memory array of claim 12, wherein the phase change material layer comprises germanium-telluride.

21. The memory array of claim 12, wherein the metal-chalcogenide layer has a thickness of about 500 Å.

22. The memory array of claim 12, wherein one or both of the first and second electrodes comprise tungsten.

23. A processor system comprising:

a processor; and

a memory device comprising a memory element, the memory element comprising:

a first electrode;

a germanium-telluride layer over the first electrode;

a tin-telluride layer over the germanium-telluride layer;

a second electrode over the tin-telluride layer.

24. The system of claim 23, wherein the memory element further comprises an insulating layer over the first electrode and a via within the insulating layer; wherein the phase change material layer, and the metal-chalcogenide layer are within the via.

25. The system of claim 24, wherein the phase change material layer has a thickness of less than or equal to about 100 Å at an edge of the via adjacent the first electrode.

26. The system of claim 23, wherein the memory element is configured to be set to a first resistance state using a current of less than or about 200 μA.

27. The system of claim 26, wherein the memory element is configured to be set to the first resistance state using a voltage of about 1.17 V.

28. The system of claim 23, wherein the memory element is configured to be reset to a second resistance state using a current of less than or about 280 μA.

29. The system of claim 28, wherein the memory element is configured to be reset to the second resistance state using a voltage of about 1.4 V.

30. The system of claim 23, wherein the germanium-telluride layer has a thickness of about 300 Å.

31. The system of claim 23, wherein the tin-telluride layer has a thickness of about 500 Å.

32. The system of claim 23, wherein one or both of the first and second electrodes comprise tungsten.

33. A method for forming a memory element, the method comprising:

forming a first electrode;

forming a chalcogenide comprising phase change material layer over the first electrode;

forming a metal-chalcogenide layer over the phase change material layer, the metal chalcogenide layer formed comprising tin-telluride;

forming a second electrode over the metal-chalcogenide layer.

34. The method of claim 33, further comprising the acts of:

forming an insulating layer over the first electrode; and

forming a via within the insulating layer; wherein the phase change material layer, and the metal-chalcogenide layer are formed within the via.

35. The method of claim 34, wherein the phase change material layer is formed having a thickness of less than or equal to about 100 Å at an edge of the via adjacent the first electrode.

36. The method of claim 33, wherein the memory element is formed to be set to a first resistance state using a current of less than or about 200 μA.

37. The method of claim 36, wherein the memory element is formed to be reset to a second resistance state using a current of less than or about 280 μA.

38. The method of claim 33, wherein the memory element is formed to be reset to the second resistance state using a voltage of about 1.4 V.

39. The method of claim 38, wherein the memory element is formed to be set to the first resistance state using a voltage of about 1.17 V.

40. The method of claim 33, wherein the phase change material layer is formed having a thickness of about 300 Å.

41. The method of claim 33, wherein the phase change material layer is formed comprising germanium-telluride.

42. The method of claim 33, wherein the metal-chalcogenide layer is formed having a thickness of about 500 Å.

43. The method of claim 33, wherein one or both of the first and second electrodes are formed comprising tungsten.