## CLAIMS

What is claimed is:

1. An integrated circuit for a print component comprising:

a plurality of memory bits;

a single lane analog bus conductively coupling the plurality of memory bits to a pad located on an exterior of the integrated circuit; and

the pad to transmit an electrical signal from the plurality of memory bits, wherein the electrical signal indicates a combination of all selected bits of the plurality of memory bits;wherein the integrated circuit is configured so that, when an external current is applied, a lower voltage signal is transmitted via the pad for a selected plurality of memory bits relative to a voltage for a single selected memory bit.

2. The integrated circuit of claim 1, wherein the pad is to transmit a single electrical signal from the plurality of memory bits, simultaneously, representing a parallel bit read of the plurality of memory bits.

3. The integrated circuit of claim 1 or 2, wherein the pad is external to a die to connect to a printer-side contact.

4. The integrated circuit of any of claims 1-3, wherein the pad is an analog signal pad to communicate an analog signal.

5. The integrated circuit of any of claims 1-4, wherein, the pad is a pad to communicate sensor states, in addition to the electrical signal.

6. The integrated circuit of any of claims 1-5, wherein a first memory bit of the plurality of memory bits is located on a first silicon die and a second memory bit of the plurality of memory bits is located on a second silicon die.

7. The integrated circuit of claim 6, wherein the first silicon die is associated with a first fluid type and the second silicon die is associated with a second fluid type different than the first type.

8. The integrated circuit of any of claims 1-7, further comprising fluidic actuators; and select logic to select the plurality of memory bits and the fluidic actuators using the same select lane.

9. The integrated circuit of any of claim 8, wherein the select logic comprises an address decoder to select fluid actuators and memory bits corresponding to the selected fluid actuators in response to an address.

10. The integrated circuit of any of claims 1-9, configured so that, when an external voltage is applied, a higher current signal is transmitted via the pad for a selected plurality of memory bits relative to a current for a single selected memory bit.

11. The integrated circuit of any of claims 1-10, wherein the plurality of memory bits behave with higher resistance when unprogrammed, and with lower resistance when programmed.

12. The integrated circuit of any of claims 1-11, further comprising nozzles, wherein the plurality of memory bits correspond to fluidic actuators proximate to the nozzles.

13. The integrated circuit of any of claims 12, wherein the pad is conductively connected to transmit an electrical signal from a crack detection resistor in combination with the plurality of memory bits.

14. The integrated circuit of claim 13, further comprising a plurality of nozzles, wherein:

the plurality of memory bits correspond to fluidic actuators proximate to the plurality of nozzles; and

the crack detection resistor is routed in-between the nozzles.

15. An integrated circuit associated with a communicating replaceable print head cartridge, comprising a single sense contact pad located on an exterior of the replaceable print head cartridge, the single sense contact pad to transmit an electrical signal from a plurality of memory bits, wherein the electrical signal indicates a combination of all selected bits of the plurality of memory bits, wherein the integrated circuit is configured so that, when an external current is applied, a lower voltage signal is transmitted via the pad for a selected plurality of memory bits relative to a voltage for a single selected memory bit.

16. The integrated circuit of claim 15,

wherein the pad is to transmit a single electrical signal from the plurality of memory bits, simultaneously, representing a parallel bit read of the plurality of memory bits.

17. The integrated circuit of claim 15 or 16, wherein a first memory bit of the plurality of memory bits is located on a first silicon die and a second memory bit of the plurality of memory bits is located on a second silicon die.

187. The integrated circuit of claim 17, wherein the first silicon die is associated with a first fluid type and the second silicon die is associated with a second fluid type different from the first type.

19. The integrated circuit of any of claims 15-17, further comprising fluidic actuators; and select logic to select the plurality of memory bits and fluidic actuators using the same select lane.

20. A method for communicating stored data from an integrated circuit, comprising:

selecting a plurality of memory bits;

providing an input analog electrical signal to the plurality of memory bits;

measuring an output analog electrical signal on a single sense contact pad communicatively connected to the plurality of memory bits, the measurement to be made for the plurality of memory bits in combination,

wherein the method is configured so that, when an external current is applied, a lower voltage signal is transmitted via the pad for a selected plurality of memory bits relative to a voltage for a single selected memory bit.

21. The method of claim 20, comprising transmitting a single electrical signal from the plurality of memory bits, simultaneously, representing a parallel bit read of the plurality of memory bits.

22. The method of of claims 20 or 21, configured so that, when an external voltage is applied, a higher current signal is transmitted via the pad for a selected plurality of memory bits relative to a current for a single selected memory bit.

23. The method of any of claims 20-22, wherein the plurality of memory bits each correspond to a fluidic actuator located on a silicon die.

24. The method of any of claims 20-23, wherein the plurality of memory bits correspond to a plurality of fluidic actuators, where the plurality of fluidic actuators are located on a plurality of silicon dies.

25. The method of any of claims 20-24, wherein the memory bits behave with higher resistance when unprogrammed, and with lower resistance when programmed