

WIDE BIPHASE DIGITAL SERVO INFORMATION,
DETECTION, AND ESTIMATION FOR DISK DRIVE
USING VITERBI DETECTION

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Cross Reference to Related Applications

This application claims the benefit of U.S. Provisional Application No. 60/006013 filed October 23, 1995. This application is related to U.S. Patent Application Serial No. 08/320,540 filed October 12, 1994.

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Field of the Invention

The present invention relates to apparatus and methods for storing, detecting, and estimating servo information stored on disk drive media, and in particular to apparatus and methods useful with partial response, maximum likelihood detection channels and magnetic disk media.

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Background of the Invention

By reading servo information recorded within data tracks on a disk surface, a disk drive head positioner servo system is able to estimate data transducer head position. The recorded servo information typically includes track (i.e. cylinder and head) addresses and servo bursts. Each circumferential data track on a disk surface has a unique track address, which is recorded in servo sectors embedded in the track, and servo burst patterns frequently repeat every two or more tracks. When a disk drive is seeking to a radial track location, the track addresses are used as coarse positioning information to approximately estimate the position of the read head and the servo bursts are used as fine positioning information to position the head precisely on the desired radial location.

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At seek time while reading track addresses, the head may be positioned between two adjacent tracks. In this situation, the head may receive a superposition of signals from both tracks. One solution to this ambiguity is to encode the track addresses into Gray-coded addresses so that the encoded addresses of any two adjacent tracks differ from each other by only in a single bit position. With this solution, when the head is reading two tracks, the ambiguity after decoding the address is one track, and an error of one track is acceptable at seek time.

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In accordance with one known technique, each data track is divided into plural sectors. Each sector includes a header section, followed by a data section. The header section may typically include a DC erase field, a preamble field, a header synchronization

character, a track address field (coarse servo information) and a servo burst field (fine servo information). The data section may typically include another preamble field, a data synchronization character, a block of user data, and error correction bytes. In this example, the header section is recorded at the same data rate as the data section, and synchronous peak detection through a single read channel structure in the disk drive is employed to read the information in both the header section and the data section. An example of this approach is found in commonly assigned U.S. Patent No. 5,036,408 to Leis et al., entitled: "High Efficiency Disk Format and Synchronization System", the disclosure thereof being incorporated herein by reference.

Another known technique is to employ radial zones or bands of concentric data tracks, each zone having a data transfer rate associated with disk radius of the zone. In this example, data areas are separated by a series of radially extending embedded servo sectors which are factory recorded with servo information at a single data transfer rate. A servo data recovery circuit asynchronously (i.e. without phase lock to incoming servo data) recovers a servo address mark, a track number and fine position information from information read by the data transducer while passing over each sector. The servo recovery circuit is separate from the read channel electronics employed for peak detection of user data information. This example is described in commonly assigned U.S. Patent No. 5,420,730 to Moon, et al., entitled: "Servo Data Recovery Circuit for Disk Drive Having Digital Embedded Sector Servo", the disclosure thereof being incorporated herein by reference.

One factor which has limited data storage densities in magnetic recording employing peak detection techniques has been intersymbol interference, arising when flux transitions are increasingly close to each other. One technique for increasing flux densities in magnetic recording while still accurately reading recorded data is to employ synchronous sampling data detection. This technique, frequently referred to as "partial response, maximum likelihood" (PRML) signalling, has provided some improved data storage densities, at the expense of increased circuit complexity, including a fast analog to digital conversion process, and channel equalization, either on the analog side or on the digital side of the signal stream, or both. An example of a disk drive employing PRML is given in commonly assigned U.S. Patent No. 5,345,342, to Abbott et al., entitled: "Disk Drive Using PRML Synchronous Sampling Data Detection and Asynchronous Detection of Sector Servo", the disclosure thereof being incorporated herein by reference. The approach described in this patent enabled special circuitry within the synchronous sampling data detection channel to asynchronously detect track number values in

embedded servo sectors recorded at a constant servo data rate whereas the user data rate differed by radial data zone across the recording disk. The servo bursts were read and processed using conventional peak detection, and sample and hold techniques.

5 An improvement over the asynchronous servo sampling technique taught by the Abbott et al. patent referred to above is found in a later, commonly assigned U.S. Patent No. 5,384,671 to Fisher, entitled: "PRML Sampled Data Channel Synchronous Servo Detector", the disclosure thereof being incorporated herein by reference. In this approach a timing loop of the synchronous sampling data detection system is phase locked to servo
10 information, the servo information including track address and fine position information is synchronously sampled and decoded. In this approach the servo preamble field is recorded as a conventional $1/4T$ sine wave pattern, which corresponds to a $2T$ pattern in a peak detection channel (T representing a unit sample cell or interval).

15 Viterbi detectors are known for use within synchronous sampled data detection channels. One example of a Viterbi detector is provided in commonly assigned U.S. Patent No. 5,341,387 to Nguyen, entitled: "Viterbi Detector Having Adjustable Detection Thresholds for PRML Class IV Sampling Data Detection", the disclosure thereof being
20 incorporated herein by reference.

25 While these prior approaches have worked well in their respective times, increasing data storage capacities and data transfer rates per unit size disk have led directly to a hitherto unsolved need for an improved disk drive head servo format, architecture and approach.

Summary of the Invention with Objects

30 A general object of the present invention is to provide improved and simplified methods, apparatus, and data format for addressing data tracks in a disk drive having a partial response, maximum likelihood synchronous sampled data detection channel.

35 Another object of the present invention is to provide a servo format and apparatus for a PRML disk drive which does not require separate peak-detection hardware.

 A further object of the present invention is to provide a simplified address decoding method and apparatus within a PRML disk drive.

One more object of the present invention is to provide a high efficiency servo address format enabling use of higher code rates, smaller cell times and less redundancy within embedded servo sectors which are synchronously sampled and detected within a PRML disk drive.

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In one aspect of the present invention a disk drive includes at least one rotating data storage disk having a major surface defining recording tracks divided into data sectors by narrow servo spokes. Each data sector of a track is recorded with user data encoded in accordance with a code having a predetermined distance and user data code rate. Each
10 servo spoke has at least one servo information field coded in a wide biphasic pattern at a servo code rate which is one fourth the user data code rate. In this aspect of the invention, a synchronous sampling data detection channel includes:

- a data transducer head positioned by a servo-controlled actuator over the recording track,
- 15 a preamplifier for receiving electrical analog signals magnetically induced by the data transducer head from flux transitions present in at least the servo information field,
- a digital sampler for synchronously sampling the electrical analog signals to produce digital samples, and
- a Viterbi detector coupled to receive digital samples from the synchronous
20 sampling data detection channel for decoding the coded wide biphasic pattern as a maximum likelihood servo data sequence.

The Viterbi detector may comprise a difference metric detector or a tree-search detector.

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The synchronous sampling data detection channel may include a finite impulse response filter adjusted to a partial response, class IV, target spectrum and in this example, the Viterbi detector is connected to receive equalized digital samples from an output of the finite impulse response filter.

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Alternatively, the synchronous sampling data detection channel may include a finite impulse response filter for filtering digital samples in accordance with a $1-D^2$ pulse response (partial response, class IV) where D represents a one bit cell delay, and a $1+D$ filter connected downstream of the finite impulse response filter in order to provide
35 digital samples filtered in accordance with a $1+D-D^2-D^3$ pulse response (EPR4). In this example the Viterbi detector is connected to receive EPR4 equalized wide biphasic samples from an output of the $1+D$ filter.

The wide biphasic magnet patterns as recorded in the plural servo information fields may be arranged as --++ magnet patterns for a binary zero information value and --++ magnet patterns for a binary one information value.

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Plural servo information fields may be provided within each servo spoke, and one of the fields may comprise a servo address mark pattern, such as a nine-symbol word 000100101 (binary) for marking the beginning of a servo information block. At least one servo information field may comprise a Gray coded track number binary pattern of predetermined bit length. This pattern is first decoded as a wide biphasic code and then it is decoded as a Gray code. The track number binary pattern may include a parity symbol, and in this case the channel may include circuitry for receiving and decoding the track number binary pattern and checking the parity symbol.

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In a related aspect of the invention, the servo information field may comprise two track number binary patterns of predetermined bit length, there being a first track number address of the track, and a second track number address of a track located adjacent to the track. In one preferred format, the second track number is recorded with a one-half track offset extending into the second track. As a further related aspect of the invention, one servo information field may further comprise an error correction code field holding error correction values calculated with respect to the first and second track numbers, and in this arrangement, the channel includes error correction code decoding and correcting circuitry for decoding, checking and correcting the decoded values of the first and second track numbers.

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These and other objects, advantages, aspects and features of the present invention will be more fully understood and appreciated upon consideration of the following detailed description of a preferred embodiment, presented in conjunction with the accompanying drawings.

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Brief Description of the Drawings

In the Drawings:

FIG. 1 is a block diagram of a disk drive read channel providing PR4 and EPR4 targets.

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FIG. 2 is a schematic diagram of a recording surface of a disk in the disk drive.

FIG. 3 illustrates a signal recorded on a servo sector on a track of the disk.

FIG. 4 is a block diagram of the fields of the servo sector.

FIG. 5A is a graph of an analog signal response from a magnetic recording of a single write current pulse wherein the channel has been equalized to an EPR4 target spectrum.

5 FIG. 5B is a graph of an analog signal response to e.g. a binary one ("00") wide biphasic write current sequence.

FIG. 5C is a graph of an analog signal response to e.g. a binary zero ("++") wide biphasic write current sequence.

10 FIG. 5D is a graph of an analog signal response to a wide biphasic sequence e.g. a binary 100 sequence ("++--++--").

FIG. 6A illustrates a first servo sector layout for track numbers without radial interference.

FIG. 6B illustrates a second servo sector layout for track numbers without radial interference.

15 FIG. 7 is trellis diagram of a PR4 channel with wide bi-phase paths highlighted.

FIG. 8A is a trellis diagram of a wide bi-phase PR4 channel with four samples taken at a time.

FIG. 8B is a simplification of the diagram of FIG. 8A.

20 FIG. 9 is a block diagram of a difference-metric Viterbi detector for wide bi-phase codes.

FIG. 10 is a block diagram of a tree-search Viterbi detector for wide bi-phase codes.

FIG. 11 is a trellis diagram of an EPR4 channel with wide bi-phase paths highlighted.

25 FIG. 12A is a trellis diagram of a wide bi-phase EPR4 channel with four samples taken at a time.

FIG. 12B is a simplification of the block diagram of FIG. 7A.

FIGS. 13A-13E are diagrams illustrating servo bursts formats.

FIGS. 14A-14B are block diagrams of servo burst detectors.

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Detailed Description of Preferred Embodiments

Turning to FIG. 1, a disk drive 10 incorporates a programmable and adaptive PR4,ML read channel. The disk drive 10 may be one of a variety of embodiments, such as that disclosed in commonly assigned U.S. Pat. No. 5,341,249 to Abbott et al., entitled:

35 "Disk Drive Using PRML Class IV Sampling Data Detection with Digital Adaptive Equalization", the disclosure thereof being incorporated herein by reference. (This patent is the parent of the Abbott et al. U.S. Patent No. 5,345,342, referenced hereinabove.)

The drive 10 includes at least one data storage disk 16. As is conventional, a data transducer head 26, for example, a magneto-resistive head, is associated in a "flying" relationship over a disk surface of each disk 16. The head 26 is positioned relative to selected ones of a multiplicity of concentric data storage tracks 71 defined on each storage surface of the rotating disk 16, see FIG. 2.

Embedded servo patterns are written by a servo writer on selected data storage surfaces of the disk 16, see FIG. 2, for example, in accordance with the methods described in a commonly assigned U.S. Pat. No. 5,170,299, the disclosure of which is incorporated here by this reference.

During reading, flux transitions sensed by head 26 as it flies in close proximity over the selected data track 71 are preamplified by a read preamplifier circuit 28. The preamplified analog signal (or "read signal") is then sent into an analog variable gain amplifier (VGA) 38. After controlled amplification, the read signal is then passed through a programmable analog filter/equalizer stage 40.

The analog filter/equalizer 40 is programmed so that it is optimized for the data transfer rate of the selected data zone 70 from within which the transducer head 26 is reading data. The equalized analog read signal is then subjected to sampling and quantization within a high speed analog to digital (A/D) converter 46 which, when synchronized to user data, generates raw data samples $\{x(k)\}$ of at least five bits resolution.

An adaptive digital FIR filter 48 employs adaptive filter coefficients for filtering and conditioning the raw data samples $\{x(k)\}$ in accordance with the desired PR4 channel response characteristics in order to produce filtered and conditioned samples $\{y(k)\}$. The bandpass filtered and conditioned data samples $\{y(k)\}$ from FIR filter 48 are then passed over a data bus path 49 to a Viterbi detector (not shown), which detects user data with the PR4 target. In those embodiments using both a PR4 and an EPR4 target, the filtered and conditioned samples $\{y(k)\}$ from FIR filter 48 are also passed through a 1+D filter 50, the output path 51 of which provides the signal filtered to EPR4 channel response characteristics. (If only an EPR4 target is desired, FIR filter 48 is programmed with the appropriate coefficients directly, and 1+D filter 50 is not needed.)

A servo engine 32 is also provided within disk drive 10, and it develops head position control and correction values which are applied to control e.g. a rotary voice coil head positioner structure 30, in accordance with decoded wide biphasic servo information values, and burst values decoded in accordance with principles of the present invention.

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The samples, including raw data samples $\{x(k)\}$ and filtered samples $\{y(k)\}$, are taken at the data sampling rate, which has a clock bit time period T . This time T corresponds to a "bit cell" or, more simply, a "cell", at the sampling rate. A timing loop 44 may receive e.g. the PR4 target samples on path 49 and synchronize sampling and quantization by the analog to A/D converter 46 at desired sampling locations. Similarly, a gain loop 36 may control the VGA 38 based e.g. on the PR4 target samples on path 49. Timing and gain loops are described in the referenced Abbott et al. U.S. Patent No. 5,345,342. A DC offset control loop 37 may also be provided to adjust an offset amplifier 93 for DC offset, based on the PR4 target samples. A representative DC offset loop is described in commonly assigned U.S. Patent No. 5,459,679 to Ziporovich, entitled: "Real-Time DC Offset Control and Associated Method", the disclosure thereof being incorporated herein by reference.

As shown in FIG. 2, an exemplary data storage surface of a storage disk 16 has multiple concentric data tracks 71 which are preferably arranged in a plurality of data recording zones 70 between an inner landing zone area LZ and a radially outermost peripheral data track zone 70-1. In the illustrated example, the data tracks are shown as arranged into e.g. nine data zones including the outermost zone 70-1, and radially inward zones 70-2, 70-3, 70-4, 70-5, 70-6, 70-7, 70-8 and 70-9, for example. In practice, more zones are presently preferred. Each data zone has a bit transfer rate selected to optimize areal transition domain densities for the particular radius of the zone.

FIG. 2 also depicts a series of radially extending embedded servo sectors or "spokes" 68 which e.g. are equally spaced around the circumference of the disk 16. By way of the FIG. 3 overview, each servo sector 68 essentially includes a servo preamble field 68A, a servo identification field 68B, and a field 68C of circumferentially staggered, radially offset servo bursts, for example. While the number of data sectors per track varies from data zone to data zone, the number of embedded servo sectors, e.g. 68 per track, remains constant throughout the surface area of the disk 16, in the present example.

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The servo sectors 68 are preferably recorded at a single data cell rate and with phase coherency from track to track with a conventional servo writing apparatus at the



factory. A laser servo writer and head arm fixture suitable for use with the servo writer are described in commonly assigned U.S. Pat. No. 4,920,442, the disclosure of which is incorporated here by this reference. Alternatively, the servo sectors are written at zoned data cell rates, as described in commonly assigned U.S. Pat. No. 5,384,671, already
5 discussed above.

Turning to FIG. 4, each servo sector 68 or "spoke" has a servo identification field of embedded servo information such as is illustrated, for example. A optional DC erase field 731 of size e.g. 40 cells (illustrated in FIG. 4 with the time "40T" below the field) in
10 a clean area on the disk with substantially no or a few transitions, which can be used to flag the onset of a servo sector 68. A preamble field 732 of size e.g. 160 cells can be written in a 2T repeating pattern such as "--++ --++ --++" of the desired length. The preamble 732 is used by timing and gain loops to establish correct gain and phase lock relative to the incoming analog signal thereby to control sampling quantization by the
15 analog to digital converter 46. Together, the optional DC erase field 731 and the preamble field 732 comprise the preamble field 68A of Fig. 3.

A servo address mark 733 is used to reset the framing clock. This is followed by the e.g. three least significant bits (LSBs) 734 of the track number. The full spoke number
20 735 is optional, although at least one bit of information should be provided to enable rotational position to be determined. The entire track number 736 is recorded at least once. The head number (not shown) may also be recorded as part of the servo addressing information. Together, the servo address mark 733, the LSB field 734, full spoke number field 735 comprise the servo identification field 68B of Fig. 3.

25 Following the addressing information, servo bursts 737 are recorded, which are used to determine head position with respect to track center, as will be described. Examples of a variety of servo patterns are given hereinafter. These patterns in field 737 correlate to the field 68C of Fig. 3. The lengths of some or all the fields of the servo
30 sector 68 may be of programmable size. Other fields of information may also be recorded among or after the fields that have been described.

We turn now to describe wide bi-phase encoding, which may be used for some or all of the digital data storing fields of servo sector 68, such as the servo address mark 733,
35 LSB field 734, spoke number field 735 and track number field 736, for example. In writing digital data, one begins with an un-coded bit (that is, either a 0 or a 1), which is referred to as a symbol. Symbols are recorded on a disk by a coding that assigns one or

more signs or magnets (+ or -) to a cell. (Somewhat ambiguously, the signs may also be referred to as being either 0 or 1.) In bi-phase code, two signs are used, and symbols may be encoded as follows:

5 1 -> + -
 0 -> - +

We define a wide bi-phase (WBP) code, with code rate 1/4, as follows:

0 -> + + - -
1 -> - - + +

10 The DC erase field 731, which should have no flux transitions, cannot be WBP encoded.

The preamble field 732 may be WBP encoded with e.g. 40 or a programmable number of WBP symbols '1' (or cells "- - + +"), for PLL and AGC lock.

15 The servo address mark ("SAM") 733 may be a nine-symbol word '000100101' encoded in WBP that marks the beginning of a servo block. This SAM has the property that all shifts (auto correlation) disagree in at least 5 positions and therefore allows for 2 independent errors without loss of synchronization. When appended to the preamble
20 732 just described, the sequence looks like '. . . 111111000100101'. This is a modified Barker sequence.

The track number 736 may be a 14 symbol address or larger that is first encoded with a normal Gray code (with code-rate = 1) and then a parity symbol may be added.

25 The result is WBP encoded. The parity symbol, if any, cannot be used at seek time but can be used at read time to detect single errors. Gray coding is used to avoid large errors when simultaneously reading two adjacent track address when the read head 26 is between tracks at seek time.

30 In an alternative servo sector layout, track addresses (track numbers) are written twice in each servo sector 68, and the paired track addresses are different from each other. In FIG. 6A, odd track addresses (A1, A3, A5, A7) are written first and even track addresses (A2, A4, A6, A8) are written second, in what appear as radial columns in the figure. In FIG. 6B, the second column records the same track number as does the first,
35 but the second column is recorded with a half-track offset. In both formats, every position of the read head 26 can read an address without interference from an adjacent track in at least one of the two columns. For this reason, Gray coding is not needed and

one can append ECC fields to each address, as shown. In the first format (FIG. 6A), the uncertainty is one track; in the second (FIG. 6B), the uncertainty is half a track. In seeking, one may recognize the column to be read by using a position error signal from the servo bursts which have a period of two tracks. For this use, the servo bursts should be positioned close to the track addresses so that the radial position of the read head 26 does not change significantly from the time the head is reading the servo burst and the time it is reading the track addresses.

Viterbi Detectors for WBP Codes with PR4 Targets

The output at path 49 of adaptive FIR filter 48 is a PR4 (class IV partial response) target, which has a pulse response of $1-D^2$, where D represents one bit cell delay. As shown in FIG. 7, the number of states needed to represent the PR4 target is 4. FIG. 7 shows the Viterbi detector trellis diagram of the PR4 target, with solid lines representing the WBP paths and dotted lines representing the non-WBP paths. All paths are valid PR4 paths. On the trellis, each WBP path is marked with a notation in the form $\pm/w$ where the '+' or '-' refers to the magnetization on the disk (what is written in the cell) and the 'w' represents the waveform sample at the Viterbi detector input. FIG. 7 shows 4 time steps of the detector from the initial state at time k-1, where the detection of a WBP encoded symbol begins, to time k+3, where it ends. The magnet '-' is also shown as a '0' and the magnet '+', as a '1'. Thus, for example, state 00 (reference numeral 80) denotes that the previous two cells were read as '--'.

Turning to the trellis, if the detector is in state 00, reference numeral 80, at time k-1, and the next sample value is 1, the detector goes to state 01, reference numeral 81, at time k. The magnet (or equivalently, the write current) for this branch at time k-1 was '+', a transition from the '-' of state 00, which ideally results in the sample value of 1. Similarly, if the detector is in state 11, reference numeral 83, at time k-1, and the sample value at time k is -1, the detector goes to state 10, reference numeral 82, at time k. The magnet for this branch at time k-1 was '-', a negative transition from the '+' of state 11, which ideally results in the sample value of -1.

Note that since each WBP symbol occupies 4 cells, the detector must be operated knowing where each WBP symbol begins and ends. This 4-cell synchronization will be called chunk synchronization.

Once chunk synchronization is achieved, the trellis can be updated 4 samples at a time, with only two states of the original trellis: 00 and 11. Therefore the 4-state Viterbi detector can be condensed to two states, as shown in FIG. 8A with reference numerals 80 and 83, respectively. In FIG. 8A, only the sample values at the detector input are given with each branch. Note that each sample shown is repeated twice. Thus, the trellis may be simplified by taking the average of every two incoming samples and then processing the resulting stream at half the clock rate. In the simplified trellis, shown in FIG. 8B, the chunks begin at times $k-1$, $k+1$, and $k+3$. (Because of the condensation of states, the time axis k has been scaled by a factor of two.)

A first Viterbi detector, which we will call the difference-metric detector, for WBP codes with PR4 targets will now be described in terms of the states and transitions shown in FIG. 8B.

Let $a0(k-1)$ represent the state of the surviving path at time $k-1$ that ends at time $k+1$ in state 0.

Let $a1(k-1)$ represent the state of the surviving path at time $k-1$ that ends at time $k+1$ in state 1.

Let $y(k)$ denote the received noisy samples after averaging, such as the average of two samples received from FIR filter 48 at output path 49, at time k .

Let $m0(k)$ represent the path metric of state 0 at time k .

Let $m1(k)$ represent the path metric of state 1 at time k .

Let $m(k) = m0(k) - m1(k)$. This is the difference metric.

The decoding algorithm for the difference-metric detector may be expressed in a pseudo-code as follows:

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if (  $m(k-1) - 2y(k) > 1$  ) then
    {  $m(k-1) = 4y(k+1) - 2y(k) - 1$ ;
       $a0(k-1) = a1(k-1) = 1$ ;
      /* both paths merge to state 1 */
    }
else if (  $m(k-1) - 2y(k) < -1$  ) then
    {  $m(k+1) = 4y(k+1) - 2y(k) + 1$ ;
       $a0(k-1) = a1(k-1) = 0$ ;
      /* both paths merge to state 0 */
    }
else
    {  $m(k+1) = -m(k-1) + 4y(k+1)$ ;

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a0(k-1) = 1;
a1(k-1) = 0
/* the paths do not merge */
}

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FIG. 9 is a block diagram showing an implementation of the difference-metric Viterbi detector for WBP codes. Block 84 calculates $a = m(k-1) - 2y(k)$. At block 85, two logical values 0 and 1 (false and true, respectively) are calculated for x and y , as follows: $x = a > 1$, and $y = a < -1$. Block 85 also calculates the values $a0(k+1)$ and $a1(k+1)$, which are the states of the surviving paths at time $k+1$ that end at time $k+3$ in states 0 and 1, respectively. These are provided to a survivor memory 86, and are calculated as shown in FIG. 8, namely:

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a0(k+1) = NOT y, and
a1(k+1) = x.

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Block 86 implements a standard Viterbi detector survivor memory whose output 86a is the output of the detector. The depth of the survivor memory will be selected to meet the detector's performance requirements; for the uses described here, a depth of at least 1 would generally be sufficient.

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A value z for use in the difference metric calculation is calculated in block 87, as follows:

```

if (x,y) == (1,0) z = -2y(k) - 1;
if (x,y) == (0,1) z = -2y(k) + 1;
otherwise          z = -m(k-1).

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Block 88 uses this calculated value z to output $m(k+1)$, calculated as follows:

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m(k+1) = 4y(k+1) + z.

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This output 88a is delayed in register 89 by $4T$ (a WBP symbol time) and the output 89a of the register is the input value $m(k-1)$ to block 87. (The initial value of $m(k-1)$ at $k=0$ is 0.)

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A second Viterbi detector, which we will call the tree-search detector, for WBP codes will now be described in terms of the states and transitions shown in FIG. 8B. The tree-search detector must be forced to begin at an initial state, since it is assumed that the two survivor paths merge at time $k-1$. The surviving paths at time $k+1$ are then detected from:

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$a(k-1)$, which represents the merged surviving path at time $k-1$, and

$y(k)$, $Y(k+1)$, $Y(k+2)$, and $Y(k+3)$, equalized and averaged samples as produced, for example, at output 49 of FIR filter 48.

In the context of servo sector fields the requirement that the tree-search detector start in a known state is reasonable, since the state can be forced, for example, by a known fields
 5 such as the preamble field 732.

The decoding algorithm for the tree-search detector may be expressed in a pseudo-code as follows:

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    metric1 = y(k) - 2y(k+1) + y(k+2)
    10 metric2 = y(k) - 2y(k+1) + 2y(k+3);
    if ( a(k-1) == 0 ) then
        a(k+1) = ( metric1 < 0 ) OR
                (( metric1 < 1 ) AND ( metric2 < 0.5 ))
    else
    15 a(k+1) = ( metric1 < -1 ) OR
        (( metric1 < 0 ) AND ( metric2 < -0.5 ));
  
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As above, in these calculations a logical false is an arithmetic 0, and a logical true, an arithmetic 1.

20 FIG. 10 is a block diagram showing an implementation of the tree-search Viterbi detector for WBP codes. Blocks 91 and 92 calculate metric1 and metric2, respectively, as defined above. At inputs 90a and 90b, block 90 receives samples $y(k+1)$ and $y(k)$, respectively, and from them calculates $y(k) - 2y(k+1)$. This is provided at inputs 91b of block 91 and 92a of block 92. At input 91a block 91 also receives sample $y(k+1)$ and at
 25 input 92b block 92 receives sample $y(k+3)$. Metric 1 is output at path 91c to block 93. Metric2 is output at path 92c to block 93. Block 93 calculates $a(k+1)$, output at path 93a, as set forth in the above pseudo-code, from metric1, metric2, and $a(k-1)$. The output 93a of block 93 is the input to 4T delay register 94, which provides $a(k-1)$ to block 93 on path 94a.

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Viterbi Detectors for WBP with EPR4 Targets

Turning to FIG. 11, we consider the implementation of a Viterbi detector that detects EPR4 targets that are WBP encoded. The EPR4 target has a pulse response of
 35 $1+D-D2-D3$. The number of states needed to represent the EPR4 target is 8. FIG. 11 is a trellis diagram of an EPR4 channel with wide bi-phase paths highlighted. This diagram

parallels the diagram for a PR4 channel found in FIG. 6, with the difference that there are 8 states and 5 possible sample inputs: -4, -2, 0, 2, and 4.

Turning to FIG. 12A, once chunk synchronization is achieved, the EPR4 trellis can be updated 4 samples at a time with only 2 of the states of the original trellis. The original states 100 and 011 are renamed to 0 and 1, respectively, in FIG. 12A, and only the sample values at the Viterbi detector input are shown on the branches. The trellis diagram may be further simplified, as shown in FIG. 12B, by dividing the incoming sample values by 2.

As with the simplified trellis of FIG. 8B, we now describe two Viterbi detectors, based on FIG. 12B, for WBP codes with EPR4 targets.

The first detector, a difference-metric detector, substantially parallels the difference-metric detector described in connection with FIG. 9.

Let $a_0(k-1)$ represent the state of the surviving path at time $k-1$ that ends at time $k+3$ in state 0.

Let $a_1(k-1)$ represent the state of the surviving path at time $k-1$ that ends at time $k+3$ in state 1.

Let $y(k)$ denote the received noisy samples, such as the average of two samples received from FIR filter 48 at output path 49, at time k , after scaling to ideal values -2, -1, 0, 1, and 2.

Let $m_0(k)$ represent the path metric of state 0 at time k .

Let $M_1(k)$ represent the path metric of state 1 at time k .

Let $m(k) = m_0(k) - m_1(k)$. This is the difference metric.

The decoding algorithm for the difference-metric detector may be expressed in a pseudo-code as follows:

```

    thr(k-1) = m(k-1) - 2y(k-1) - 4y(k-2) + 2y(k-3);
    if ( thr(k-1) > 2 ) then
        { m(k+3) = 8y(k) + 2y(k-1) - 4y(k-2) - 2y(k-3)
          -2;
          a0(k-1) = a1(k-1) = 1;
          /* both paths merge to state 1 */
        }
    else if ( thr(k-1) < -2 ) then
        { m(k+3) = 8y(k) + 2y(k-1) - 4y(k-2) - 2y(k-3) + 2;

```

```

        a0(k-1) = a1(k-1) = 0;
        /* both paths merge to state 0 */
    else
        { m(k+3) = - m(k-1) + 8y(k) + 4y(k-1) - 4y(k-3);
          a0(k-1) = 1;
          a1(k-1) = 0
        }
        /* the paths do not merge */
    }

```

As with the difference-metric Viterbi detector for WBP with PR4 targets, a survivor memory depth of 3 would generally be sufficient for the uses described here.

The second, tree-search Viterbi detector for WBP codes with EPR4 targets will now be described. In describing the tree-search detector, it is assumed that the two survivor paths merge at time k-1. The surviving paths at time k+3 are then detected from: a(k-1), which represents the merged surviving path at time k-1; and y(k), y(k-1) . . . y(k-7), equalized and averaged samples as produced, for example, as the output of 1+D filter 50.

The decoding algorithm for the tree-search detector may be expressed in a pseudo-code as follows:

```

    metric1 = 2y(k-1) + 4y(k-2) - 2y(k-3) - 8y(k-4) - 2y(k-5) + 4y(k-6) +
    2y(k-7);
    metric2 = 8y(k) - 4y(k-1) + 4y(k-3) - 8y(k-4) - 2y(k-5) + 4y(k-6) +
    2y(k-7);
    if ( a(k-1) == 0 ) then
        a(k+3) = ( metric1 < 0 ) OR
        (( metric1 < 4 ) AND ( metric2 < 2 ))
    else
        a(k-3) = ( metric1 < -4 ) OR
        (( metric1 < 0 ) AND ( metric2 < -2 ));

```

As with the tree-search detector for WBP with PR4 targets, this detector for EPR4 targets has no survivor memory.

Returning to FIG. 1, a Viterbi detector 60 for PRML detection of WBP codes with EPR4 targets can be used to detect all WBP-encoded digital information in the servo sector, such as track number, head number, and sector number. Viterbi detector 60 may be a difference-metric detector or a tree search detector, as described above in connection with FIGS. 11, 12A, and 12B, or a conventional Viterbi detector. Alternatively, in place

of an EPR4 detector, WBP-encoded data in the servo sector may be decoded by a Viterbi detector for WBP codes with PR4 targets, such as the difference-metric detector or the tree-search detector described above in connection with FIGS. 7, 8A, 8B, 9, and 10, or by a conventional Viterbi detector.

5

In FIG. 1 a digital servo burst detector 54 also receives the EPR4 target output signal from 1+D filter 50. Alternatively, burst detector 54 may receive a PR4 target from FIR filter 48, where burst formats are used that can be detected with a PR4 target.

10

Turning to FIG. 13A-13E, five servo burst formats will be described. The centers of the data tracks are indicated by TK0, TK1, TK2, and TK3. The bursts in each format repeat with a period of two tracks. The first format, which we will call the type I format, i.e. full track bursts, is illustrated diagrammatically in FIG. 13A. The type I bursts A, B, and C (and, optionally, D) are written to be the width of a data track. Because the write head is less than this wide, the bursts are written in at least two passes and at least one erase band (not shown) will be found within each burst. There is also an erase band (not shown), for example, between burst A and burst C, that runs along TK1.

15

The second format, which we will call the type II format, i.e. narrow bursts, is illustrated diagrammatically in FIG. 13B. In this format, each burst, E, F, G, and H, is written only once; thus there is no erase band within the burst. The distance between radially adjacent bursts (such as E and F) is half a track width. The write head will generally exceed this width, so each burst will normally extend over one track center.

20

In both type I and type II formats, the bursts themselves are normally sinusoids of constant frequency and amplitude.

25

The third format, which we will call the antipodal format, is illustrated diagrammatically in FIG. 13C. In this format, the bursts --J, K, L, and M-- are written to fill the space left blank, for example, between the A and B bursts in the type I format (FIG. 13A). The unrecorded areas are filled with a sinusoidal waveform of opposite (or antipodal) polarity. Thus, if the signal in burst J is $\sin(x)$, the signal in burst K is $-\sin(x)$. The waveforms in bursts L and M correspond to those of bursts J and K.

30

Unlike the situation with type I and type II, phase information is important in the antipodal format. Thus, the PLL is locked while reading this burst format, so as not to "correct" the phase information. For the same reason, this format is subject to errors

35

arising from the erase band within the bursts, radial phase incoherence, and accumulated phase error. To allow the disk drive to limit the effect of such errors, an optional resynchronization pattern (not shown) may be recorded before bursts themselves.

5 The fourth format, which we will call the compressed format, is illustrated diagrammatically in FIG. 13D. This format is like type I in form, with the difference that, unlike the situation with the other formats, in compressed format the servo information is written on spoke tracks SPOKE TK0, SPOKE TK1, SPOKE TK2, and SPOKE TK3 that do not correspond to the data tracks, which here are denoted DATA TK0, DATA TK1, and DATA TK2. Each burst P, Q, and R is written only once; thus there is no erase band within the bursts and the bursts are nevertheless the full width of the servo track. Note that with this format, in tracking an odd numbered data track, such as track DATA TK1, the disk drive will not be following a servo track center. In fact, the head will ideally be placed exactly between two servo tracks, and the two-track periodicity of the burst format must be used to resolve the track number ambiguity between the Gray coded numbers received from spoke tracks SPOKE TK1 and SPOKE TK2 while tracking data track DATA TK1, for example.

20 The fifth format, which we will call the frequency format, is illustrated diagrammatically in FIG. 13E. In this format, unlike the ones previously described, the burst waveforms are not all recorded at one frequency. As with the antipodal format, frequency format bursts are recorded across the full radial width of the half tracks. As illustrated in FIG. 14E, the radial sequence of bursts S, T, U, and V are recorded as sinusoids with angular frequencies w_1 and w_2 , so that the form of the sequence of bursts is: S is $\sin w_1 t$; T is $\sin w_2 t$; U is $-\sin w_1 t$, and V is $-\sin w_2 t$. The two frequencies must be different and should be selected to have no intersecting harmonics.

30 Turning to FIGS. 14A-14B, burst detector 54 will take different forms depending on the format in which the servo bursts are recorded. Turning to FIG. 14A, burst detector 541 is useful for synchronous formats such as the antipodal format and the frequency format. Multiplier 542 multiplies the EPR4 sample waveforms by a sine wave 1 0 -1 0. The result is accumulated by adder 543 in register 544. The output of the detector from register 544 represents the signed amplitude of the (generally) composite signal produced by two radially adjacent bursts, such as bursts K and J of FIG. 13C.

35 This output will ideally be zero when the read head is exactly between the two bursts and on, for example, the track TK1.



Turning to FIG. 14B, burst detector 55 is useful non-synchronous burst formats such as the type I, the type II, and the compressed formats. Burst detector 55 calculates an phase-amplitude vector of the burst signal by multiplying the EPR4 sample waveforms by two orthogonal sine waves with a phase offset of 90° ; the first sine wave 1 0 -1 0 is used in multiplier 551, adder 552, and accumulating register 553; the second, orthogonal, sine wave 0 -1 0 1 is used in multiplier 554, adder 555, and accumulating register 556. The result of this process is a phase-amplitude vector whose real part is in register 553 and whose imaginary art is in register 556. When the burst has been read, the energy of the burst is calculated as the square root, circuit 560 of the sum, adder 559, of the squares of the real part, circuit 557, and the imaginary part, circuit 558, of the phase-amplitude vector. This calculated energy estimates the degree of overlap between the burst and the read head and is used later to estimate the head position with respect to the repeating two-track burst pattern. (Note than in the non-synchronous type I, type II, and compressed burst formats under consideration, no two bursts are radially adjacent, so the burst detector will have only one burst to process at a time.)

Two alternative burst detectors for the frequency format will now be described. The first alternative operates as a pair of the burst detectors 541 illustrated in FIG. 14A. The sine wave input to the first detector of the pair has as input to multiplier 542 a sine wave with an angular frequency of w_1 ; the sine wave input to the second detector's multiplier 542 has an angular frequency of w_2 . The output of each detector is the signed amplitude of the burst signal at the corresponding angular frequency, and these signed amplitudes are compared to estimate the position of the read head.

The second alternative burst detector for the frequency format, unlike the first alternative just described, is not sensitive to radial phase incoherence or phase error. The second alternative duplicates the operation of a pair of the burst detectors 55 illustrated in FIG. 14B. The sine wave input to multipliers 551 and 554 in the first of the pair of detectors has an angular frequency of w_1 ; the sine wave inputs for the second detector's multipliers 551 and 554 have an angular frequency of w_2 . The outputs of the two detectors, each of which estimate the signed amplitude of the burst signal at the corresponding frequency, are compared to estimate the position of the read head.

A further alternative burst detector and associated synchronous servo burst pattern is described in the referenced U.S. Patent Application Serial No. 08/320,540 filed October 12, 1994, by Fisher et al., entitled: "Synchronous Detection of Concurrent Servo



Bursts for Fine Head Position in Disk Drive", the disclosure thereof being incorporated herein by reference.

5 Having thus described presently preferred embodiments of the invention, it will now be appreciated that the objects of the invention have been fully achieved, and it will be understood by those skilled in the art that many changes in construction and widely differing embodiments and applications of the invention will suggest themselves without departing from the spirit and scope of the invention. The disclosure and the description herein are purely illustrative and are not intended to be in any sense limiting.



What is claimed is:

1. A disk drive comprising:
 - at least one rotating data storage disk, the disk having a major surface defining recording tracks divided into data sectors by narrow servo spokes,
 - 5 a data sector of a recording track for recording with user data encoded in accordance with a code having a predetermined distance and user data code rate,
 - a servo spoke of the recording area having at least one servo information field coded in a wide biphasic pattern at a servo code rate which is one fourth the user data code rate,
 - 10 a synchronous sampling data detection channel including:
 - a data transducer head positioned by a servo-controlled actuator over the recording track,
 - a preamplifier for receiving electrical analog signals magnetically induced by the data transducer head from flux transitions present in at least the servo information
 - 15 field,
 - a digital sampler for synchronously sampling the electrical analog signals to produce digital samples, and
 - a Viterbi detector coupled to receive digital samples from the synchronous sampling data detection channel for decoding the coded wide biphasic pattern as a
 - 20 maximum likelihood servo data sequence.
2. The disk drive set forth in claim 1 wherein the Viterbi detector comprises a difference metric detector.
- 25 3. The disk drive set forth in claim 2 wherein the difference metric Viterbi detector comprises:
 - a difference circuit connected to subtract two times a present wide biphasic encoded servo information sample received from the channel from a difference metric to produce a difference value,
 - 30 a first calculator connected to receive the difference value for calculating a plurality of logical values, for calculating a first state of surviving path, and for calculating a state of a second surviving path,
 - a survivor memory unit connected to the first calculator to receive the first and second states and having a predetermined path length for putting out detected servo
 - 35 information,





a difference metric calculator connected to the first calculator to receive the plurality of logical values, the difference metric and the present sample, for calculating a present difference metric value, and
 a delay register for receiving and delaying the present difference metric value by a wide biphasic clock interval to produce the difference metric.

4. The disk drive set forth in claim 2 wherein the difference metric Viterbi detector comprises:
- a difference circuit connected to subtract two times a present wide biphasic encoded servo information sample $y(k)$ received from the channel from a difference metric $m(k-1)$ to produce a difference value a ,
- a first calculator connected to receive the difference value a for calculating logical values 0 and 1 for x and y , in accordance with $x = a > 1$ and $y = a < 1$ and for calculating a state of surviving path at time $K+1$ that ends at time $k+3$ in state 0 as $a0(k+1) = \text{NOT } y$, and for calculating a state of surviving path at time $k+1$ that ends at time $k+3$ in state 1 as $a1(k+1) = x$,
- a survivor memory unit connected to the first calculator to receive states $a0(k+1)$ and $a1(k+1)$ and having a predetermined path length for putting out detected servo information,
- a raw difference metric calculator connected to the first calculator to receive x and y , and connected to receive the difference metric $m(k-1)$ and the present sample $y(k)$ for calculating a raw difference metric z in accordance with:
- | | |
|---------------------------|--------------------|
| if $(x,y) = (1,0)$, then | $z = -2y(k) - 1$, |
| if $(x,y) = (0,1)$, then | $z = -2y(k) + 1$, |
| otherwise | $z = -m(k-1)$, |
- an intermediate difference metric calculator connected to receive the raw difference metric z and to receive a time adjusted sample $y(k+1)$ for calculating a present difference metric $m(k+1) = 4y(k+1) + z$, and
- a delay register for receiving and delaying the present difference metric $m(k+1)$ by a wide biphasic clock interval to produce the difference metric $m(k-1)$.

5. The disk drive set forth in claim 4 wherein the synchronous sampling data detection channel includes a finite impulse response filter adjusted to a partial response, class IV, target spectrum and wherein the difference circuit is connected to receive equalized digital samples from an output of the finite impulse response filter.





6. The disk drive set forth in claim 2 wherein the channel is equalized to an EPR4 target spectrum, and wherein the Viterbi detector detects the wide biphas encoded servo information in accordance with

```

thr(k-1) = m(k-1) - 2y(k-1) - 4y(k-2) + 2y(k-3);
5   if ( thr(k-1) > 2 ) then
      { m(k+3) = 8y(k) + 2y(k-1) - 4y(k-2) - 2y(k-3)
        -2;
          a0(k-1) = a1(k-1) = 1;
          /* both paths merge to state 1 */
10      }
      else if ( thr(k-1) < -2 ) then
          { m(k+3) = 8y(k) + 2y(k-1) - 4y(k-2) - 2y(k-3) + 2;
            a0(k-1) = a1(k-1) = 0;
            /* both paths merge to state 0 */
15      }
      else
          { m(k+3) = - m(k-1) + 8y(k) + 4y(k-1) - 4y(k-3);
            a0(k-1) = 1;
            a1(k-1) = 0
20          /* the paths do not merge */
          },

```

where $a0(k-1)$ represents a state of a surviving path at time $k-1$ that ends at time $k+3$ in a state 0; $a1(k-1)$ represents a state of a surviving path at time $k-1$ that ends at a time $k+3$ in a state 1; $y(k)$ denotes a received noisy samples, such as the average of two samples at time k , after having been scaled to ideal values -2, -1, 0, 1, and 2; $m0(k)$ represents a path metric of state 0 at time k ; $M1(k)$ represents a path metric of state 1 at time k ; and, $m(k) = m0(k) - m1(k)$, the difference metric.

7. The disk drive set forth in claim 1 wherein the Viterbi detector is a tree-search detector.

8. The disk drive set forth in claim 7 wherein the tree-search Viterbi detector comprises:

a difference circuit connected to the channel to receive and subtract two times a one unit time adjusted wide biphas encoded servo information sample $y(k+1)$ from a present sample $y(k)$ to produce a difference value a ,



a first metric calculator connected to receive the difference value a and a two-unit time adjusted sample $y(k+2)$ for calculating and putting out a first metric $1 = y(k) - 2y(k+1) + y(k+2)$,

5 a second metric calculator connected to receive the difference value a and a three-unit time adjusted sample $y(k+3)$ for calculating and putting out a second metric $2 = y(k) - 2y(k+1) + 2y(k+3)$, and

a tree-search calculator for receiving the metric1, metric2 and a detector output value $a(k-1)$, for calculating an intermediate value $a(k+1)$ in accordance with:

10 if ($a(k-1) = 0$), then
 $a(k+1) = (\text{metric } 1 < 0) \text{ OR } ((\text{metric } 1 < 1) \& (\text{metric } 2 < 0.5))$,
 else
 $a(k+1) = (\text{metric } 1 < 1) \text{ or } ((\text{metric } 1 < 0) \& (\text{metric } 2 < -0.5))$, and
 15 a delay register for receiving and delaying the intermediate value $a(k+1)$ by a wide biphas clock interval to produce the detector output value $a(k-1)$.

20 9. The disk drive set forth in claim 7 wherein the synchronous sampling data detection channel includes a finite impulse response filter adjusted to a partial response, class IV, target spectrum and wherein the difference circuit is connected to receive equalized digital samples from an output of the finite impulse response filter.

25 10. The disk drive set forth in claim 1 wherein the synchronous sampling data detection channel includes a finite impulse response filter for filtering digital samples in accordance with a $1-D^2$ pulse response (partial response, class IV) where D represents a one bit cell delay, and a $1+D$ filter connected downstream of the finite impulse response filter to provide digital samples filtered in accordance with a $1+D-D^2-D^3$ pulse response (EPR4), and wherein the Viterbi detector is connected to receive EPR4 equalized wide biphas samples from an output of the $1+D$ filter.

30 11. The disk drive set forth in claim 10 wherein the Viterbi detector detects surviving paths at a time $k+3$ in accordance with steps comprising:

metric1 = $2y(k-1) + 4y(k-2) - 2y(k-3) - 8y(k-4) - 2y(k-5) + 4y(k-6) + 2y(k-7)$;
 35 metric2 = $8y(k) - 4y(k-1) + 4y(k-3) - 8y(k-4) - 2y(k-5) + 4y(k-6) + 2y(k-7)$;
 if ($a(k-1) == 0$) then





$a(k+3) = (\text{metric1} < 0) \text{ OR}$
 $((\text{metric1} < 4) \text{ AND } (\text{metric2} < 2))$

else

$a(k-3) = (\text{metric1} < -4) \text{ OR}$
 $((\text{metric1} < 0) \text{ AND } (\text{metric2} < -2));$

where $a(k-1)$, which represents the merged surviving path at time $k-1$; and
 $y(k), y(k-1) \dots y(k-7)$, represent equalized and averaged wide biphase encoded servo
information samples.

10

12. The disk drive set forth in claim 1 wherein the servo spoke includes plural
servo information fields encoded in wide biphase.

15

13. The disk drive set forth in claim 1 wherein the wide biphase magnet patterns
recorded in the plural servo information fields are $--++$ for a binary zero information value
and $--++$ for a binary one information value.

20

14. The disk drive set forth in claim 13 wherein one of the plural servo
information fields comprises a servo address mark pattern.

15. The disk drive set forth in claim 14 wherein the servo address mark pattern is
a nine-symbol word 000100101 (binary) for marking the beginning of a servo block.

25

16. The disk drive set forth in claim 1 wherein the at least one servo information
field comprises a track number binary pattern of predetermined bit length, the pattern
being decoded as a wide biphase code and then decoded as a Gray code with a code rate of
one.

30

17. The disk drive set forth in claim 16 wherein the track number binary pattern
includes a parity symbol, and further comprising means for receiving and decoding the
track number binary pattern and checking the parity symbol.

35

18. The disk drive set forth in claim 1 wherein the at least one servo information
field comprises two track number binary patterns of predetermined bit length, a first track
number being an address of the track, and a second track number being an address of a
second track adjacent the track.





19. The disk drive set forth in claim 18 wherein the second track number is recorded with a one-half track offset extending into the second track.

5 20. The disk drive set forth in claim 19 wherein the at least one servo information field further comprises error correction code values calculated with respect to the first and second track numbers, and further comprising error correction code decoding and correcting circuitry coupled to the synchronous sampling data detection channel for decoding, checking and correcting the decoded values of the first and second track numbers.

10

21. A disk drive comprising:

at least one rotating data storage disk, the disk having a major surface defining recording tracks divided into data sectors by narrow servo spokes,

15 a data sector of a recording track for recording with user data encoded in accordance with a code having a predetermined distance and user data code rate,

a servo spoke of the recording area having at least one preamble field and at least one servo information field coded in a wide biphase pattern at a servo code rate which is one fourth the user data code rate,

a synchronous sampling data detection channel including:

20 a data transducer head positioned by a servo-controlled actuator over the recording track,

a preamplifier for receiving electrical analog signals magnetically induced by the data transducer head from flux transitions present in at least the servo information field,

25 a digital sampler for synchronously sampling the electrical analog signals to produce digital samples,

a partial response filter for filtering the digital samples to a partial response class IV target spectrum to produce PR4 samples,

30 a 1+D filter, D being a unit delay operator, connected to filter the PR4 samples to EPR4 target samples, and

a wide biphase Viterbi detector connected to receive and decode the EPR4 target samples taken from the servo information field as most likely servo information binary values.

35 22. A difference metric Viterbi detector for detecting wide biphase encoded servo information within a partial response, class IV, synchronous sampling data detection channel, the detector comprising:





a difference circuit connected to subtract two times a present wide biphas encoded servo information sample $y(k)$ received from the channel from a difference metric $m(k-1)$ to produce a difference value a ,

5 a first calculator connected to receive the difference value a for calculating logical values 0 and 1 for x and y , in accordance with $x = a > 1$ and $y = a < 1$ and for calculating a state of surviving path at time $K+1$ that ends at time $k+3$ in state 0 as $a0(k+1) = \text{NOT } y$, and for calculating a state of surviving path at time $k+1$ that ends at time $k+3$ in state 1 as $a1(k+1) = x$,

10 a survivor memory unit connected to the first calculator to receive states $a0(k+1)$ and $a1(k+1)$ and having a predetermined path length for putting out detected servo information,

a raw difference metric calculator connected to the first calculator to receive x and y , and connected to receive the difference metric $m(k-1)$ and the present sample $y(k)$ for calculating a raw difference metric z in accordance with:

15 if $(x,y) = (1,0)$, then $z = -2y(k) - 1$,
if $(x,y) = (0,1)$, then $z = -2y(k) + 1$,
otherwise $z = -m(k-1)$,

an intermediate difference metric calculator connected to receive the raw difference metric z and to receive a time adjusted sample $y(k+1)$ for calculating a present difference metric $m(k+1) = 4y(k+1) + z$, and

20 a delay register for receiving and delaying the present difference metric $m(k+1)$ by a wide biphas clock interval to produce the difference metric $m(k-1)$.

23. The difference metric Viterbi detector set forth in claim 22 wherein the
25 channel includes a finite impulse response filter adjusted to a partial response, class IV, target spectrum and wherein the difference circuit is connected to receive samples from an output of the finite impulse response filter.

24. A tree-search Viterbi detector for detecting wide biphas encoded servo
30 information within a partial response, class IV, synchronous sampling data detection channel, the detector comprising:

a difference circuit connected to the channel to receive and subtract two times a one unit time adjusted wide biphas encoded servo information sample $y(k+1)$ from a present sample $y(k)$ to produce a difference value a ,

35 a first metric calculator connected to receive the difference value a and a two-unit time adjusted sample $y(k+2)$ for calculating and putting out a first metric $1 = y(k) - 2y(k+1) + y(k+2)$,





a second metric calculator connected to receive the difference value a and a three-unit time adjusted sample $y(k+3)$ for calculating and putting out a second metric $2 = y(k) - 2y(k+1) + 2y(k+3)$, and

- 5 a tree-search calculator for receiving the metric1, metric2 and a detector output value $a(k-1)$, for calculating an intermediate value $a(k+1)$ in accordance with:

if $(a(k-1) = 0)$, then

$a(k+1) = (\text{metric1} < 0)$ OR
 $((\text{metric1} < 1) \& (\text{metric2} < 0.5))$,

else

- 10 $a(k+1) = (\text{metric1} < 1)$ or
 $((\text{metric1} < 0) \& (\text{metric2} < -0.5))$, and

a delay register for receiving and delaying the intermediate value $a(k+1)$ by a wide biphas clock interval to produce the detector output value $a(k-1)$.

- 15 25. The tree-search Viterbi detector set forth in claim 21 wherein the channel includes a finite impulse response filter adjusted to a partial response, class IV, target spectrum and wherein the difference circuit is connected to receive samples from an output of the finite impulse response filter.

- 20 26. A difference metric Viterbi detector for detecting wide biphas encoded servo information within a partial response synchronous sampling data detection channel, the detector comprising:

- 25 a difference circuit connected to subtract two times a present wide biphas encoded servo information sample received from the channel from a difference metric to produce a difference value,

a first calculator connected to receive the difference value for calculating a plurality of logical values, for calculating a first state of surviving path, and for calculating a state of a second surviving path,

- 30 a survivor memory unit connected to the first calculator to receive the first and second states and having a predetermined path length for putting out detected servo information,

a difference metric calculator connected to the first calculator to receive the plurality of logical values, the difference metric and the present sample, for calculating a present difference metric value, and

- 35 a delay register for receiving and delaying the present difference metric value by a wide biphas clock interval to produce the difference metric.





27. A difference metric Viterbi detector for detecting wide biphas encoded servo information within a partial response synchronous sampling data detection channel equalized to an EPR4 target spectrum, the detector for detecting the wide biphas encoded servo information in accordance with:

```

5      thr(k-1) = m(k-1) - 2y(k-1) - 4y(k-2) + 2y(k-3);
      if ( thr(k-1) > 2 ) then
          { m(k+3) = 8y(k) + 2y(k-1) - 4y(k-2) - 2y(k-3)
            -2;
              a0(k-1) = a1(k-1) = 1;
10          /* both paths merge to state 1 */
              }
      else if ( thr(k-1) < -2 ) then
          { m(k+3) = 8y(k) + 2y(k-1) - 4y(k-2) - 2y(k-3) + 2;
            a0(k-1) = a1(k-1) = 0;
15          /* both paths merge to state 0 */
      else
          { m(k+3) = - m(k-1) + 8y(k) + 4y(k-1) - 4y(k-3);
            a0(k-1) = 1;
            a1(k-1) = 0
20          /* the paths do not merge */
          },

```

where $a0(k-1)$ represents a state of a surviving path at time $k-1$ that ends at time $k+3$ in a state 0; $a1(k-1)$ represents a state of a surviving path at time $k-1$ that ends at a time $k+3$ in a state 1; $y(k)$ denotes a received noisy samples, such as the average of two samples at
25 time k , after having been scaled to ideal values $-2, -1, 0, 1$, and 2 ; $m0(k)$ represents a path metric of state 0 at time k ; $M1(k)$ represents a path metric of state 1 at time k ; and, $m(k) = m0(k) - m1(k)$, the difference metric.

28. A tree-search Viterbi detector for detecting wide biphas encoded servo
30 information within a partial response synchronous sampling data detection channel equalized to an EPR4 target spectrum, the detector for detecting the wide biphas encoded servo information wherein two survivor paths merge at a time $k-1$, and wherein surviving paths at a time $k+3$ are detected in accordance with steps comprising:

```

      metric1 = 2y(k-1) + 4y(k-2) - 2y(k-3) - 8y(k-4) - 2y(k-5) + 4y(k-6) +
35 2y(k-7);
      metric2 = 8y(k) - 4y(k-1) + 4y(k-3) - 8y(k-4) - 2y(k-5) + 4y(k-6) +
2y(k-7);

```





if ($a(k-1) == 0$) then
 $a(k+3) = (\text{metric1} < 0)$ OR
 $((\text{metric1} < 4) \text{ AND } (\text{metric2} < 2))$

else

5 $a(k-3) = (\text{metric1} < -4)$ OR
 $((\text{metric1} < 0) \text{ AND } (\text{metric2} < -2))$;

where $a(k-1)$, which represents the merged surviving path at time $k-1$; and
 $y(k)$, $y(k-1) \dots y(k-7)$, represent equalized and averaged wide biphas encoded servo
information samples.

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