DESCRIPTION

Title Of Invention: APPARATUS AND METHODS FOR BIASING OF LOW NOISE AMPLIFIERS

BACKGROUND

Technical Field

[0001] Embodiments of the invention relate to electronic systems, and in particular, to radio frequency (RF) electronics.

Description of Related Technology

[0002] A low noise amplifier (LNA) can be used to boost the amplitude of a relatively weak radio frequency (RF) signal received via an antenna. Thereafter, the boosted RF signal can be used for a variety of purposes, including, for example, driving a switch, a mixer, and/or a filter in an RF communication system.

[0003] Examples of RF communication systems with one or more LNAs include, but are not limited to, mobile phones, tablets, base stations, network access points, customer-premises equipment (CPE), laptops, and wearable electronics.

[0004] LNAs can be included in RF communication systems to amplify signals of a wide range of frequencies. For example, an LNA can be used to provide low noise amplification to RF signals in a frequency range of about 30 kHz to 300 GHz, such as in the range of about 400 MHz to about 7.125 GHz for Frequency Range 1 (FR1) of the Fifth Generation (5G) communication standard or in the range of about 24.250 GHz to about 71.000 GHz for Frequency Range 2 (FR2) of the 5G communication standard.

SUMMARY

[0005] In certain aspect, the present disclosure relates to a mobile device. The mobile device includes an antenna and a front-end system that includes a low noise amplifier including at least one amplification transistor configured to amplify a radio frequency input signal received from the antenna, and a biasing circuit including a current bias circuit configured to generate a bias current based on a reference current and a voltage bias circuit configured to generate at least one input bias voltage for the at least one amplification transistor

based on the bias current. The current bias circuit includes a first bias transistor configured to receive the reference current, a second bias transistor configured to generate the bias current, and an amplifier configured to control a first bias voltage of the first bias transistor to match a second bias voltage of the second bias transistor.

[0006] In various examples, the current bias circuit further includes a plurality of selection switches and a plurality of current mirroring transistors each selectable by a corresponding one of the plurality of selection switches, the plurality of current mirroring transistors biased by the second bias voltage.

[0007] In several examples, the first bias transistor includes a drain connected to a first input of the amplifier and a gate connected to an output of the amplifier, and the second bias transistor includes a drain connected to a second input of the amplifier and a gate connected to the output of the amplifier.

[0008] In some examples, the at least one amplification transistor includes a common source transistor, and the at least one input bias voltage includes a gate bias voltage for the common source transistor. According to a number of examples, the biasing circuit includes a bias resistor and a bias resistor bypass switch, the voltage bias circuit configured to provide the gate bias voltage to a gate of the common source transistor through a parallel combination of the bias resistor and the bias resistor bypass switch. In accordance with various examples, the at least one amplification transistor further includes a cascode transistor in series with the common source transistor, and the at least one input bias voltage further includes a cascode bias voltage for the cascode transistor.

[0009] In several examples, the front-end systems further includes a controllable current source configured to generate the reference current, the controllable current source configured to control the reference current based on a gain control signal.

[0010] In various examples, the voltage bias circuit further includes a first voltage bias transistor and a resistor in series between a supply voltage and a ground voltage, and a second voltage bias transistor and a third voltage bias transistor in series between a gate of the first voltage bias transistor and the ground voltage. According to a number of examples, the voltage bias circuit is configured to generate a first input bias voltage of the at least one input bias voltage based on a voltage across the resistor, and to generate a second

input bias voltage of the at least one input bias voltage based on a gate voltage of the second voltage bias transistor.

[0011] In certain aspect, the present disclosure relates to a low noise amplifier includes at least one amplification transistor configured to amplify a radio frequency input signal, and a biasing circuit including a current bias circuit configured to generate a bias current based on a reference current and a voltage bias circuit configured to generate at least one input bias voltage for the at least one amplification transistor based on the bias current. The current bias circuit including a first bias transistor configured to receive the reference current, a second bias transistor configured to generate the bias current, and an amplifier configured to control a first bias voltage of the first bias transistor to match a second bias voltage of the second bias transistor.

[0012] In various examples, the current bias circuit further includes a plurality of selection switches and a plurality of current mirroring transistors each selectable by a corresponding one of the plurality of selection switches, the plurality of current mirroring transistors biased by the second bias voltage.

[0013] In several examples, the first bias transistor includes a drain connected to a first input of the amplifier and a gate connected to an output of the amplifier, and the second bias transistor includes a drain connected to a second input of the amplifier and a gate connected to the output of the amplifier.

[0014] In some examples, the at least one amplification transistor includes a common source transistor, and the at least one input bias voltage includes a gate bias voltage for the common source transistor. According to a number of examples, the biasing circuit includes a bias resistor and a bias resistor bypass switch, the voltage bias circuit configured to provide the gate bias voltage to a gate of the common source transistor through a parallel combination of the bias resistor and the bias resistor bypass switch. In accordance with several examples, the at least one amplification transistor further includes a cascode transistor in series with the common source transistor, and the at least one input bias voltage further includes a cascode bias voltage for the cascode transistor.

[0015] In various examples, the low noise amplifier further includes a controllable current source configured to generate the reference current, the controllable current source configured to control the reference current based on a gain control signal.

[0016] In several examples, the voltage bias circuit includes a first voltage bias transistor and a resistor in series between a supply voltage and a ground voltage, and a second voltage bias transistor and a third voltage bias transistor in series between a gate of the first voltage bias transistor and the ground voltage. According to a number of examples, the voltage bias circuit is configured to generate a first input bias voltage of the at least one input bias voltage based on a voltage across the resistor, and to generate a second input bias voltage of the at least one input bias voltage based on a gate voltage of the second voltage bias transistor.

[0017] In certain aspect, the present disclosure relates to a method of radio frequency signal amplification. The method includes amplifying a radio frequency input signal using at least one amplification transistor of a low noise amplifier, generating at least one input bias voltage for the at least one amplification transistor based on a bias current using a voltage bias circuit of the low noise amplifier, and generating the bias current based on a reference current using a current bias circuit of the low noise amplifier, including receiving the reference current using a first bias transistor, generating the bias current using a second bias transistor, and controlling a first bias voltage of the first bias transistor to match a second bias voltage of the second bias transistor using an amplifier.

[0018] In some examples, controlling the first bias voltage of the first bias transistor to match the second bias voltage of the second bias transistor includes controlling a drain-to-source voltage of the first bias transistor to substantially equal a drain-to-source voltage of the second bias transistor.

[0019] In several examples, generating the at least one input bias voltage for the at least one amplification transistor including generating a gate bias voltage for a common source transistor and generating a cascode bias voltage for a cascode transistor that is in series with the common source transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Embodiments of this disclosure will now be described, by way of non-limiting example, with reference to the accompanying drawings.

[0021] Figure 1 is a schematic diagram of one example of a communication network.