

WHAT IS CLAIMED IS:

1. A multi-level cascaded voltage modulator connectable to a load, comprising:
a plurality of power cells connected in series, wherein each cell of the plurality of cells comprises a of bidirectional switch and a storage element; and
a control system coupled to the plurality of cells and having a multi-level hysteresis voltage controller, wherein the control system is configured to cause the plurality of cells to output N levels of voltage on the load, wherein N is a positive integer corresponding to the number of power cells of the plurality of power cells.
2. The modulator of claim 1, wherein each cell of the plurality of cells includes
a secondary winding isolation transformer;
a three-phase diode bridge coupled to the transformer and the storage element; and
a diode.
3. The modulator of claim 2, wherein the bidirectional switch is one of an IGBT or a MOSFET.
4. The modulator of claim 2, wherein each cell of the plurality of cells further comprises an LCR filter at its output.
5. The modulator of claim 2, further comprising a CR filter at the output of the plurality of cells.
6. The modulator of claim 2, wherein the control system is further configured to cause the transfer of electrical power from the energy storage elements of the power cells to the load.
7. The modulator of claim 2, wherein the control system is further configured to balance voltages on the storage elements.
8. The modulator of claim 2, wherein the storage element is a capacitor.

9. The modulator of claims 1-8, wherein the control system including one or more processors coupled to a non-transitory memory comprising a plurality of instructions that when executed causes the one or more processors to control a level of voltage on the load.

10. The modulator of claim 9, wherein the plurality of instructions when executed causes the one or more processors to control an output voltage level of the modulator as a function of the level of voltage on the load, a reference voltage and a voltage error equal to the difference between the level of voltage on the load and the reference voltage.

11. The modulator of claim 9, wherein the plurality of instructions when executed causes the one or more processors to:

subtract from a reference voltage signal V_{REF} a real feedback voltage signal V_{REAL} received from a voltage sensor;

produce, by a voltage level estimator, an estimated voltage level signal, $Levels$, using a high boundary (HB) threshold of a hysteresis block, a low boundary (LB) threshold of the hysteresis block, and the voltage difference signal ΔV ; and

generate, by a switching pattern generator, a plurality of switching signals based on the estimated voltage level, $Levels$, and a state of the hysteresis block.

12. The modulator of claim 9, wherein to subtract from a reference voltage signal V_{REF} a real feedback voltage signal V_{REAL} , the plurality of instructions when executed causes the one or more processors to:

feed the real feedback voltage signal V_{REAL} to a low-pass filter input;

feed a low-pass filter output signal to a negative input of a first summation block;

feed the reference voltage signal V_{REF} to a positive input of the first summation block;

and

produce a voltage difference signal ΔV at an output of the first summation block.

13. The modulator of claim 11, wherein:

when ΔV reaches the high boundary (HB) threshold of the hysteresis block, the plurality of instructions when executed causes the one or more processors to set the state of the hysteresis block to "1."

14. The modulator of one of claims 11 or 13, wherein:
when ΔV reaches the low boundary (LB) threshold of the hysteresis block, the plurality of instructions when executed causes the one or more processors to set the state of the hysteresis block to "0."
15. The modulator of claim 11, wherein to produce the estimated voltage level Levels, the plurality of instructions when executed causes the one or more processors to:
apply a clock signal to a clock generator;
count, by a resettable counter, a number of clock signals generated by the clock generator when one or more of the following conditions is true:
 ΔV is lower than the low boundary (LB) threshold of the hysteresis block; or
 ΔV is higher than the high boundary (HB) threshold of the hysteresis block;
increment, by a free running counter, a free running counter output signal;
apply the free running counter output signal to a second summation block; and
decrement a number of Levels at an output of the voltage level estimator when both of the following cases are true at the same time:
the signal ΔV is lower than the low boundary hysteresis threshold LB; and
the value of an output counting signal of the resettable counter is higher than a preset value of a time constant.
16. The modulator of claim 15, wherein when both the signal ΔV is lower than the low boundary hysteresis threshold LB and the value of the output counting signal of the resettable counter is higher than the preset value of a time constant, the plurality of instructions when executed causes the one or more processors to:
set the output of a logic element of a level decrement circuit to True;
detect the output of the logic element with a rising edge detector; and
increment the free running counter, and thereby decrement an output level at a summation block.
17. The modulator of claim 1, wherein the multi-level hysteresis voltage controller comprises:
a low pass filter having a low-pass filter input and a low-pass filter output;
a first summation block having a positive input and a negative input;

a hysteresis block having a high boundary (HB) threshold and a low boundary (LB) threshold;

a voltage level estimator having a plurality of voltage level estimator inputs and a voltage level output signal Levels; and

a switching pattern generator having a plurality of switching pattern generator inputs and a plurality of switching pattern generator outputs.

18. The modulator of claim 17, wherein the switching pattern generator comprises:

a comparator block;

a resettable counter;

a first multiplexer having a first plurality of input signals; and

a second multiplexer having a second plurality of input signals.

19. The modulator of claim 18, wherein each input signal of the second plurality of input signals represents an array of switching states each corresponding to a one of plurality of output levels for a voltage modulator.

20. The modulator of claim 19, wherein the plurality of output levels ranges from OVDC when all switching signals are false to a maximum output voltage when all switching signals are true.

21. The modulator of claim 17, wherein the voltage level estimator comprises:

a clock counting circuit;

a level decrement circuit;

an enable and reset circuit for the resettable counter; and

a second summation block.

22. The modulator of claim 21, wherein the clock counting circuit comprises a clock generator, a logic switch, and a resettable counter.

23. The modulator of claim 21 or 22, wherein the level decrement circuit comprises a first logic element, a rising edge detector, and a free running counter.

24. The modulator of claims 21-23, wherein the enable and reset circuit comprises a second logic element, a rising edge detector and a third logic element.

25. The modulator of claim 24, wherein the first logic element is an AND gate, the second logic element is an XOR gate, and the third logic element is an OR gate.

26. The modulator of claim 17, wherein when ΔV reaches the high boundary (HB) threshold of the hysteresis block, the state of the hysteresis block is set to "1."

27. The modulator of claims 17 or 26, wherein when ΔV reaches the low boundary (LB) threshold of the hysteresis block, the state of the hysteresis block is set to "0."

28. The modulator of any one of claims 17-27, wherein the load is in a power electronic circuit in one or more of an electrode biasing power supply for a Tokamak plasma reactor, an electrode biasing power supply for a FRC plasma reactor, a power supply for a neutral beam injector, a magnetron modulator, a klystron modulator, an E-gun modulator, a high power X-ray power supply, a mediumwave transmitter, a longwave transmitter, and a shortwave solid-state transmitter.

29. A multi-level hysteresis voltage controller for a multi-level voltage modulator connectable to a load, comprising:

a low pass filter having a low-pass filter input and a low-pass filter output;

a first summation block having a positive input and a negative input;

a hysteresis block having a high boundary (HB) threshold and a low boundary (LB) threshold;

a voltage level estimator having a plurality of voltage level estimator inputs and a voltage level output signal Levels; and

a switching pattern generator having a plurality of switching pattern generator inputs and a plurality of switching pattern generator outputs.

30. The multi-level hysteresis voltage controller of claim 29, wherein the switching pattern generator comprises:

a comparator block;

a resettable counter;

a first multiplexer having a first plurality of input signals; and
a second multiplexer having a second plurality of input signals.

31. The multi-level hysteresis voltage controller of claim 30, wherein each input signal of the second plurality of input signals represents an array of switching states each corresponding to a one of plurality of output levels for a voltage modulator.

32. The multi-level hysteresis voltage controller of claim 31, wherein the plurality of output levels ranges from 0VDC when all switching signals are false to a maximum output voltage when all switching signals are true.

33. The multi-level hysteresis voltage controller of claim 29, wherein the voltage level estimator comprises:

a clock counting circuit;
a level decrement circuit ;
an enable and reset circuit for the resettable counter; and
a second summation block.

34. The multi-level hysteresis voltage controller of claim 33, wherein the clock counting circuit comprises a clock generator, a logic switch, and a resettable counter.

35. The multi-level hysteresis voltage controller of claim 33 or 34, wherein the level decrement circuit comprises a first logic element, a rising edge detector, and a free running counter.

36. The multi-level hysteresis voltage controller of and of claims 33-35, wherein the enable and reset circuit comprises a second logic element, a rising edge detector and a third logic element.

37. The multi-level hysteresis voltage controller of claim 36, wherein the first logic element is an AND gate, the second logic element is an XOR gate, and the third logic element is an OR gate.

38. The multi-level hysteresis voltage controller of claim 29, wherein when ΔV reaches the high boundary (HB) threshold of the hysteresis block, the state of the hysteresis block is set to “1.”

39. The multi-level hysteresis voltage controller of claims 29 or 38, wherein when ΔV reaches the low boundary (LB) threshold of the hysteresis block, the state of the hysteresis block is set to “0.”

40. The multi-level hysteresis voltage controller of any one of claims 29-39, wherein the load is in a power electronic circuit in one or more of an electrode biasing power supply for a Tokamak plasma reactor, an electrode biasing power supply for a FRC plasma reactor, a power supply for a neutral beam injector, a magnetron modulator, a klystron modulator, an E-gun modulator, a high power X-ray power supply, a mediumwave transmitter, a longwave transmitter, and a shortwave solid-state transmitter.

41. A method of controlling a voltage supplied to a load using a multi-level hysteresis voltage controller, comprising:

receiving a real feedback voltage signal V_{REAL} from a voltage sensor;

subtracting the real feedback voltage signal V_{REAL} from a reference voltage signal V_{REF} by

feeding the real feedback voltage signal V_{REAL} to a low-pass filter input;

feeding a low-pass filter output signal to a negative input of a first summation block;

feeding the reference voltage signal V_{REF} to a positive input of the first summation block; and

producing a voltage difference signal ΔV at an output of the first summation block;

producing, by a voltage level estimator, an estimated voltage level signal, $Levels$, using a high boundary (HB) threshold of a hysteresis block, a low boundary (LB) threshold of the hysteresis block, and the voltage difference signal ΔV ; and

generating, by a switching pattern generator, a plurality of switching signals based on the estimated voltage level, $Levels$, and a state of the hysteresis block.

42. The method of claim 41, wherein:

when ΔV reaches the high boundary (HB) threshold of the hysteresis block, the state of the hysteresis block is set to “1.”

43. The method of one of claims 41 or 42, wherein:

when ΔV reaches the low boundary (LB) threshold of the hysteresis block, the state of the hysteresis block is set to “0.”

44. The method of claim 43, wherein the voltage level estimator produces the estimated voltage level Levels by:

applying a clock signal to a clock generator;

counting, by a resettable counter, a number of clock signals generated by the clock generator when one or more of the following conditions is true:

ΔV is lower than the low boundary (LB) threshold of the hysteresis block; or

ΔV is higher than the high boundary (HB) threshold of the hysteresis block;

incrementing, by a free running counter, a free running counter output signal;

applying the free running counter output signal to a second summation block; and

decrementing a number of Levels at an output of the voltage level estimator when both of the following cases are true at the same time:

the signal ΔV is lower than the low boundary hysteresis threshold LB; and

the value of an output counting signal of the resettable counter is higher than a preset value of a time constant.

45. The method of claim 44, wherein when both the signal ΔV is lower than the low boundary hysteresis threshold LB and the value of the output counting signal of the resettable counter is higher than the preset value of a time constant:

a logic element output of a level decrement circuit becomes True;

a rising edge detector detects the logic element output; and

the free running counter is incremented, thereby decrementing an output level at a summation block.