

DRAM OPERATION FREQUENCY ADJUSTING SYSTEM AND METHOD

Technical Field

The invention relates to Dynamic Random-Access Memory (DRAM) technology, more particularly to an operation frequency adjusting system for DRAM and a method thereof.

Technology Background

DRAM is a dynamic random access memory. DRAM retains data for only a short time. In order to retain data, DRAM adopts a memory capacitor and refreshes at intervals so as to retain data stored therein. The refreshment is operated by a DRAM controller. The refreshment of DRAM may consume a relative large amount of electric energy, which requires that batteries of DRAM should have high capacity.

As a typical system on chip (SOC), a multimedia system on chip includes a plurality of functional modules, such as processor, hardware accelerator, and so on. The functional modules operate independently and access to various memory devices. Because of that some of the functional modules of the multimedia system on chip store their data on an external DRAM during data processing, as to a complicated multimedia system on chip, difference in requirements of bandwidth of the DRAM for different tasks may be rather big. For example, during display processes for high-definition streaming media files, the multimedia system on chip requires the processor and the hardware accelerator to run at full speed. However, during playing MP3, operations and the desired bandwidth of DRAM decrease shortly. Thus, the requirement on power consumption of the multimedia system-on-chip is raised.

Those conventional multimedia systems on chip pre-configure operation frequency of DRAM only at some special intervals, for example, at the start time of the system, without consideration for different features of those tasks.

It is difficult to achieve an appreciate balance between efficiency and power consumption of DRAM.

Thus, an urgent technology problem needed to be solved by those skilled in the art is how to provide a method for adjusting operation frequency of DRAM so as to achieve an appreciate balance between efficiency and power consumption of DRAM, which enables the system on chip to operate at a desired speed and simultaneously achieve an improvement in the power consumption.

SUMMARY OF THE INVENTION

A technical problem to be solved in the present invention is how to provide a solution adjusting an operation frequency of DRAM and a DRAM operation frequency system using the solution, so as to adjust the balance between efficiency and power consumption of DRAM.

To solve the above technical problem, the present invention provides a DRAM operation frequency adjusting system including:

- a statistic module counting effective operation statuses of DRAM during a predetermined time interval;

- a parameter configuration module generating a target operation frequency according to the count of the effective operation statuses of DRAM; and

- a frequency switch controller switching the present operation frequency of DRAM to the target operation frequency.

The present invention also provides a DRAM operation frequency adjusting method including:

- counting effective operation statuses of DRAM during a predetermined time interval to obtain a bandwidth utilization rate of DRAM at a present operation frequency;

- generating a target operation frequency when the bandwidth utilization rate of DRAM is not adapted to a present application environment; and

- switching the present operation frequency of DRAM to the target operation frequency.

Compared with prior arts, the invention has advantages presented as follows.

In the invention, a bandwidth utilization rate of DRAM at a present operation frequency can be obtained by counting effective operation statuses of DRAM during a predetermined time interval. When the bandwidth utilization rate of DRAM is not adapted to the present application environment, the present operation frequency of DRAM is adjusted to a desired operation frequency. Particularly, the present operation frequency of DRAM increases according to the present application environment under a condition that the present operation frequency is low and the bandwidth utilization rate is high, and the present operation frequency of DRAM decreases according to the present application environment under a condition that the present operation frequency is high and the bandwidth utilization rate is low. The way that adjusts the operation frequency of DRAM in real time according to the bandwidth utilization rate can benefit the balance between the efficiency and the power consumption of DRAM.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram showing an example of a DRAM operation frequency adjusting system;

FIG. 2 shows several operation statuses of DRAM;

FIG. 3 is a schematic diagram showing an example of a statistic module.

FIG. 4 is a schematic diagram showing an example of a parameter configuration module.

FIG. 5 is a schematic diagram showing another example of a DRAM operation frequency adjusting system;

FIG. 6 is a time sequence chart of operation of DRAM.

FIG. 7 is a schematic diagram showing another example of a parameter configuration module.

FIG. 8 is a schematic diagram showing an example of a frequency switch controller.

FIG. 9 is a schematic diagram showing an example of a DRAM controller.

FIG. 10 is a flowchart showing an example of a DRAM operation frequency adjusting method.

EMBODIMENTS

The detailed description of the present invention is presented largely according to drawings and preferred embodiments to explain objections, features, and advantages of the present invention.

Referring to FIG. 1, a schematic block diagram of a DRAM operation frequency adjusting system 100 in a preferred embodiment is shown. The operation frequency adjusting system 100 includes a statistic module 11, a parameter configuration module 12, and a frequency switch controller 13.

The statistic module 11 counts effective operation statuses of DRAM and obtains a present bandwidth utilization rate of DDRAM (i.e., a bandwidth utilization rate of DDRAM at a present operation frequency) by counting the effective operation statuses of DRAM.

The parameter configuration module 12 generates a target operation frequency adapted to a present application environment according to the count of the effective operation statuses of DRAM.

The frequency switch controller 13 switches the present operation frequency of DRAM to the target operation frequency.

In factual implement, the statistic module 11 can count various effective operation statuses of DRAM during a predetermined time interval, and calculate the bandwidth utilization rate of DRAM at the present operation frequency during the predetermined time interval according to the count of the effective operation statuses of DRAM.

The operation statuses of DRAM are determined by data access commands. The data access commands are generated by a finite state machine 910 of a DRAM controller 91 of DRAM. Referring to FIG. 2, corresponding to the data access commands, operation statuses of the finite state machine 910 generally include idle (IDLE), pre-charge (PRE), acting (ACT), reading (READ), writing

(WRIT), and so on. Thus, the count of the effective operation statuses of DRAM can be obtained by counting non-idle operation statuses of the finite state machine 910. The statistic module 11 obtains a real-time bandwidth utilization rate of DDRAM by counting the non-idle operation statuses of the finite state machine 910 during a predetermined time interval so as to determine whether the operation frequency of DRAM should be adjusted.

The predetermined time interval can be determined according to the present application environment of DRAM. When the bandwidth utilization rate of DRAM at the present frequency is not adapted to the present application environment, the statistic module 11 may inform the parameter configuration module 12 in a certain way (e.g., by means of interruption) to generate the target operation frequency befitting the present application environment according to a facture desired bandwidth utilization rate of DRAM. The frequency switch controller 13 adjusts the operation frequency of DRAM from the present operation frequency to the target operation frequency. As such, a better balance between operating efficiency and power consumption of DRAM is achieved by adjusting the operation frequency of DRAM in real time based on the dynamic count of the bandwidth utilization rate of DRAM.

Referring to FIG. 3, in a preferred embodiment, the statistic module 11 includes an effective operation status statistic sub-module 111 and an interruption control module 112.

The effective operation status statistic sub-module 111 counts the non-idle operation statuses of the finite state machine 910 during the predetermined time interval so as to obtain the operation statuses of DRAM. The non-idle operation statuses of the finite state machine 910 include pre-charge (PRE), acting (ACT), reading (READ), writing (WRIT), and so on, which are respectively corresponding to various data access commands of DRAM.

The interruption control module 112 generates an interruption signal for adjusting the operation frequency of DRAM according to the bandwidth

utilization rate of DRAM at the present operation frequency. The interruption signal includes a first interruption signal and a second interruption signal. The interruption control module 112 generates the first interruption signal denoting that the operation frequency of DRAM is desired to decrease, when the present bandwidth utilization rate of DRAM is lower than a desired bandwidth utilization rate at the end of the predetermined time interval. The interruption control module 112 generates the second interruption signal denoting that the operation frequency of DRAM is desired to increase, when the status count of the non-idle operation statuses of the finite state machine in the predetermined time interval exceeds a predetermined interruption threshold value.

The effective operation status statistic sub-module 111 may further includes a time interval register 1110, a time counter 1112, a status counter 1113, and a status accumulation register 1114.

The time interval register 1110 sets the predetermined time interval.

The time counter 1112 measures time during the predetermined time interval and clears its time count result at the end of the predetermined time interval.

The status counter 1113 counts the non-idle operation statuses of the finite state machine 910 in real time during the predetermined time interval, copies its own status count to the status accumulation register 1114 and simultaneously clears its own status count when the time count result of the time counter 1112 is equal to the predetermined time interval set in the time interval register 1110. That is, the status count of the status counter 1113 varies with time in the predetermined time interval. The status count of the status counter 1113 at the time when the time count result of the time counter 1112 is equal to the predetermined time interval set in the time interval register 1110, is a status count result adding up all non-idle operation statuses of the finite state machine 910 during the predetermined time interval.

The status accumulation register 1114 saves the status count from the status counter 1113 when the time count result of the time counter 1112 is equal to the

predetermined time interval set in the time interval register 1110. The bandwidth utilization rate of DRAM in the predetermined time interval can be determined by the status count saved in the status accumulation register 1114.

The interruption control module 112 further includes an interruption threshold value register 1121 and an interruption controlling logic module 1123.

The interruption threshold value register 1121 sets a threshold value of the bandwidth utilization rate.

The interruption controlling logic module 1123 sends out an interruption signal according to the status count of the status counter 1113 in the predetermined time interval and the threshold value, or according to the status count saved in the status accumulation register 1114.

The interruption controlling logic module 1123 includes a first interruption control module 1123a and a second interruption control module 1123b. The first interruption control module 1123a determines whether the bandwidth utilization rate of DRAM at the present operation frequency is lower, according to the status count result in the status accumulation register 1114 at the end of the predetermined time interval, and generates a first interruption signal denoting that the operation frequency of DRAM is desired to decrease if the bandwidth utilization rate of DRAM at the present operation frequency is lower than a desired value. The second interruption control module 1123b determines whether the bandwidth utilization rate of DRAM at the present operation frequency is higher, according to the status count of the status counter 1113 in the predetermined time interval and the threshold value, and generates a second interruption signal denoting that the operation frequency of DRAM is desired to increase if the bandwidth utilization rate of DRAM at the present operation frequency exceeds the threshold value.

Correspondingly, referring to FIG. 4, the parameter configuration module 12 includes a target frequency configuration sub-module 121. The target frequency configuration sub-module 121 includes a first configuration unit 1211

generating a target operation frequency lower than the present operation frequency of DRAM according to the first interruption signal and a second configuration unit 1212 generating a target operation frequency higher than the present operation frequency of DRAM according to the second interruption signal.

In the present embodiment, the generation of the interruption signal includes two occasions. On one occasion, at the end of the predetermined time interval, the bandwidth utilization rate of DRAM determined by the status count in the status accumulation register 1114 being lower than the desired value in factual application, the interruption controlling logic module 1123 can send out the first interruption signal, which denotes that the present operation frequency of DRAM is high. On the other one occasion, the interruption controlling logic module 1123 determines the bandwidth utilization rate of DRAM in real-time according to the status count of the status counter 1113 in the predetermined time interval, and send out the second interruption signal, which denotes that the present operation frequency of DRAM is low, when the real-time bandwidth utilization rate of DRAM exceeds the threshold value.

FIG. 2 shows several operation statuses of DRAM. Those operation statuses except the status of IDLE can be considered as the effective operation status, i.e., the non-idle operation statuses. Assuming that the present operation frequency of DRAM is assumed to be 160 MHz and that the status count in the status counter 1113 during one second should be 80 millions, the bandwidth utilization rate of DRAM at the present operation frequency should be $(80/160)*100\%$, i.e., 50%.

For example, the present operation frequency of DRAM is 120 MHz. DRAM employs 16 bit SDRAM as its memory. The bandwidth utilization rate of DRAM obtained by the statistic module 11 is 20%. Thus, the effective bandwidth of DRAM should be $120*16*20\%$ Mbps, i.e., 384 Mbps. The bandwidth utilization rate 20% can be considered steady if nothing has changed in the application environment. If the bandwidth utilization rate 60% is more

appropriate, the interruption control module 112 sends out the first interruption signal, the parameter configuration module 12 then sets the target operation frequency of DRAM to $384/16/60\%$ MHz, i.e., 40 MHz. The frequency switch controller 13 adjusts the operation frequency of DRAM to 40 MHz. As such, the effective bandwidth of DRAM is also $40*16*60\%$ Mbps, i.e., 384 Mbps. However, the operation frequency of DRAM decreases, which results in a reduction of power consumption.

As another example, the present operation frequency of DRAM is 40 MHz. DRAM employs 16 bit SDRAM as its memory. The threshold value of the bandwidth utilization rate is 60% applied to the present application environment. If the bandwidth utilization rate of DRAM obtained by the statistic module 11 is 80%, which exceeds the threshold value, the interruption control module 112 sends out the second interruption signal. Assuming that the bandwidth utilization rate 40% is more appreciate in the present application environment, the parameter configuration module 12 sets the target operation frequency of DRAM to $(40*16*80\%)/16/40\%$ MHz, i.e., 80 MHz. The frequency switch controller 13 adjusts the operation frequency of DRAM to 80 MHz. As such, the efficiency of DRAM has improved.

Referring to FIG. 5, in order to prevent data from being lost during adjusting the operation frequency of DRAM, in the present embodiment, the DRAM operation frequency adjusting system 100 further includes a clock control module 15. The clock control module is configured for enabling DRAM to refresh according to an internal clock while the frequency switch controller 13 is under operation and enabling DRAM to refresh according to a system clock after the operation of the frequency switch controller 13 is finished.

In factual application, the refreshment of DRAM can be divided into two classes including Auto Refresh (AR) and Self Refresh (SR). Accordingly, DRAM has two operation modes including an AR mode and an SR mode. In the AR mode, DRAM refreshes under the system clock. In the SR mode,

DRAM refreshes not depending on the system clock but upon the internal clock.

When DRAM is in the SR mode, the system clock is not necessary, so the adjustment of the system clock, i.e., the adjustment of the operation frequency of DRAM from the present operation frequency to the target operation frequency, can be carried out in the SR mode. After DRAM quits from the SR mode, DRAM can be operated at the target operation frequency.

Referring to a time sequence chart of operation of DRAM shown in FIG. 6, CLK is the system clock provided for DRAM. The frequency of CLK before the time T_2 may be different from the frequency of CLK after the time T_{n+1} . In the present embodiment, the frequency before the time T_2 is the present operation frequency of DRAM. The adjustment of the operation frequency of DRAM is carried out during the time $T_2 \sim T_{n+1}$. The frequency of CLK after the time T_2 may be the target operation frequency hence.

Because of that all outer signals are invalid except clock Enable signal (CKE) and none of outer refresh instructions is necessary, the adjustment of the operation frequency in SR mode keeps a good balance between the efficiency and the power consumption of DRAM, however, without resulting in the loss of data.

In order to ensure the system clock valid, the system clock can be determined by a sequence checking parameter. The DRAM operation frequency adjusting system 100 further includes a sequence checking parameter validating module 16. The sequence checking parameter validating module 16 is configured for collecting a sequence checking parameter corresponding to the target operation frequency.

Generally, the sequence checking parameter linearly relates to the frequency of the system clock of DRAM. For example, assuming that the refresh interval of DRAM is 10 μ s, therefore, the sequence checking parameter should be set to 1000 at a frequency of 100 MHz, or the sequence checking

parameter should be set to 100 at a frequency of 10 MHz.

The clock control module 15 and the sequence checking parameter validating module 16 can be set in the DRAM controller 91 or out of the DRAM controller 91.

Referring to FIG. 7, the parameter configuration module 12 further includes a frequency switch request configuration module 122 configured for setting a frequency switch request signal with a default value denoting invalid, a handshaking signal configuration module 123 configured for generating a handshaking signal with a default value denoting invalid, and a sequence checking parameter configuration module 124 configured for respectively generating sequence checking parameters for the operation frequencies of DRAM.

Referring to FIG. 8, the frequency switch controller 13 includes a frequency switch request generating module 131, a frequency adjustment module 133, and an invalid request configuration module 135.

The frequency switch request generating module 131 is configured for generating a frequency switch request signal and setting the frequency switch request signal to valid.

The frequency adjustment module 133 is configured for switching the present operation frequency of DRAM to the target operation frequency according to a valid handshaking signal.

The invalid request configuration module 135 is configured for enabling the frequency switch request signal to return to invalid after the frequency adjustment module 133 finishes the frequency adjustment.

Referring to FIG. 9, the DRAM controller 91 further includes a self refresh control module 912, a handshaking signal waken module 913, a sequence checking parameter validation module 914, a self refresh quitting module 915, and a handshaking signal sleeping module 916.

The self refresh control module 912 is configured for sending out a first

controlling command, which requests DRAM to refresh under the internal clock, according to a valid frequency switch request signal.

The handshaking signal waken module 913 is configured for setting the handshaking signal to valid after the first controlling command being sent out.

The sequence checking parameter validation module 914 is configured for collecting a sequence checking parameter corresponding to the target operation frequency when the frequency switch request signal return invalid.

The self refresh quitting module 915 is configured for determining the system clock according to the sequence checking parameter and sending out a second controlling command, which requests DRAM to refresh under the system clock.

The handshaking signal sleeping module 916 is configured for resetting the handshaking signal to invalid after the second controlling command being sent out.

In order to avoid the loss of data during the frequency adjustment of DRAM, the DRAM controller may preferably includes:

a data request interruption module 917 configured for executing those existing data requests and stopping answering new data requests after receiving a valid frequency switch request signal but before the first controlling command being sent out; and

a data request execution module 918 configured for accepting new data requests after the handshaking signal return invalid.

In factual, the DRAM controller 91 accepts external data requests. The DRAM controller 91 can execute all the data requests that have been received by DRAM controller 91, but stop answering new data requests, i.e., stop function modules of chips accessing DRAM, before the frequency adjustment. As such, the loss of data is avoided during the frequency adjustment.

Because of that all outer signals are invalid except Clock Enable Signal (CKE) when DRAM is in the self refresh mode, and no outer refresh instruction is necessary, which may benefit improving the power consumption.

A working process of the DRAM operation frequency adjusting system 100 based on the above described preferred embodiments are presented to enable those skilled in the art to most effectively understand the substance of the present invention.

Assuming that the target frequency configuration sub-module 121 had generated a target operation frequency, the frequency switch request configuration module 122 sets the default value of the frequency switch request signal (i.e., clock switch request, hereinafter referred as csr). The default value of csr denotes invalid. That is, the default value of csr is set to a binary code “0”. The handshaking signal configuration module 123 sets the default value of the handshaking signal (hereinafter referred as sl). The default value of sl denotes invalid. That is, the default value of sl is set to a binary code “0”. The sequence checking parameter configuration module 124 configures sequence checking parameters respectively for the present operation frequency and the target operation frequency of DRAM.

In this situation, the process switching the present operation frequency of DRAM to the target operation frequency includes following steps.

In the step S101, the frequency switch request generating module generates a frequency switch request signal (csr), and the value of the frequency switch request signal (csr) is set to valid, i.e., the value of the frequency switch request signal (csr) is set to a binary code “1”.

In the step S102, the self refresh control module 912 sends out the first controlling command, which requests DRAM to refresh under the internal clock, after detecting that the value of csr is “1”.

In the step S103, the handshaking signal waken module 913 sets the value of the handshaking signal to valid, i.e., the value of the handshaking signal to valid is set to a binary code “1”.

In the step S104, the frequency adjustment module 133 switches the present operation frequency of DRAM to the target operation frequency after detecting

that the value of sl is “1”.

In the step S105, the invalid request configuration module 135 resets the value of the frequency switch request signal (csr) to “0”, after the frequency switch is finished.

In the step S106, the sequence checking parameter validation module 914 collects a sequence checking parameter corresponding to the target operation frequency after detecting that the value of the frequency switch request signal (csr) is “1”.

In the step S107, the self refresh quitting module 915 determines the system clock according to the sequence checking parameter and sends out the second controlling command, which requests DRAM to refresh under the system clock.

In the step S108, the handshaking signal sleeping module 916 resets the handshaking signal (sl) from “1” to “0”.

The means that the DRAM controller 91 and the frequency switch controller 13 employ the frequency switch request signal and the handshaking signal to communicate each other is only used as an example. The skilled in the art, of course, can employ any other communication means as needed.

The invention can be applied to multi-media systems on chip. When the processor or the hardware accelerator accesses DRAM, the DRAM operation frequency adjusting system 100 adjusts the operation frequency of DRAM according to characters of media tasks.

Referring to FIG. 10, a flow chart of a DRAM operation frequency adjusting method is shown. DRAM operation frequency adjusting method includes following steps:

step 401, counting effective operation statuses of DRAM during a predetermined time interval to obtain a bandwidth utilization rate of DRAM at a present operation frequency;

step 402, generating a target operation frequency when the bandwidth

utilization rate of DRAM is not adapted to present application environment; and

step 403, switching the present operation frequency of DRAM to the target operation frequency.

The step counting the effective operation statuses of DRAM may include following sub-steps:

sub-step A1, counting non-idle operation statuses of a finite state machine 910 in a DRAM controller of DRAM to obtain the effective operation statuses of DRAM; and

sub-step A2, determining the bandwidth utilization rate of DRAM according to the effective operation statuses of DRAM at the end of the predetermined time interval; generating a first interruption signal denoting that the operation frequency of DRAM should decrease when the bandwidth utilization rate of DRAM at present is lower; generating a second interruption signal denoting that the operation frequency of DRAM should increase when the bandwidth utilization rate of DRAM at present exceeds a predetermined interruption threshold value in the predetermined time interval.

The step generating the target operation frequency may include following sub-steps:

generating a target operation frequency lower than the present operation frequency of DRAM according to the first interruption signal when the first interruption signal is generated; or, generating a target operation frequency higher than the present operation frequency of DRAM according to the second interruption signal when the second interruption signal is generated.

In a preferred embodiment of the present invention, the method further includes steps: requesting DRAM to refresh under an internal clock during the frequency switch and requesting DRAM to refresh under a system clock.

Preferably, the system clock is determined by a sequence checking parameter. The DRAM operation frequency adjusting method further includes obtaining a corresponding sequence checking parameter according to the target operation

frequency.

In a preferred embodiment of the present invention, the method further includes:

presetting a frequency switch request signal with a default value thereof denoting invalid, a handshaking signal with a default value thereof denoting invalid, and sequence checking parameters corresponding to the operation frequencies of DRAM.

The step switching the operation frequency of DRAM may includes following sub-steps:

sub-step B1, generating a frequency switch request signal and setting the frequency switch request signal to valid;

sub-step B2, sending out a first controlling command, which requests DRAM to refresh under the internal clock, according a valid frequency switch request signal;

sub-step B3, setting the handshaking signal to valid after sending out the first controlling command;

sub-step B4, switching the present operation frequency of DRAM to the target operation frequency according to a valid handshaking signal;

sub-step B5, resetting the frequency switch request signal to invalid after finishing the frequency switch;

sub-step B6, collecting a sequence checking parameter corresponding to the target operation frequency when the frequency switch request signal return invalid;

sub-step B7, determining the system clock according to the sequence checking parameter and sending out the second controlling command, which requests DRAM to refresh under the system clock; and

sub-step B8, resetting the handshaking signal to invalid.

In factual application, in order to avoid loss of data during the frequency switch of DRAM, the method may further include:

executing accepted data requests and stopping answering new data requests after receiving a valid frequency switch request signal but before sending out the first controlling command; and

accepting new data requests after the handshaking signal return invalid.

As to the embodiments of the method, because of that they are similar to the embodiments of the system, the related portion refers to the embodiments of the system.

The DRAM operation frequency adjustment system and method have been detailed in the above descriptions. The principle and realization of the invention has been described by way of examples, which are only presented to facilitate understanding of the methodology and the substance of the invention. Numerous changes in the embodiments and the application areas can be made by those skilled in the art according to the substance of the invention. Accordingly, the foregoing description of embodiments should not be considered as definition of the scope of the present invention.

CLAIMS

1. A DRAM operation frequency adjusting system, comprising:
 - a statistic module counting effective operation statuses of DRAM;
 - a parameter configuration module generating a target operation frequency according to the count of the effective operation statuses of DRAM; and
 - a frequency switch controller switching a present operation frequency of DRAM to the target operation frequency.
2. The system as claimed in claim 1, wherein the statistic module obtains the count of the effective operation statuses of DRAM by counting non-idle operation statuses of the finite state machine of DRAM.
3. The system as claimed in claim 1, wherein the statistic module includes an effective operation status statistic sub-module and an interruption control module, the effective operation status statistic sub-module counting non-idle operation statuses of a finite state machine of DRAM during a predetermined time interval to obtain a bandwidth utilization rate of DRAM at the present operation frequency, the interruption control module generating an interruption signal for adjusting the operation frequency of DRAM.
4. The system as claimed in claim 3, wherein the effective operation status statistic sub-module comprises:
 - a time interval register setting the predetermined time interval;
 - a time counter measuring time during the predetermined time interval and clearing its time count result at the end of the predetermined time interval;
 - a status counter counting the non-idle operation statuses of the finite state machine during the predetermined time interval, copying a status count thereof to a status accumulation register when the time count result of the time counter is equal to the predetermined time interval set in the time interval register, and simultaneously clearing the status count thereof; and
 - a status accumulation register saving the status count from the status counter when the time count result of the time counter is equal to the predetermined time

interval set in the time interval register.

5. The system as claimed in claim 3, wherein the interruption signal includes a first interruption signal and a second interruption signal, the interruption control module generating the first interruption signal denoting that the operation frequency of DRAM is desired to decrease when the present bandwidth utilization rate of DRAM is lower than a desired bandwidth utilization rate, the interruption control module generating the second interruption signal denoting that the operation frequency of DRAM is desired to increase when the status counter of the non-idle operation statuses of the finite state machine in the preconfigured time interval exceeds a predetermined interruption threshold value.

6. The system as claimed in claim 4, wherein the interruption control module includes:

an interruption threshold value register setting a threshold value of the bandwidth utilization rate; and

an interruption controlling logic module sending out an interruption signal according to the status count of the status counter in the preconfigured time interval and the threshold value, or according to the status count saved in the status accumulation register.

7. The system as claimed in claim 6, wherein the interruption controlling logic module includes:

a first interruption control module generating a first interruption signal denoting that the operation frequency of DRAM at the present operation frequency is desired to decrease if the bandwidth utilization rate of DRAM at the present operation frequency is lower; and

a second interruption control module generating a second interruption signal denoting that the operation frequency of DRAM is desired to increase if the bandwidth utilization rate of DRAM at the present frequency is higher.

8. The system as claimed in claim 7, wherein the parameter configuration module includes a target frequency configuration sub-module, the target frequency

configuration sub-module including:

a first configuration unit generating a target operation frequency lower than the present operation frequency of DRAM according to the first interruption signal; and

a second configuration unit generating a target operation frequency higher than the present operation frequency of DRAM according to the second interruption signal.

9. The system as claimed in claim 1, further comprising a clock control module enabling DRAM to refresh according to an internal clock while the frequency switch controller is under operation and enabling DRAM to refresh according to a system clock after the operation of the frequency switch controller is finished.

10. The system as claimed in claim 9, wherein the system clock is determined by a sequence checking parameter, the system further comprising a sequence checking parameter validating module collecting a sequence checking parameter corresponding to the target operation frequency.

11. The system as claimed in claim 9 or 10, wherein the clock control module and the sequence checking parameter validating module are set in a DRAM controller of DRAM.

12. The system as claimed in claim 1, further comprising a DRAM controller connected to the frequency switch controller;

the parameter configuration module comprising:

a frequency switch request configuration module configured for setting a frequency switch request signal with a default value denoting invalid;

a handshaking signal configuration module configured for generating a handshaking signal with a default value denoting invalid; and

a sequence checking parameter configuration module configured for respectively generating sequence checking parameters corresponding to operation frequencies of DRAM;

the frequency adjustment controller comprising:

- a frequency switch request generating module configured for generating a frequency switch request signal and setting the frequency switch request signal to valid;

- a frequency adjustment module configured for switching the present operation frequency of DRAM to the target operation frequency according to a valid handshaking signal; and

- a invalid request configuration module configured for enabling the frequency switch request signal to return to invalid after the frequency adjustment module finishes the frequency switch.

13. The system as claimed in claim 12, wherein the DRAM controller comprises:

- a self refresh control module configured for sending out a first controlling command, which requests DRAM to refresh under an internal clock, according to a valid frequency switch request signal;

- a handshaking signal waken module configured for setting the handshaking signal to valid after the first controlling command being sent out;

- a sequence checking parameter validation module configured for collecting a sequence checking parameter corresponding to the target operation frequency when the frequency switch request signal return invalid;

- a self refresh quitting module configured for determining a system clock according to the sequence checking parameter and sending out a second controlling command, which requests DRAM to refresh under the system clock; and

- a handshaking signal sleeping module configured for resetting the handshaking signal to invalid after the second controlling command being sent out.

14. The system as claimed in claim 13, wherein the DRAM controller further comprises:

a data request interruption module configured for executing existing data requests and stopping answering new data requests after receiving a valid frequency switch request signal but before the first controlling command being sent out; and

a data request execution module configured for accepting new data requests after the handshaking signal return invalid.

15. A DRAM operation frequency adjusting method, comprising:

counting effective operation statuses of DRAM during a predetermined time interval to obtain a bandwidth utilization rate of DRAM at a present operation frequency;

generating a target operation frequency when the bandwidth utilization rate of DRAM is not adapted to a present application environment; and

switching the present operation frequency of DRAM to the target operation frequency.

16. The method as claimed in claim 15, wherein the step counting effective operation statuses of DRAM comprises:

sub-step A1, counting non-idle operation statuses of a finite state machine in a DRAM controller of DRAM during the predetermined time interval to obtain the effective operation statuses of DRAM; and

sub-step A2, determining the bandwidth utilization rate of DRAM according to the effective operation statuses of DRAM at the end of the predetermined time interval, generating a first interruption signal denoting that the operation frequency of DRAM should decrease when the bandwidth utilization rate of DRAM is lower; and generating a second interruption signal denoting that the operation frequency of DRAM should increase when the bandwidth utilization rate of DRAM exceeds a predetermined interruption threshold value in the predetermined time interval.

17. The method as claimed in claim 16, wherein the step generating a target operation frequency comprises:

generating a target operation frequency lower than the present operation frequency of DRAM according to the first interruption signal when the first interruption signal is generated; or, generating a target operation frequency higher than the present operation frequency of DRAM according to the second interruption signal when the second interruption signal is generated.

18. The method as claimed in claim 15, further comprising:

requesting DRAM to refresh under an internal clock during the frequency switch; and

requesting DRAM to refresh under a system clock.

19. The method as claimed in claim 18, wherein the system clock is determined by a sequence checking parameter, the method further comprising:

obtaining a corresponding sequence checking parameter according to the target operation frequency.

20. The method as claimed in claim 15, further comprising:

pre-setting a frequency switch request signal with a default value denoting invalid, a handshaking signal with a default value denoting invalid, and sequence checking parameters corresponding to operation frequencies of DRAM;

wherein the step switching the operation frequency comprises:

sub-step B1, generating a frequency switch request signal and setting the frequency switch request signal to valid;

sub-step B2, sending out a first controlling command, which requests DRAM to refresh under an internal clock, according a valid frequency switch request signal;

sub-step B3, setting the handshaking signal to valid after sending out the first controlling command;

sub-step B4, switching the present operation frequency of DRAM to the target operation frequency according to a valid handshaking signal;

sub-step B5, resetting the frequency switch request signal to invalid after finishing the frequency switch;

sub-step B6, collecting a sequence checking parameter corresponding to the target operation frequency when the frequency switch request signal return invalid;

sub-step B7, determining a system clock according to the sequence checking parameter and sending out a second controlling command, which requests DRAM to refresh under the system clock; and

sub-step B8, resetting the handshaking signal to invalid.

21. The method as claimed in claim 20, further comprising:

executing accepted data requests and stopping answering new data requests after receiving a valid frequency switch request signal but before sending out the first controlling command; and

accepting new data requests after the handshaking signal return invalid.

22. The method as claimed in claim 18, wherein the step counting effective operation statuses of DRAM comprises:

counting non-idle operation statuses of a finite state machine in a DRAM controller of DRAM during the predetermined time interval to obtain the effective operation statuses of DRAM; and

generating a first interruption signal denoting that the operation frequency of DRAM is desired to decrease at the end of the predetermined time interval; or generating a second interruption signal denoting that the operation frequency of DRAM is desired to increase when the count of the non-idle operation statuses of the finite state machine exceeds a predetermined interruption threshold value in the predetermined time interval;

the step generating a target operation frequency comprises:

generating a target operation frequency lower than the present operation frequency of DRAM according to the first interruption signal when the first interruption signal is generated; or generating a target operation frequency higher than the present operation frequency of DRAM according to the second interruption signal when the second interruption signal is generated.