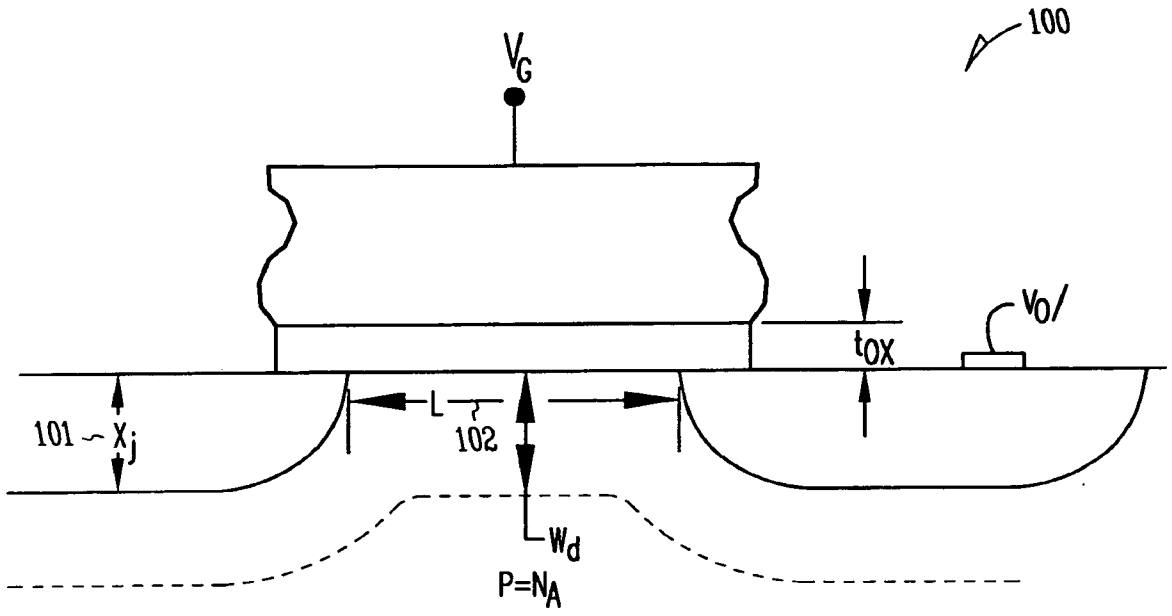



$V_G \longrightarrow V_G/k$ $\quad V_O \longrightarrow V_O/k$

$t_{OX} \longrightarrow t_{OX}/k$

$L \longrightarrow L/k$

$X_j \longrightarrow X_j/k$ JUNCTION DEPTH DECREASED

$W_d \longrightarrow W_d/k$

$N_A \longrightarrow k\ N_A$ SUBSTRATE DOPING INCREASED

*FIG. 1*

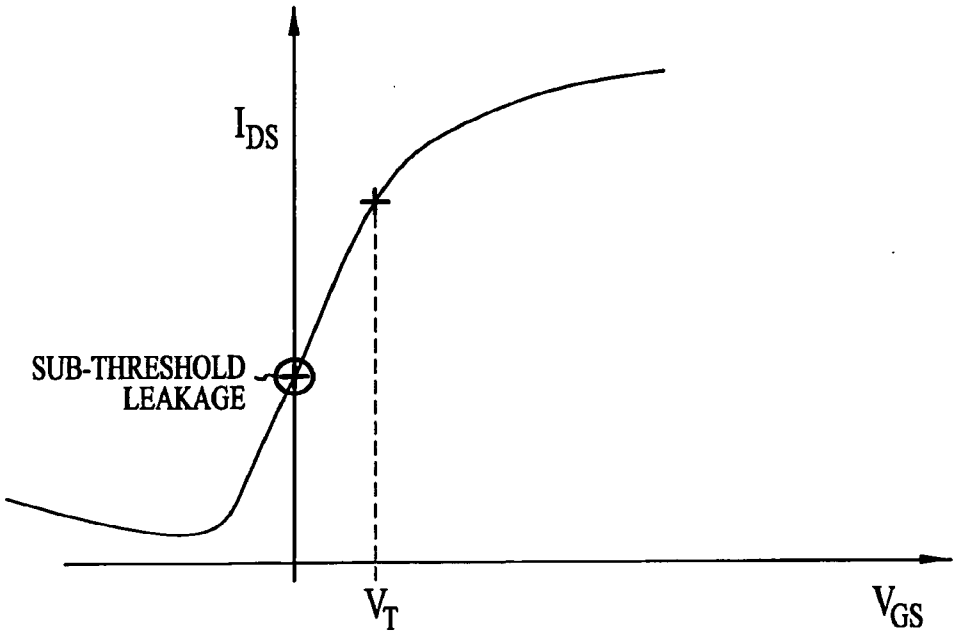

$I_{DS}$
SUB-THRESHOLD LEAKAGE
$V_T$
$V_{GS}$

*FIG. 2*

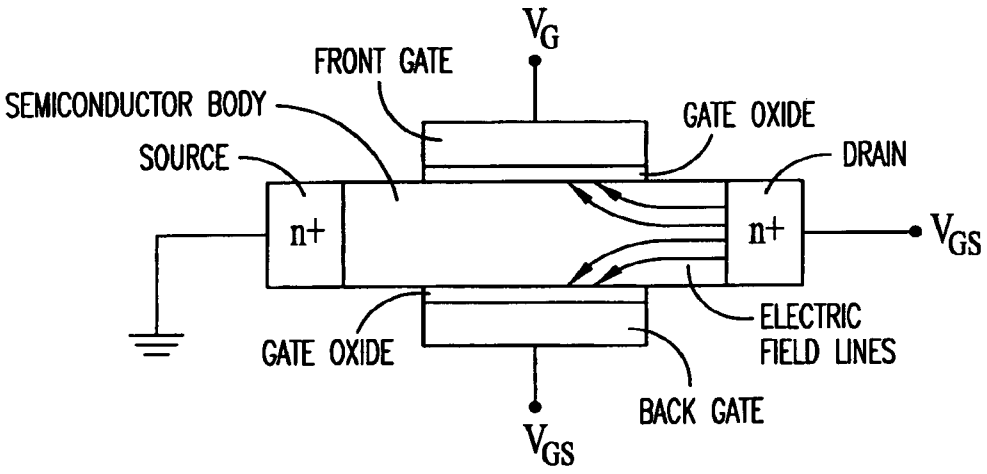

$V_G$
FRONT GATE
SEMICONDUCTOR BODY
GATE OXIDE
SOURCE
DRAIN
n+
n+
$V_{GS}$
ELECTRIC FIELD LINES
GATE OXIDE
BACK GATE
$V_{GS}$

*FIG. 3*

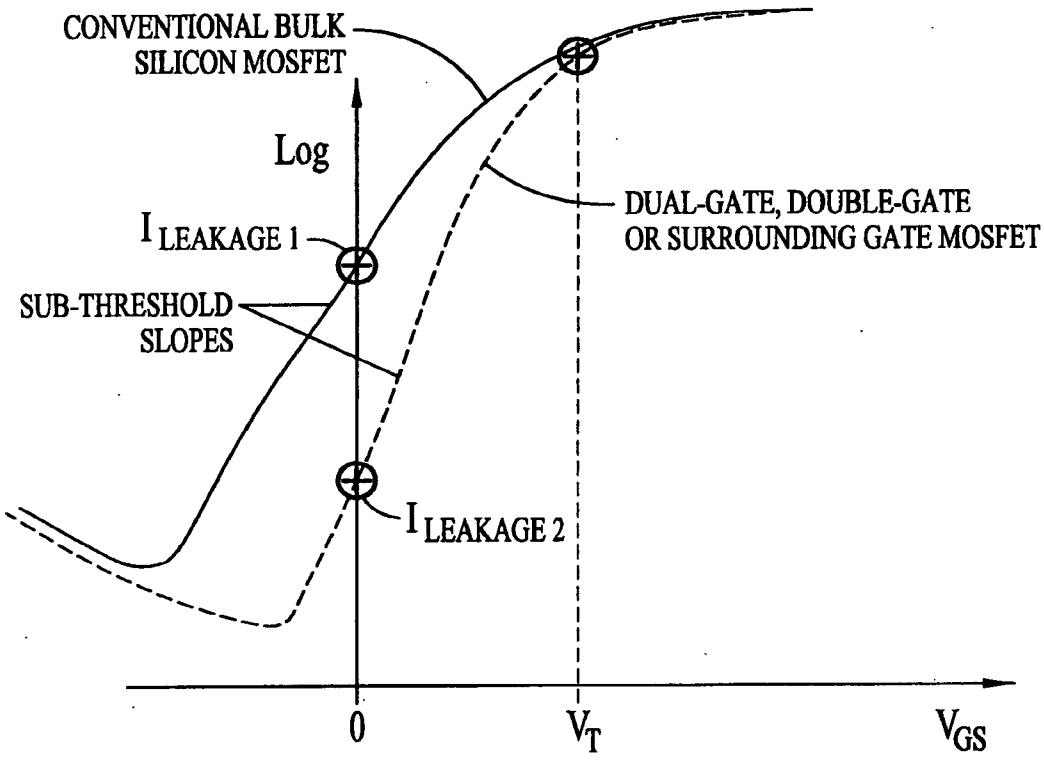

CONVENTIONAL BULK
SILICON MOSFET
Log
I LEAKAGE 1
SUB-THRESHOLD
SLOPES
DUAL-GATE, DOUBLE-GATE
OR SURROUNDING GATE MOSFET
I LEAKAGE 2
0
$V_T$
$V_{GS}$

*FIG. 4*

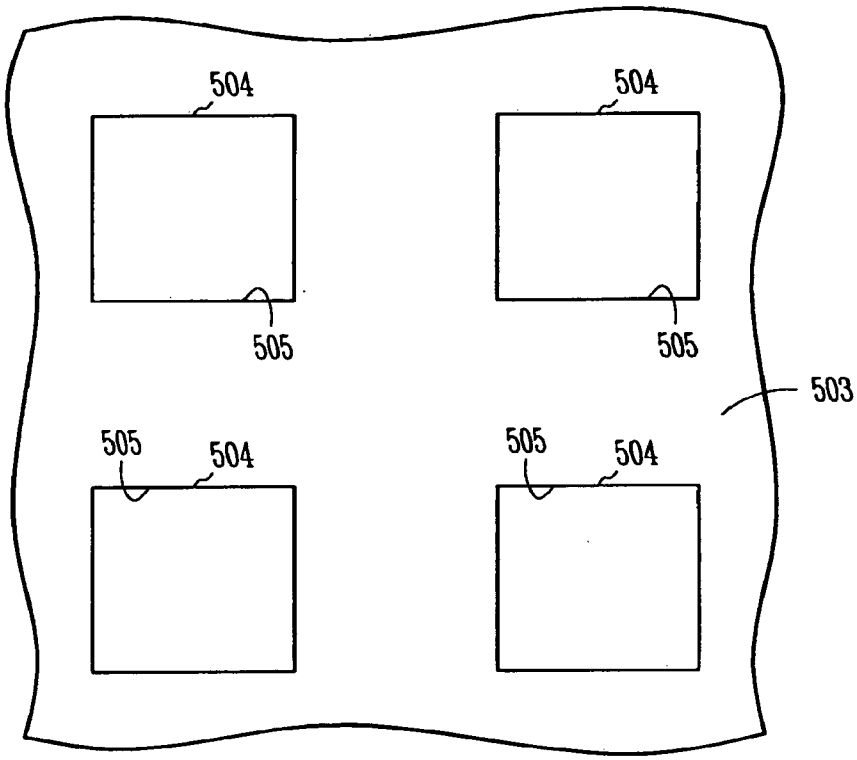

504
504
505
505
503
505
504
505
504

FIG. 5A

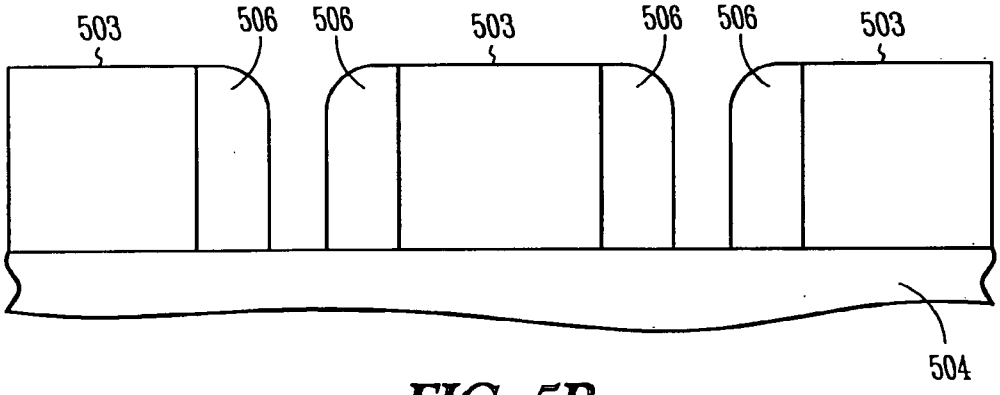

503
506
506
503
506
506
503
504

FIG. 5B

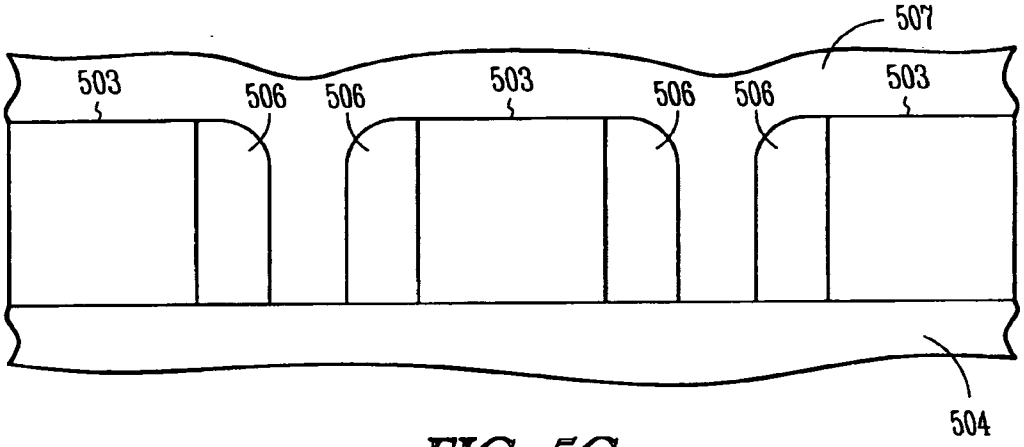

507
503
506
506
503
506
506
503
504

FIG. 5C

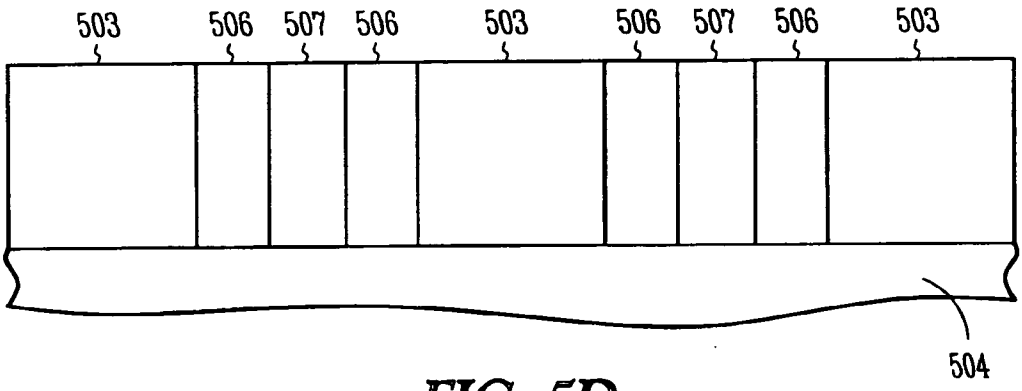

503
506
507
506
503
506
507
506
503
504

FIG. 5D

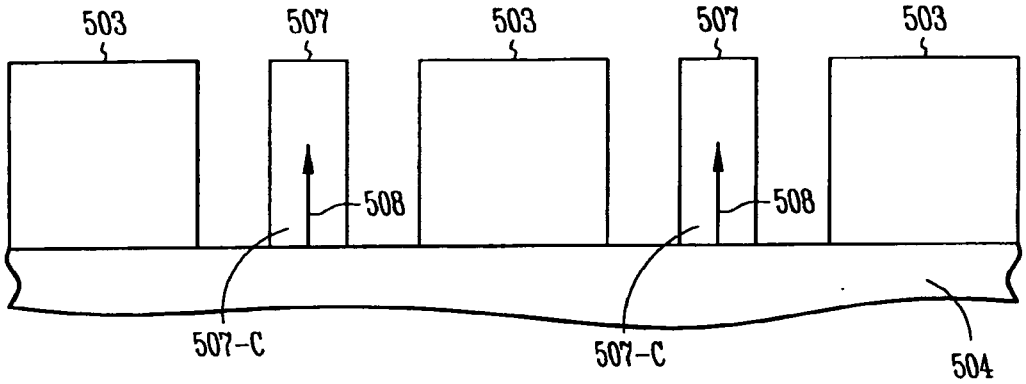



*FIG. 5E*

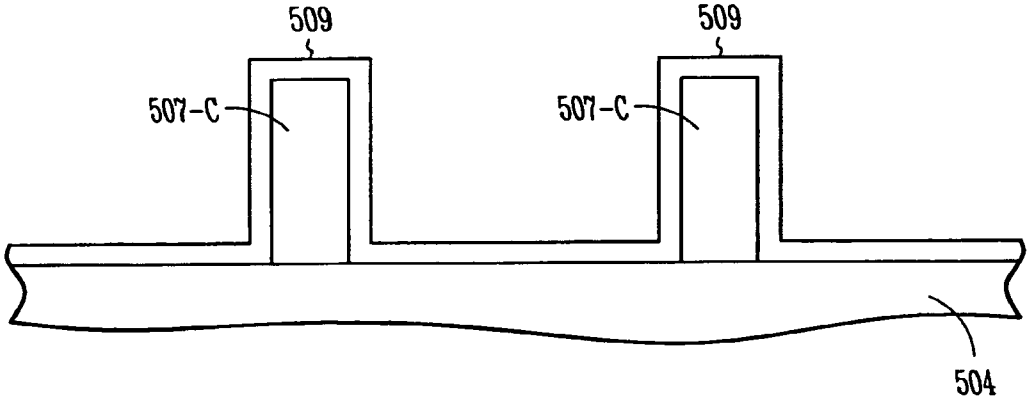



*FIG. 5F*

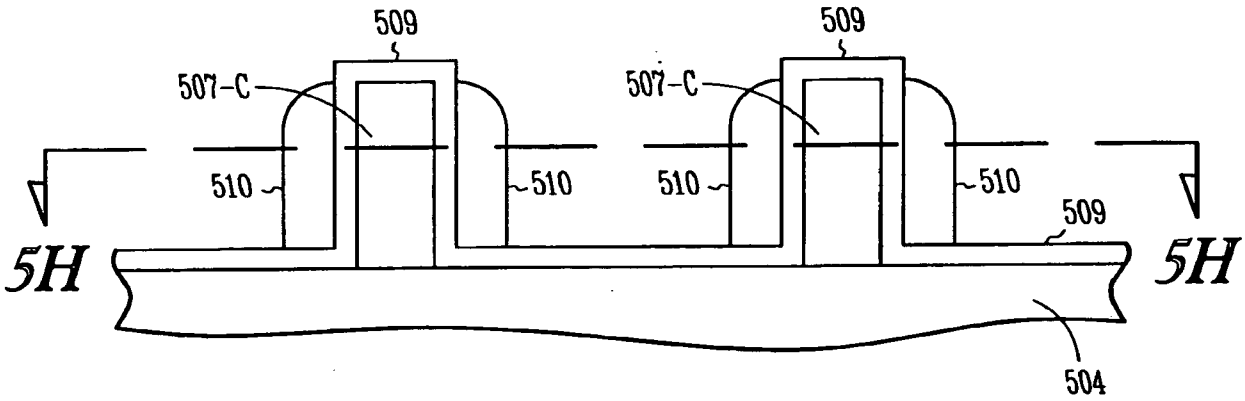

509
509
507-C
507-C
510
510
510
510
509
5H
5H
504

FIG. 5G

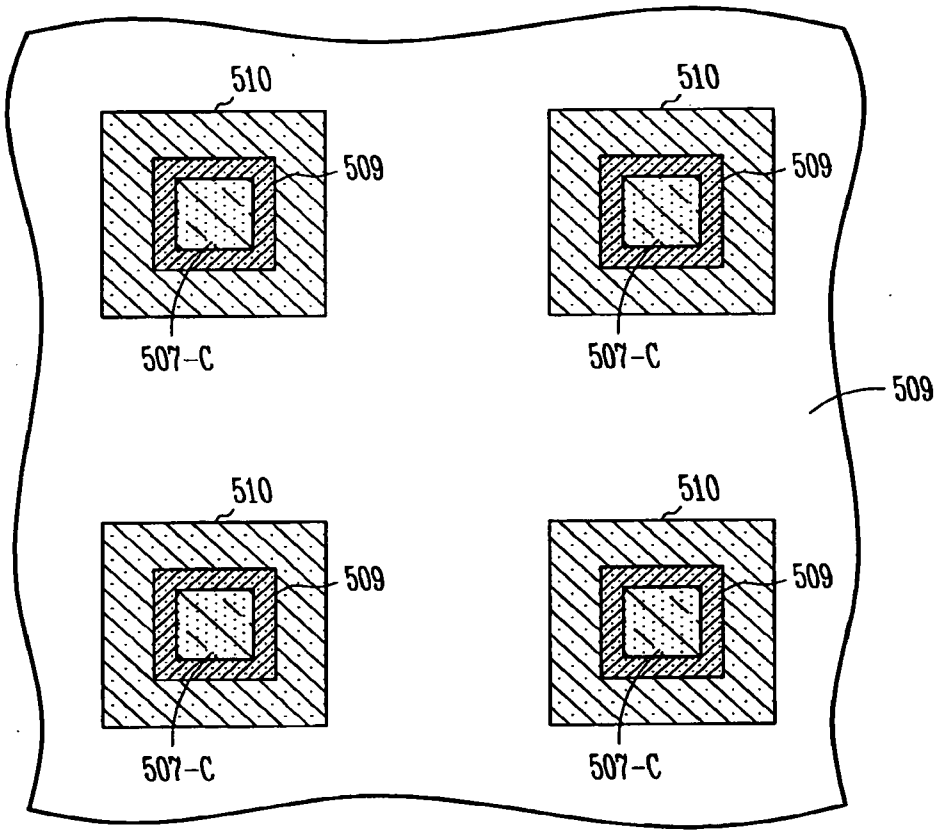

510
510
509
509
507-C
507-C
509
510
510
509
509
507-C
507-C

FIG. 5H

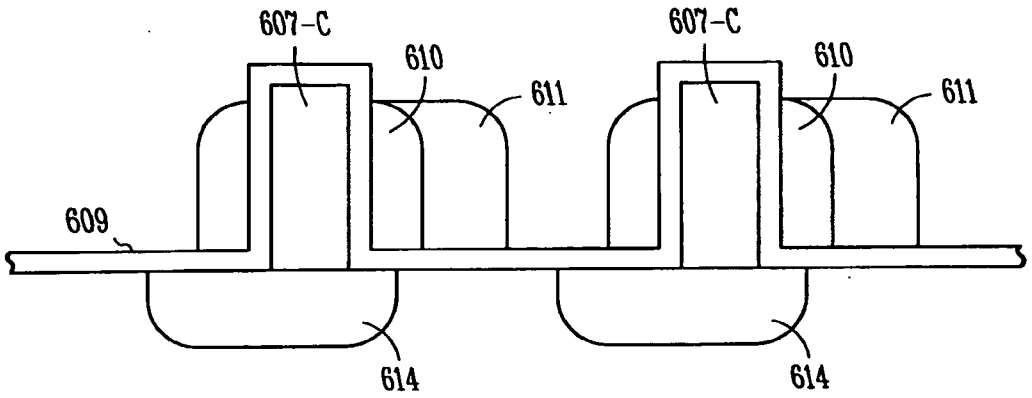



FIG. 6A

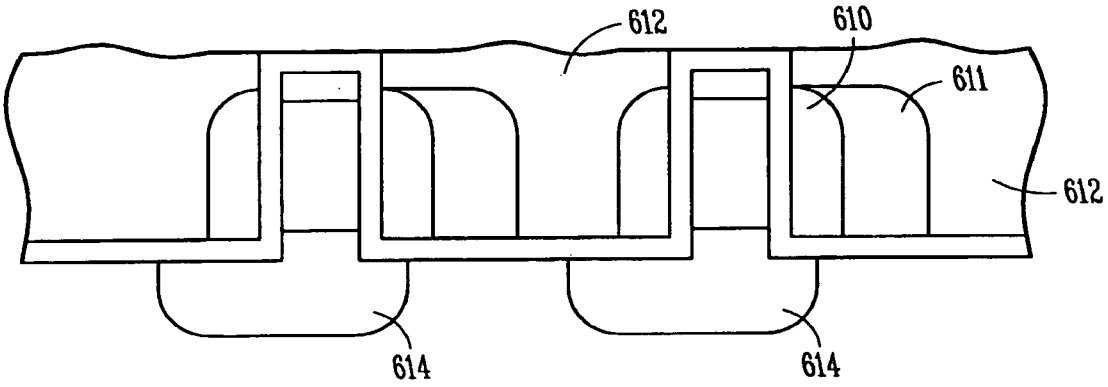



FIG. 6B

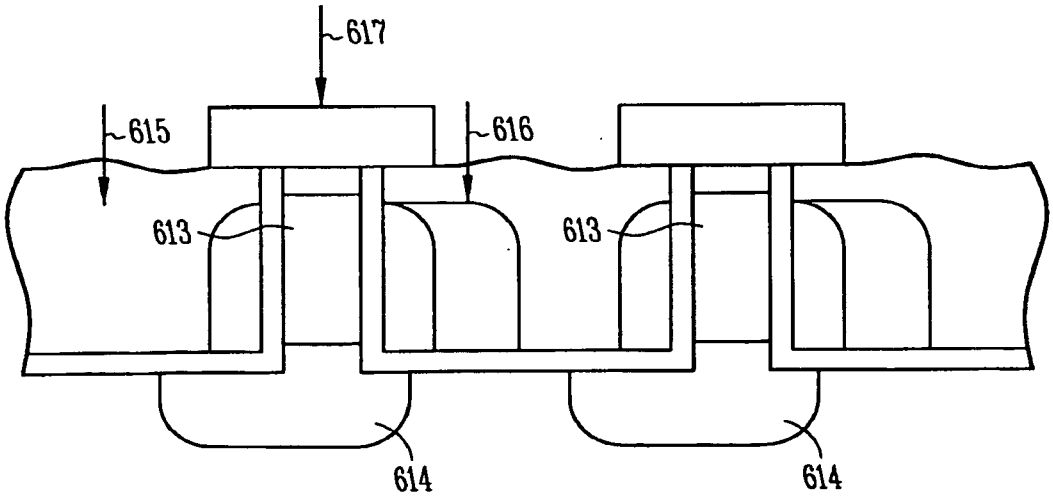



FIG. 6C

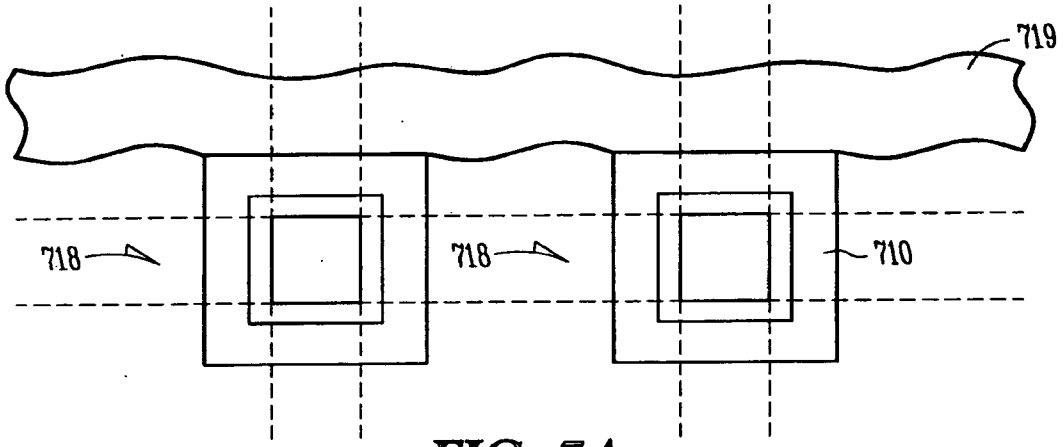

719
718
718
710

FIG. 7A

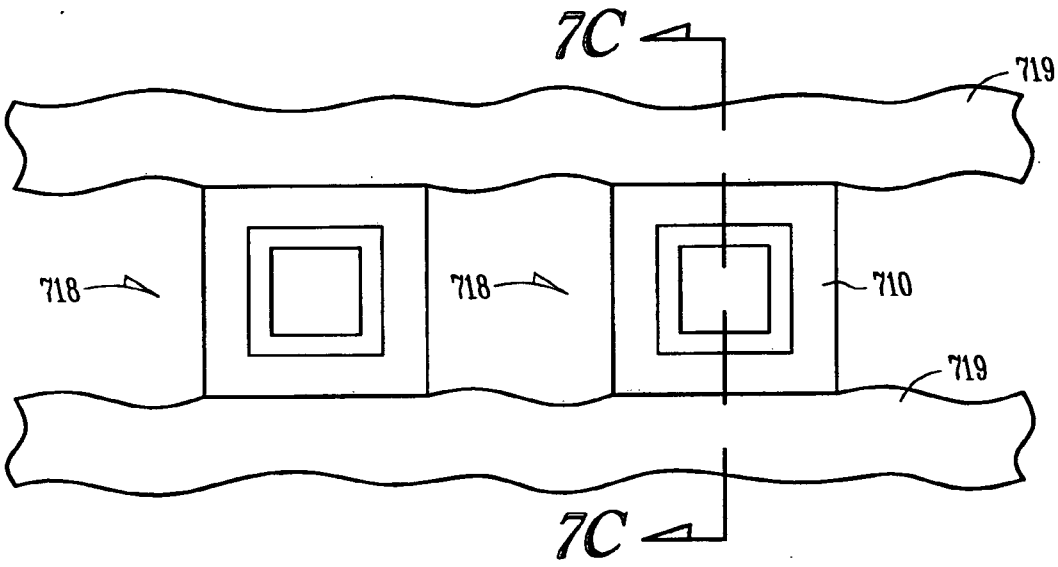
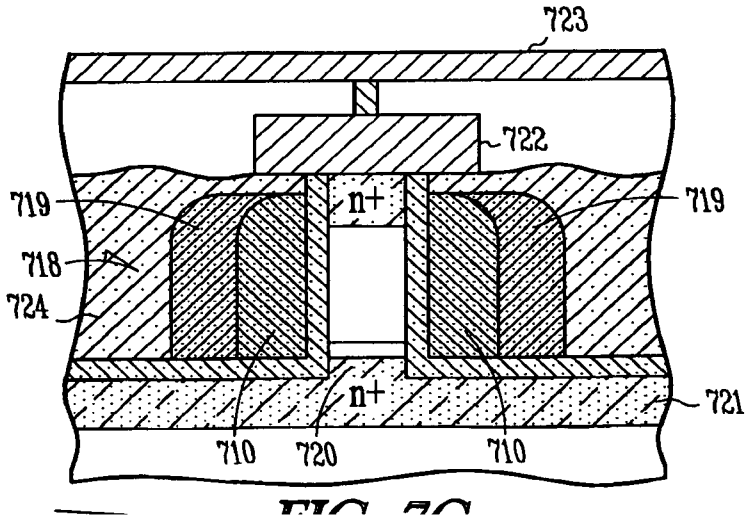

7C
719
718
718
710
719
7C

FIG. 7B


723
722
719
n+
719
718
724
n+
721
710
720
710

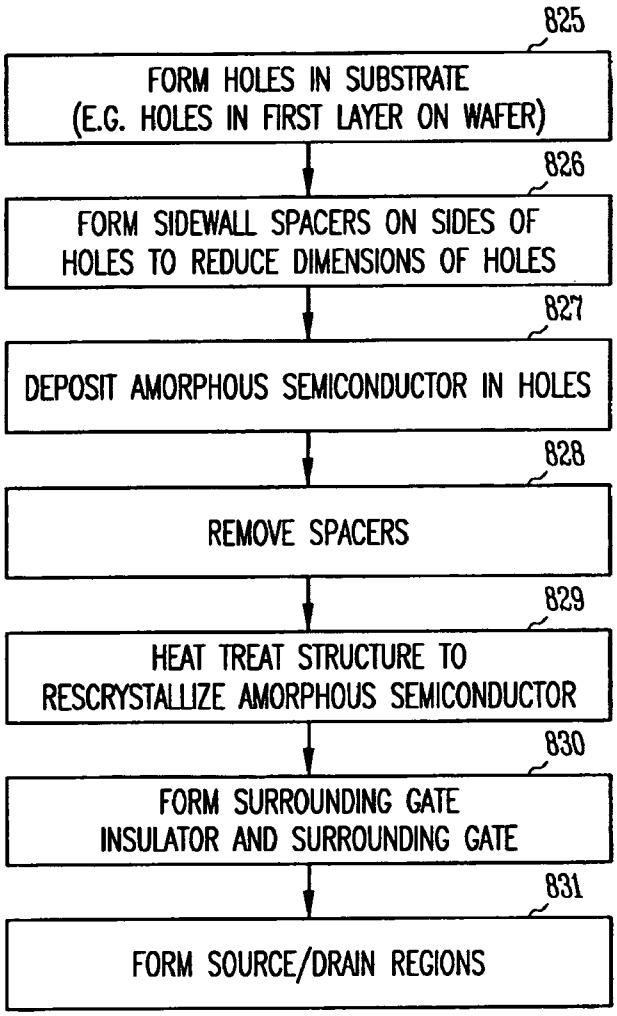

825
FORM HOLES IN SUBSTRATE (E.G. HOLES IN FIRST LAYER ON WAFER)
826
FORM SIDEWALL SPACERS ON SIDES OF HOLES TO REDUCE DIMENSIONS OF HOLES
827
DEPOSIT AMORPHOUS SEMICONDUCTOR IN HOLES
828
REMOVE SPACERS
829
HEAT TREAT STRUCTURE TO RESCRYSTALLIZE AMORPHOUS SEMICONDUCTOR
830
FORM SURROUNDING GATE INSULATOR AND SURROUNDING GATE
831
FORM SOURCE/DRAIN REGIONS

*FIG. 8*

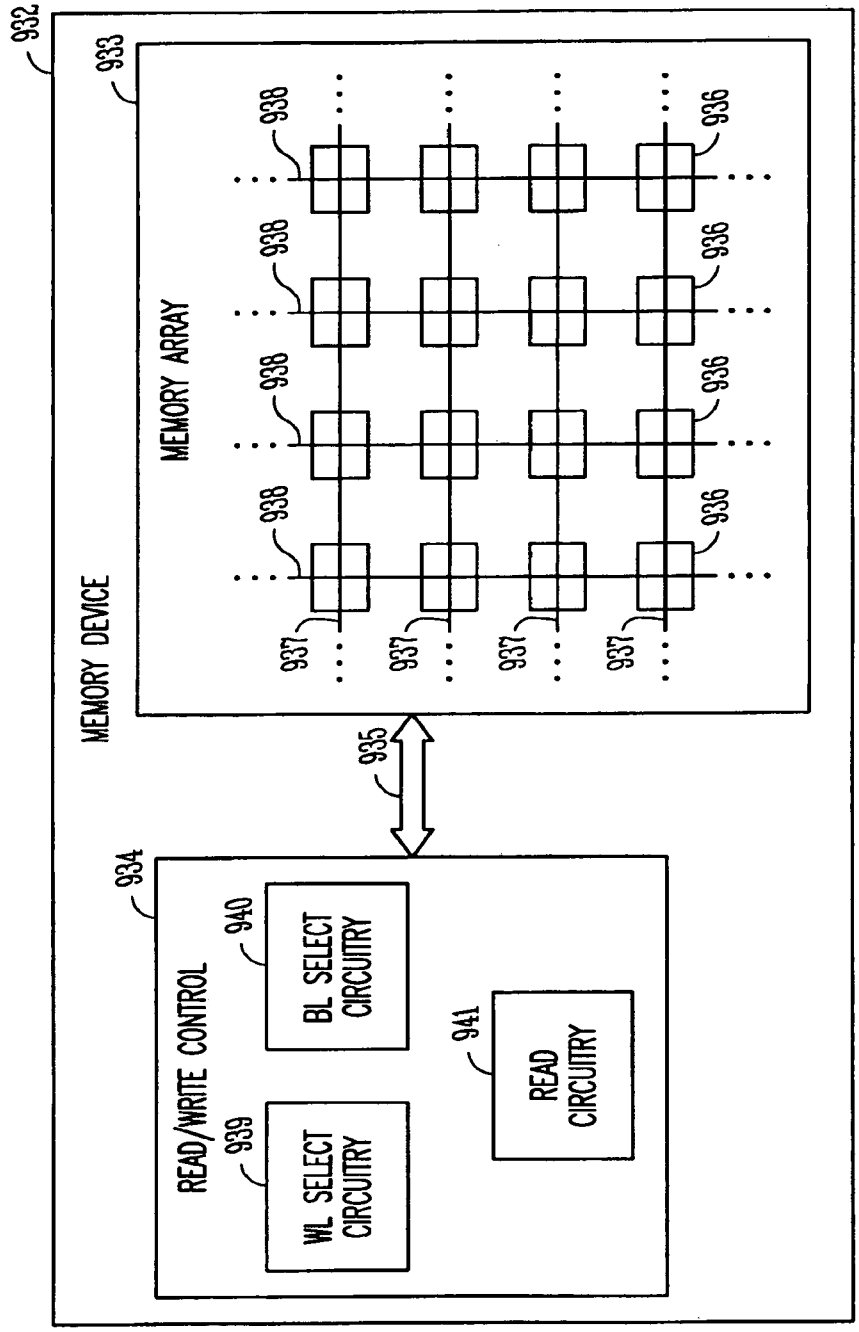

932
MEMORY DEVICE
933
MEMORY ARRAY
936
937
938
935
934
READ/WRITE CONTROL
939
WL SELECT CIRCUITRY
940
BL SELECT CIRCUITRY
941
READ CIRCUITRY

FIG. 9

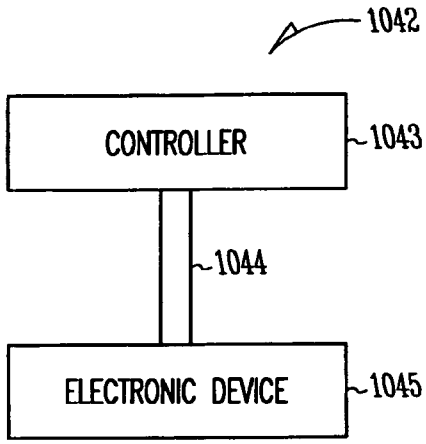

1042
CONTROLLER
1043
1044
ELECTRONIC DEVICE
1045

*FIG. 10*

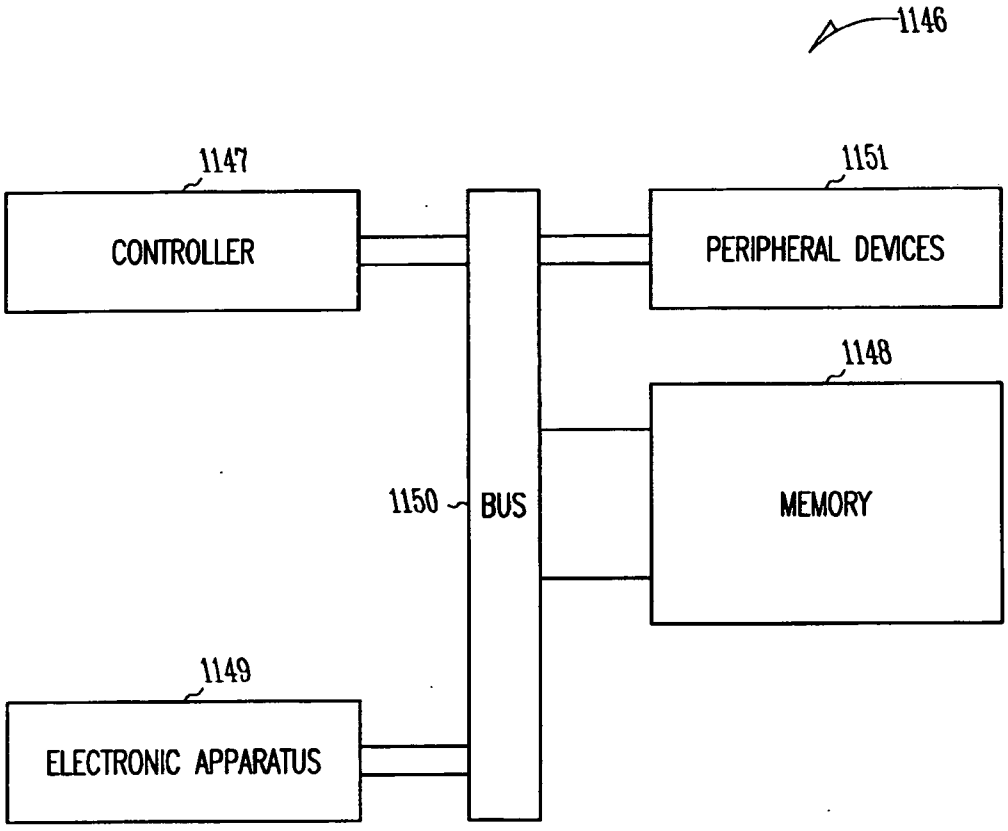

1146
1147
CONTROLLER
1151
PERIPHERAL DEVICES
1148
MEMORY
1150
BUS
1149
ELECTRONIC APPARATUS

*FIG. 11*