What is claimed is:

1. A microelectronic device, comprising:

an upper quantum well;

a lower quantum well separated from the upper quantum well by a barrier layer; and

a gate electrode proximate the upper quantum well.

2. The microelectronic device of claim 1, wherein at least one of said upper quantum well and said lower quantum well comprises indium gallium arsenide.

3. The microelectronic device of claim 1, wherein the barrier layer comprises indium aluminum arsenide.

4. The microelectronic device of claim 1, further including an upper quantum well contact coupled to the upper quantum well and a lower quantum well contact coupled to the lower quantum well.

5. The microelectronic device of claim 4, wherein the lower quantum well contact extends through the upper quantum well and is electrically isolated therefrom.

6. The microelectronic device of claim 1, wherein at least one of said upper quantum well and said lower quantum well is n-doped.

7. The microelectronic device of claim 1, wherein at least one of said upper quantum well and said lower quantum well is p-doped.

8. The microelectronic device of claim 1, wherein the gate electrode is adapted to modulate current density in the upper quantum well.

9. A method of fabrication a microelectronic device, comprising:

forming a lower quantum well;

forming a barrier layer proximate the lower quantum well;

forming an upper quantum well proximate the barrier layer; and

forming a gate electrode proximate the upper quantum well.

10. The method of claim 9, wherein forming the lower quantum well comprises forming an indium gallium arsenide lower quantum well.

11. The method of claim 9, wherein forming the upper quantum well comprises forming an indium gallium arsenide upper quantum well.

12. The method of claim 9, wherein forming the barrier layer comprises forming an indium aluminum arsenide barrier layer.

13. The method of claim 9, further including forming an upper quantum well contact coupled to the upper quantum well and forming a lower quantum well contact coupled to the lower quantum well.

14. The method of claim 13, wherein forming the lower quantum well contact comprises:

forming an opening through the upper quantum well;

depositing a dielectric material on sidewalls of the opening;

extending the opening through the barrier layer to expose a portion of the lower quantum well; and

depositing a conductive material in the opening.

15. The method of claim 9, further comprising doping at least one of said upper quantum well and said lower quantum well.

16. The method of claim 9, further comprising forming a top barrier layer between the upper quantum well and the gate electrode.

17. The method of claim 9, further comprising:

providing a microelectronic substrate;

forming a buffer layer on the microelectronic substrate; and

forming a bottom barrier layer on the buffer layer;

wherein forming the lower quantum well comprises forming the lower quantum well on the bottom barrier layer.

18. A system, comprising:

an integrated circuit device; and

a main memory;

wherein at least one of said integrated circuit device and said main memory includes a microelectronic device comprising an upper quantum well, a lower quantum well separated from the upper quantum well by a barrier layer; and a gate electrode proximate the upper quantum well.

19. The system of claim 18, wherein at least one of said upper quantum well and said lower quantum well comprises indium gallium arsenide.

20. The system of claim 18, wherein the barrier layer comprises indium aluminum arsenide.

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What is claimed is:

1. A microelectronic device, comprising:
an upper quantum well;

a lower quantum well separated from the upper quantum well by a barrier layer;

a gate electrode separated from the upper quantum well by a top barrier layer;

an upper quantum well contact extending through the top barrier layer and coupled to the upper quantum well; and

a lower quantum well contact coupled to the lower quantum well, wherein the lower quantum well contact extends through the top barrier layer and the upper quantum well and is electrically isolated therefrom with a dielectric material.

2. The microelectronic device of claim 1, wherein at least one of said upper quantum well and said lower quantum well comprises indium gallium arsenide.

3. The microelectronic device of claim 1, wherein the barrier layer comprises indium aluminum arsenide.

4. The microelectronic device of claim 1, wherein at least one of said upper quantum well and said lower quantum well is n-doped.

5. The microelectronic device of claim 1, wherein at least one of said upper quantum well and said lower quantum well is p-doped.

6. The microelectronic device of claim 1, wherein the gate electrode is adapted to modulate current density in the upper quantum well.

7. A method of fabrication a microelectronic device, comprising:
forming a lower quantum well;

forming a barrier layer proximate the lower quantum well;

forming an upper quantum well proximate the barrier layer;

forming a gate electrode separated from the upper quantum well by a top barrier layer;

forming an upper quantum well contact extending through the top barrier layer and coupled to the upper quantum well; and

forming a lower quantum well contact coupled to the lower quantum well comprising:
forming an opening through the top barrier layer and the upper quantum well;

depositing a dielectric material on sidewalls of the opening;

extending the opening through the barrier layer to expose a portion of the lower quantum well; and

depositing a conductive material to fill the opening.

8. The method of claim 7, wherein forming the lower quantum well comprises forming an indium gallium arsenide lower quantum well.

9. The method of claim 7, wherein forming the upper quantum well comprises forming an indium gallium arsenide upper quantum well.

10. The method of claim 7, wherein forming the barrier layer comprises forming an indium aluminum arsenide barrier layer.

11. The method of claim 7, further comprising doping at least one of said upper quantum well and said lower quantum well.

12. The method of claim 7, further comprising:
providing a microelectronic substrate;

forming a buffer layer on the microelectronic substrate; and

forming a bottom barrier layer on the buffer layer;

wherein forming the lower quantum well comprises forming the lower quantum well on the bottom barrier layer.

13. A system, comprising:
an integrated circuit device; and

a main memory;

wherein at least one of said integrated circuit device and said main memory includes a microelectronic device comprising an upper quantum well, a lower quantum well separated from the upper quantum well by a barrier layer; a gate electrode separated from the upper quantum well by a top barrier layer; an upper quantum well contact extending through the top barrier layer and coupled to the upper quantum well; and a lower quantum well contact coupled to the lower quantum well, wherein the lower quantum well contact extends through the top barrier layer and the upper quantum well and is electrically isolated therefrom with a dielectric material.

14. The system of claim 13, wherein at least one of said upper quantum well and said lower quantum well comprises indium gallium arsenide.

15. The system of claim 13, wherein the barrier layer comprises indium aluminum arsenide.