Claims

1. A pulse width modulation (PWM) system (2) comprising a plurality of module building blocks (4_1-4_4), wherein each module building block is connected to and controlled by a control board (6_1-6_4), each module building block comprises a set of function modules (8_1-8_5), provided with pulse width modulated phase outputs (10_1-10_5) adapted to be connected to predetermined loads, and wherein each module building block (4_1-4_4) is connected to a direct current (DC) link, and that the control boards (6_1-6_4) are connected to each other via a communication bus (12), one of the control boards is a master control board (6_1) and the others are slave control boards (6_2, 6_3, 6_4),
w h e r e i n that each slave control board (6_2, 6_3, 6_4) is configured to determine a fictive master board timer based upon timer information received from the master control board via said communication bus (12), and is further configured to synchronize the timer rate of a slave board timer (14_2, 14_3, 14_4) to a timer rate of the master control board, or of an external timer rate, such that said slave board time then is said fictive master board timer, and that said timer information further comprises interlacing angle information defining an interlacing point for each of the slave control boards receiving the timer information, wherein the interlacing angles of a plurality of control boards are determined in relation to each other such that the variation of at least one predetermined operation parameter, related to the loads connected to said pulse width modulated phase outputs of said function modules, is minimized,
wherein said timer information also comprises timer offset information defining a time offset between the master board timer (14_1) and the slave board timer (14_2, 14_3, 14_4), and wherein the slave control board (6_2, 6_3, 6_4) is configured to apply said time offset in the control of the pulse width modulated phase outputs (10_1-10_5), such that the position of a slave pulse width modulated phase output signal is controlled in relation to the fictive master board timer.

2. The system (2) according to claim 1, wherein at least two control boards, for which the interlacing angles are determined, are arranged to control function modules at different module building blocks.

3. The system (2) according to claim 1 or 2, wherein the interlacing angles are determined, by said master control board or by an external control unit, to control one type of load such that the interlacing angles designated to said one type of load are evenly

spread out between 0-360 degrees.

4. The system (2) according to any of claims 1-3, wherein said predetermined operation parameter is a capacitor voltage variation of a load, e.g. a step up/down chopper.

5. The system (2) according to any of claims 1-3, wherein said predetermined operation parameter is a DC-link voltage ripple of a one and/or three phase load, e.g. a voltage source converter.

6. The system (2) according to any of claims 1-5, wherein the master control board (6_1) comprises a master board timer (14_1) configured to generate a clock signal having a master timer rate, wherein each of the slave control boards (6_2, 6_3, 6_4) comprises a slave board timer (14_2, 14_3, 14_4).

7. The system (2) according to claim 1, wherein said slave board timers (14_2, 14_3, 14_4) are configured to continue running independently if the master board timer (14_1) is running or not, using the lastly received master timer rate and timer offset, and to resynchronize to the master timer rate, and to update the timer offset, when the master board timer (14_1) restarts, or changes.

8. The system (2) according to any of claims 1-7, wherein said communication bus (12) is an inter converter serial bus (ICE-bus).

9. The system (2) according to any of claims 1-7, wherein said communication bus (12) is internet protocol (IP) bus.

10. A method in a pulse width modulation (PWM) system (2) comprising a plurality of module building blocks (4_1-4_4), wherein each module building block is connected to and controlled by a control board (6_1-6_4), each module building block comprises a set of function modules (8_1-8_5), provided with pulse width modulated phase outputs (10_1-10_5) adapted to be connected to predetermined loads, and wherein each module building block (4_1-4_4) is connected to a direct current (DC) link, and that the control boards (6_1-6_4) are connected to each other via a communication bus (12), one of the control boards is a master control board (6_1) and the others are slave control boards

(6_2, 6_3, 6_4), c h a r a c t e r i z e d i n that the method comprises:

-determining, by each slave control board (6_2, 6_3, 6_4), a fictive master board timer based upon timer information received from the master control board via said communication bus (12),

-synchronizing the timer rate of the slave board timer (14_2, 14_3, 14_4) to the master timer rate or to an external timer rate, such that said slave board timer matches with said fictive master board timer,

wherein said timer information further comprises interlacing angle information defining an interlacing point for each of the slave control boards receiving the timer information, and the method further comprises:

-determining the interlacing angles of a plurality of control boards in relation to each other such that the variation of at least one predetermined operation parameter related to the loads connected to said pulse width modulated phase outputs of said function modules is minimized,

wherein said timer information further comprises timer offset information defining a time offset between the master board timer (14_1) and the slave board timer (14_2, 14_3, 14_4), the method further comprises:

-applying, by each of the slave control boards (6_2, 6_3, 6_4), said time offset when controlling the pulse width modulated phase outputs (10_1-10_5), such that the position of a slave pulse width modulated phase output signal is controlled in relation to the fictive master board timer.

11. The method according to claim 10, wherein at least two control boards for which the interlacing angles are determined are arranged to control function modules at different module building blocks.

12. The method according to claim 10 or 11, comprising determining the interlacing angles of slave control boards configured to control one type of load such that the interlacing angles designated to said one type of load are evenly spread out between 0-360 degrees.

13. The method according to any of claims 10-12, wherein said predetermined operation parameter is a capacitor voltage variation of a load, being e.g. a step up/down chopper.

14. The method according to any of claims 10-12, wherein said predetermined operation parameter is a DC-link voltage ripple of a one or three phase load, being e.g. a voltage source inverter.

15. The method according to claim 10, comprising continue running said slave board timers (14_2, 14_3, 14_4) independently if the master board timer (14_1) is running or not, using the lastly received master timer rate and timer offset, and resynchronizing to the master timer rate, and updating the timer offset, when the master board timer (14_1) restarts, or changes.

16. A rail-bound vehicle comprising one or many pulse width modulation systems (2) according to any of claims 1-9.