CLAIMS

1. A data link comprising:

a transmitter hardware module configured to receive a data stream, the transmitter hardware module further configured to convert units in the data stream from having a size of eight data bits to having a size of a predetermined number of data bits before transmitting the data stream in parallel transmission, the size of the predetermined number of data bits being of any whole number of 7 or less;

a receiver hardware module configured to receive the data stream from the transmitter hardware module, the receiver hardware module further configured to convert units in the data stream from having ~~-~~the size of the predetermined number of data bits to having the size of eight data bits;

a pulse detection module configured to detect transmission in the data stream from the transmitter hardware module of one or more units having a size beyond the predetermined number of data bits, the pulse detection module configured to emit an alarm indication signal upon detection of the one or more units having the size beyond the predetermined number of data bits; ~~and~~

a supervisory module configured to provide an alarm upon receiving the alarm indication signal from the pulse detection module~~.~~;

a switch matrix configured to scramble units in the data stream having the size of the predetermined number of data bits during transmission from the transmitter hardware module to the receiver hardware module; and

a pattern detector configured to detect transmission in the data stream from the transmitter hardware module of the one or more units having the size beyond the predetermined number of data bits before the data stream is received by the switch matrix.

2. The data link according to claim 1,

wherein the receiver hardware module is configured to prevent from receiving one or more additional data bits in excess of the predetermined number of data bits.

3. The data link according to claim 1 or claim 2,

wherein the receiver hardware module comprises a first-in-first-out ring buffer.

4. The data link according to any one of claims 1 to 3,

wherein the transmitter hardware module comprises a first-in-first-out ring buffer.

5. The data link according to any one of claims 1 to 4,

wherein a most significant bit pin of the transmitter hardware module is electrically connected to the pulse detection module.

6. The data link according to any one of claims 1 to 5,

wherein the predetermined number of data bits is 7.

~~7. The data link according to any one of claims 1 to 6, further comprising:~~

~~a switch matrix configured to scramble units in the data stream having the size of the predetermined number of data bits during transmission from the transmitter hardware module to the receiver hardware module.~~

~~8.~~7.The data link module according to claim ~~7~~1,

wherein data pins of the transmitter hardware module is mapped to data pins of the receiver hardware module using one or more map pattern codes.

~~9.~~8.The data link module according to claim ~~7 or claim 8~~1,

wherein the switch matrix is electrically connected to the supervisory module.

~~10. The data link module according to any one of claims 7 to 9, further comprising:~~

~~a pattern detector configured to detect transmission in the data stream from the transmitter hardware module of the one or more units having the size beyond the predetermined number of data bits before the data stream is received by the switch matrix.~~

~~11.~~9. A method of forming ~~the~~ a data link, the method comprising:

forming a transmitter hardware module configured to receive a data stream, the transmitter hardware module further configured to convert units in the data stream from having a size of eight data bits to having a size of a predetermined number of data bits before transmitting the data stream in parallel transmission, the predetermined number of data bits being of any whole number of 7 or less;

forming a receiver hardware module configured to receive the data stream from the transmitter hardware module, the receiver hardware module further

configured to convert units in the data stream from having the size of the predetermined number of data bits to having the size of eight data bits;

providing a pulse detection module configured to detect transmission in the data stream from the transmitter hardware module of one or more units having a size beyond the predetermined number of data bits, the pulse detection module configured to emit an alarm indication signal upon detection of the one or more units having the size beyond the predetermined number of data bits; ~~and~~

providing a supervisory module configured to provide an alarm upon receiving the alarm indication signal from the pulse detection module~~.~~;

providing a switch matrix configured to scramble units in the data stream having the size of the predetermined number of data bits during transmission from the transmitter hardware module to the receiver hardware module; and

providing a pattern detector configured to detect transmission in the data stream from the transmitter hardware module of the one or more units having the size beyond the predetermined number of data bits before the data stream is received by the switch matrix.

~~12.~~10. The method according to claim ~~11~~9,

wherein the receiver hardware module is configured to prevent from receiving one or more additional data bits in excess of the predetermined number of data bits.

~~13.~~11. The method according to claim ~~11~~ 9 or claim ~~12~~10,

wherein the receiver hardware module comprises a first-in-first-out ring buffer.

~~14.~~12. The method according to any one of claims ~~11~~ 9 to ~~13~~11,

wherein the transmitter hardware module comprises a first-in-first-out ring buffer.

~~15.~~13. The method according to any one of claims ~~11~~ 9 to ~~14~~12,

wherein a most significant bit pin of the transmitter hardware module is electrically connected to the pulse detection module.

~~16.~~14. The method according to any one of claims ~~11~~ 9 to ~~15~~13,

wherein the predetermined number of data bits is 7.

~~17. The method according to any one of claims 11 to 16, further comprising:~~

~~providing a switch matrix configured to scramble units in the data stream having the size of the predetermined number of data bits during transmission from the transmitter hardware module to the receiver hardware module.~~

~~18.~~15. The method according to claim ~~17~~9,

wherein data pins of the transmitter hardware module is mapped to data pins of the receiver hardware module using one or more map pattern codes.

~~19.~~16. The method according to claim ~~17 or claim 18~~9,

wherein the switch matrix is electrically connected to the supervisory module.

~~20. The method according to any one of claims 17 to 19, further comprising:~~

providing a pattern detector configured to detect transmission in the data stream from the transmitter hardware module of the one or more units having the size beyond the predetermined number of data bits before the data stream is received by the switch matrix.