RESERVE COPY.

PATENT SPECIFICATION

DRAWINGS ATTACHED

958,248

958,248

Date of Application and filing Complete Specification *May* 6, 1960.
No. 46089/63.
Application made in United States of America (*No.* 811476) *on May* 6, 1959.
(*Divided out of No.* 958,242)
Complete Specification Published May 21, 1964.

© Crown Copyright, 1964.

Index at Acceptance: Class H1, K(1A1:1C1:1CX:2S1:2S2:2S10,2S20:3E1:3J:3S:4C:5).
International Classification: H 01 l.

Semiconductor devices.

COMPLETE SPECIFICATION

We, TEXAS INSTRUMENTS INCORPORATED, of 13500 North Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to semiconductor devices and more particularly to semiconduotor devices containing a plurality of semiconductor wafers or layers in or on one surface of a relatively high impedance substrate for electrically isolating said wafers or layers from one another through said substrate.

The present invention is a semiconductor device comprising a plurality of semiconductor wafers or layers in or on one surface of a substrate which has a relatively high impedance for electrically isolating said wafers or layers from one another through said substrate, each of said wafers or layers including one or more discrete regions therein or thereon adapted to provide the electrical properties of at least part of one or more circuit elements, and an electrical interconnection between two of said circuit elements including an electrically conductive lead secured to one or more wafer or layer surfaces remote from said substrate.

Each wafer or layer which is in or on the substrate may include one or more circuit elements formed therein or thereon as described in parent British Patent Application No. 16071/60 (Serial No. 958242) from which the present application is divided, or British Patent Application No. 3633/60 (Seria' No. 945,734) and/or any of the divisional applications therefrom.

An embodiment of the invention will now be described, by-way of example, with reference to the accompanying drawings, in which:—

Fig. 1 illustrates a top plan view of a semiconductor device embodying the invention;

Figs. 2A-2C illustrate the circuit diagram of the semiconductor device of Fig. 1 and variations thereof which are described in detail in said parent British Patent Application No. 16071/60; (Serial No. 958,242) and

Figs. 3—6, inclusive, show cross sectional views of some of the circuit elements illustrated in Fig. 1, which circuit elements are described in detail in said parent British Patent Application No. 16071/60 (Serial No. 958,242).

With reference to the drawings, embodiments of the invention will now be described in detail in order to provide a better understanding of the principles of the invention and various forms and embodiments thereof.

With reference to Fig. 1, there is illustrated semiconductor wafers or layers 12 and 14 of single crystal semiconductor material mounted or secured on substrate 10, for example, by solder glass. The substrate 10 has a relatively high impedance for isolating the wafers or layers 12 and 14 from one another through said substrate and said substrate 10 may be intrinsic semiconductor material having a relatively high order of resistivity. The wafers or layers may be secured on the substrate or disposed in the substrate. According to the latter, the entire unit could be formed from a block of intrinsic semiconductor material into which doping impurities are diffused in the regions occupied by the wafers or layers 12 and 14, wherein the wafers or layers and the substrate are part of the same physical piece of semiconductor material.

A description of the circuit elements included in or on the wafers or layers 12 and 14 will not be given herein since these wafers or layers and elements are described in detail in said parent British Patent Application and are illustrated in Figs. 2A to 6 herein.

(Price 4s. 6d.)

However, in this embodiment, the wafer or layer 12 includes multi-emitter transistors TR2 and TR3, diffused resistors R1 and R3, bulk resistors R2 and R4, transistor TR1 and diode D3. The circuit elements included in wafer or layer 14 are capacitors C1 and C2, and diodes D2 and D7.

Electrical interconnections are made between two circuit elements included in or on one wafer or layer and between two circuit elements included in different wafers or layers by electrical leads secured to the wafer or layer surfaces remote from the substrate surface. This is illustrated by the electrical lead interconnecting the base region 20 of multi-emitter transistor TR2 to the emitter region 48 of transistor TR1 or diode D1 and the electrical interconnection between the emitter region 24 of multi-emitter transistor TR2 and the emitter region of muli-emitter TR3 or the electrical lead interconnecting the emitter region 22 of multi-emitter transistor TR2 and the capacitor C1. Further illustrations are the electrical lead interconnecting the emitter region of multi-emitter transistor TR3 and one region of the diode D3; and the electrical lead interconnecting the other region of the diode D3 and the capacitor C2. Also, external connections to the device are made by a coplanar arrangement of relatively flat leads 33, 40, 68, 38, 76, 74, 72 and 70 which coplanar array is parallel to the surface of the substrate 10. The relatively flat electrically conductive leads 33, etc. are electrically connected to various circuit elements included in or on the wafers or layers 12 and 14 as illustrated by the electrical interconnection between lead 72 and the base region 20 of multi-emitter transistor TR2.

More specifically, ohmic metal contacts 26, 28, 30, 56 and 60 are plated or evaporated onto desired regions of the wafer or layer surface and then the electrically conductive leads secured thereto. Also, substantially flat conductive leads 33, etc. may be soldered or alloyed to substrate 10 to provide the aforementioned coplanar arrangement of leads whereby certain substantially flat leads 68, 70, 72, 74 and 76 terminate at a spaced position from the wafers or layers 12 and 14 and certain substantially flat leads 33, 40 and 38 contact the underside of wafer or layer 12.

In the above manner, an assembly of a plurality of semiconductor wafers or layers is disposed in or on a substrate with interconnections between circuit elements in the same wafer or layer and interconnections between circuit elements in different wafers or layers and furthermore leads 33, etc. are provided for external connection to the device.

It must be emphasized that only one embodiment of the invention has been described and that other variations and modifications thereof may be made without departing from the scope of the invention as defined in the appended claims.

Reference is additionally made to our co-pending patent applications nos. 23279/63; 46086/63; 46087/63; 46088/63; and 46090/63 (Serial Nos. 958244, 958245, 958246, 958247 and 958249), also divided from said parent patent application.

Terms indicative of position, such as "on" and "overlying", are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor device could be used in any desired positional orientation.

WHAT WE CLAIM IS:

1. A semiconductor device comprising a plurality of semiconductor wafers or layers in or on one surface of a substrate which has a relatively high impedance for electrically isolating said wafers or layers from one another through said substrate, each of said wafers or layers including one or more discrete regions therein or thereon adapted to provide the electrical properties of at least part of one or more circuit elements, and an electrical interconnection between two of said circuit elements including an electrically conductive lead secured to one or more wafer or layer surfaces remote from said substrate.

2. A semiconductor device according to claim 1, including a co-planar array, parallel to said one surface, of substantially flat electrically conductive leads selected ones of which are electrically connected to selected ones of said circuit elements.

3. A semiconductor device according to either preceding claim, wherein one of said circuit elements is a transistor.

4. A semiconductor device according to any preceding claim, wherein one of said circuit elements is a diode.

5. A semiconductor device according to claim 3, or claims 3 and 4, wherein said transistor includes a base region and an emitter region contiguous therewith to form a P-N junction extending to said wafer or layer surface, or one of said wafer or layer surfaces, and there defining a first enclosed area, a collector region contiguous with said base region to form therewith another P-N junction extending to said wafer or layer surface and there defining another enclosed area surrounding said first enclosed area.

6. A semiconductor device according to claim 4 or claims 4 and 5, wherein said diode includes two regions of opposite conductivity types to form therebetween a P-N junction extending to said wafer or layer surface, or one of said wafer or layer surfaces, and there defining an enclosed area.

However, in this embodiment, the wafer or layer 12 includes multi-emitter transistors TR2 and TR3, diffused resistors R1 and R3, bulk resistors R2 and R4, transistor TR1 and diode D3. The circuit elements included in wafer or layer 14 are capacitors C1 and C2, and diodes D2 and D7.

Electrical interconnections are made between two circuit elements included in or on one wafer or layer and between two circuit elements included in different wafers or layers by electrical leads secured to the wafer or layer surfaces remote from the substrate surface. This is illustrated by the electrical lead interconnecting the base region 20 of multi-emitter transistor TR2 to the emitter region 48 of transistor TR1 or diode D1 and the electrical interconnection between the emitter region 24 of multi-emitter transistor TR2 and the emitter region of muli-emitter TR3 or the electrical lead interconnecting the emitter region 22 of multi-emitter transistor TR2 and the capacitor C1. Further illustrations are the electrical lead interconnecting the emitter region of multi-emitter transistor TR3 and one region of the diode D3; and the electrical lead interconnecting the other region of the diode D3 and the capacitor C2. Also, external connections to the device are made by a coplanar arrangement of relatively flat leads 33, 40, 68, 38, 76, 74, 72 and 70 which coplanar array is parallel to the surface of the substrate 10. The relatively flat electrically conductive leads 33, etc. are electrically connected to various circuit elements included in or on the wafers or layers 12 and 14 as illustrated by the electrical interconnection between lead 72 and the base region 20 of multi-emitter transistor TR2.

More specifically, ohmic metal contacts 26, 28, 30, 56 and 60 are plated or evaporated onto desired regions of the wafer or layer surface and then the electrically conductive leads secured thereto. Also, substantially flat conductive leads 33, etc. may be soldered or alloyed to substrate 10 to provide the aforementioned coplanar arrangement of leads whereby certain substantially flat leads 68, 70, 72, 74 and 76 terminate at a spaced position from the wafers or layers 12 and 14 and certain substantially flat leads 33, 40 and 38 contact the underside of wafer or layer 12.

In the above manner, an assembly of a plurality of semiconductor wafers or layers is disposed in or on a substrate with interconnections between circuit elements in the same wafer or layer and interconnections between circuit elements in different wafers or layers and furthermore leads 33, etc. are provided for external connection to the device.

It must be emphasized that only one embodiment of the invention has been described and that other variations and modifications thereof may be made without departing from the scope of the invention as defined in the appended claims.

Reference is additionally made to our co-pending patent applications nos. 23279/63; 46086/63; 46087/63; 46088/63; and 46090/63 (Serial Nos. 958244, 958245, 958246, 958247 and 958249), also divided from said patent patent application.

Terms indicative of position, such as "on" and "overlying", are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor device could be used in any desired positional orientation.

WHAT WE CLAIM IS:

1. A semiconductor device comprising a plurality of semiconductor wafers or layers in or on one surface of a substrate which has a relatively high impedance for electrically isolating said wafers or layers from one another through said substrate, each of said wafers or layers including one or more discrete regions therein or thereon adapted to provide the electrical properties of at least part of one or more circuit elements, and an electrical interconnection between two of said circuit elements including an electrically conductive lead secured to one or more wafer or layer surfaces remote from said substrate.

2. A semiconductor device according to claim 1, including a co-planar array, parallel to said one surface, of substantially flat electrically conductive leads selected ones of which are electrically connected to selected ones of said circuit elements.

3. A semiconductor device according to either preceding claim, wherein one of said circuit elements is a transistor.

4. A semiconductor device according to any preceding claim, wherein one of said circuit elements is a diode.

5. A semiconductor device according to claim 3, or claims 3 and 4, wherein said transistor includes a base region and an emitter region contiguous therewith to form a P-N junction extending to said wafer or layer surface, or one of said wafer or layer surfaces, and there defining a first enclosed area, a collector region contiguous with said base region to form therewith another P-N junction extending to said wafer or layer surface and there defining another enclosed area surrounding said first enclosed area.

6. A semiconductor device according to claim 4 or claims 4 and 5, wherein said diode includes two regions of opposite conductivity types to form therebetween a P-N junction extending to said wafer or layer surface, or one of said wafer or layer surfaces, and there defining an enclosed area.

7. A semiconductor device according to any preceding claim, wherein one of said circuit elements is a resistor including an elongated portion of semiconductor material of one conductivity type bounded by a P-N junction.

8. A semiconductor device according to any preceding claim, wherein a region adapted to provide the electrical properties of part of a circuit element is one plate of a capacitor, an oxide of silicon dielectric overlies said plate and conductive material overlies said dielectric.

9. A semiconductor device according to any preceding claim, wherein said substrate is intrinsic semiconductor material.

H. D. FITZPATRICK & CO.,
Chartered Patent Agents,
3 Gray's Inn Square, London, W.C.1.
and
94 Hope Street, Glasgow, C.2.

Sheerness: Printed for Her Majesty's Stationery Office, by Smiths Printers and Duplicators.—1964.
Published at the Patent Office, 25 Southampton Buildings, London, W.C.2., from which copies may be obtained.

