

ABSTRACT

A semiconductor memory device includes a bit line extending in a first direction, an active pattern on the bit line, the active pattern including first and second vertical portions facing each other in the first direction and a horizontal portion connecting the first and second vertical portions, first and second word lines on the horizontal portion between the first and second vertical portions, the first and second word lines extending in a second direction crossing the first direction, a gate insulating pattern between the first and second word lines and the active pattern, and a capacitor connected to each of the first and second vertical portions, the capacitor including a first electrode pattern connected to one of the first and second vertical portions, a second electrode pattern on the first electrode pattern, and a ferroelectric pattern between the first electrode pattern and the second electrode pattern.

FIG. 5A