

Stack Cell Memory Device and Method of Forming the Same

ABSTRACT

A single transistor stacked DRAM memory cell 8 includes a transfer gate 18 formed over a semiconductor region 10 and insulated therefrom. A bit line contact region 16 is disposed in the semiconductor region adjacent a first edge of the transfer gate 18. A storage node contact region 14 is disposed in the semiconductor region 10 adjacent a second edge of the transfer gate 18. The storage node contact region 14 is spaced from the bit line contact region 16 by a channel region. A cylindrical spacer region 28 is disposed over the semiconductor region 10. This spacer region 28 surrounds the storage node contact region 14 so as to expose this contact region 14. A conductive storage node 22 surrounds inner, outer and upper portions of the spacer region 28 and is electrically coupled to the storage node contact region 14. A conductive plate 26 is capacitively coupled to the storage node 22.

Figure 1(a)