ABSTRACT OF THE DISCLOSURE

**APPARATUS FOR PACKAGE REDUCTION IN STACKED CHIP AND BOARD ASSEMBLIES**

An electronic device package having semiconductor die-carrying interposer substrates in a stacked configuration. Each interposer substrate bears at least one die mounted by its active surface to a surface of the interposer substrate and wire bonded to terminals on the opposing substrate surface through an opening in the interposer substrate. Two interposer substrates are placed together with die-carrying sides outward and electrically connected with conductive elements extending transversely therebetween to form an interposer assembly, the interposer assembly bearing conductive elements extending transversely from one of the interposer substrates for connection to a carrier substrate. The space between the interposer substrates may be filled with a dielectric underfill material, as may the space between the interposer assembly and the carrier substrate to which the former is mounted.

[FIG. 2]