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(54) I.F. AMPLIFIER FOR AM-FM RADIO RECEIVERS

(71) We, GENERAL ELECTRIC COMPANY, a corporation organised and existing under the laws of the State of New York, United States of America, of 1 River Road, Schenectady 12305, State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to an IF amplifier for an AM-FM radio receiver which in particular may be of the super-heterodyne variety wherein a single filter capacitor may be used (1) as an adjustable current source, hereinafter also termed "main current source" or "B+" type bias supply" or simply "bias supply" which provides substantially the entire collector, emitter and base d.c. operating current for most of the I.F. amplifier stages in both FM operation and AM operation, and also for the FM local oscillator and FM mixer in FM operation; (2) for providing the AGC function in AM operation, and (3) for providing the AFC function in FM operation. The "B+" type bias is supplied through the adjustable current source which adjusts the "B+" type bias in accordance with the FM-AM detector output. In the FM mode setting, automatic frequency control of the local oscillator is provided by the main current source. In the AM mode setting, automatic gain control of the IF amplifier and of the AM section of the tuner is provided by the main current source. The designation "bias supply" should not be mistaken to mean a supply of merely small bias currents, such as transistor base currents. The current delivered by the bias supply to the IF amplifier is quite substantial. Also, the designation "B+ type" should not be confused with the primary d.c. power supply line for the receiver (+6 volts),

which is designated B+ in the usual manner. The invention has preferred application to integrated circuit fabrication.

The invention is particularly suited to integrated circuit (IC) fabrication of such receivers, wherein increasing complexity on the "chip" and decreasing complexity off the "chip" is favoured.

Radio receivers for AM and FM operation have been fabricated for some time using solid state elements. With the advent of integrated circuit devices, the use of "discrete" transistors has tended to decline in favour of integrated circuit devices. Generally, integrated circuit devices, wherein active and passive components are formed in a monolithic semiconductor chip, have been proposed for individual functional components of radio receivers, such as the audio amplifiers, the intermediate frequency amplifiers, etc. One arrangement is known, wherein most of the functions are performed on a single chip, and is described in U.K. Patent Specification No. 1,338,201, hereinafter termed, by the name of its inventor, Peil I, the "I" serving to distinguish from the present invention, in which the same William Peil is co-inventor. In the Peil I arrangement, separate filters are provided for AFC, AGC and bias supplies. Embodiments of the present invention employ many principles common to Peil I, but departs therefrom particularly in mode conversion and filtering of the control functions and bias supplies. Also, the IF amplifier configuration herein disclosed, is considerably simplified vis-a-vis Peil I.

The present invention is an intermediate frequency (IF) amplifier for a radio receiver capable of receiving in the AM mode or FM mode, the IF amplifier being d.c. coupled and arranged to amplify signals at frequencies both in a frequency range centred about the higher FM IF, and centered about the lower AF IF, the amplifier comprising:

(a) a plurality of consecutive stages, said

consecutive stages considered collectively, having wide band a.c. gain embracing both said ranges, each such consecutive stage including an emitter coupled transistor pair comprising an input transistor and an output transistor, there being provided for each such pair an emitter-resistor arranged to pass the emitter currents of both transistors of its respective pair, those ends of said emitter-resistors which are remote from the respective emitters being connected together and to an earth-line or earth-point,

(b) a primary bus through which is to be applied d.c. collector operating current to the individual transistors of said consecutive stages,

(c) a secondary bus for passing d.c. base current to the output transistor of each said pair and for applying degenerative feedback to provide balanced biasing of each said transistor pair,

(d) means for establishing said secondary bus at a potential which is a function of the potential of said primary bus and for applying said degenerative feedback to said secondary bus, including

(1) a collector load resistance connected between said primary bus and the collector of the output transistor of the last stage of said consecutive stages, and

(2) a degenerative feedback resistance having one end connected to the collector of the output transistor of the last stage and the other end connected to the base of said output transistor of the last stage and to said secondary bus,

wherein the said collector load resistance and feedback resistance, and the circuits associated with said consecutive stages are so designed or selected, that

(A) when there is applied *via* said primary bus the aforesaid d.c. collector operating current in the FM-mode at a first value lying in a first range of current values, the primary bus is at a first d.c. potential, lying in a first range of potential values, with respect to earth, and the I.F. amplifier exhibits a first value of overall I.F. amplifier a.c. gain, and

(B) when there is applied *via* said primary bus the aforesaid d.c. collector operating current in the AM-mode at a second and different value lying in a second range of current values, the primary bus is at a second and different d.c. potential, lying in a second range of potential values, with respect to earth, and the I.F. amplifier exhibits a second and different value of overall I.F. amplifier a.c. gain lying in a range of gain values,

(C) the second value of gain being variable in accordance with the d.c. potential on said secondary bus, as derived from said potential of second value on said primary

bus and as transmitted *via* said secondary bus to said output transistors.

An embodiment of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:—

Fig. 1 is a simplified drawing primarily in block diagram form, of an AM-FM receiver incorporating the invention, and

Figs. 2a and 2b are together a diagram (Fig. 2) of the same embodiment subject to a minor modification, and show the receiver in the form of an essentially complete circuit diagram, omitting only the AM-FM detector and the audio amplifier.

A radio receiver incorporating the invention is shown in simplified block diagram form in Fig. 1. The radio receiver takes the general form of a superheterodyne receiver and is intended for AM-FM operation. Of particular interest are those features directed to the main current source (adjustable current source) 29, the IF amplifier, and to automatic frequency control filtering and automatic gain control filtering.

Signal conversion to a pair of fixed intermediate frequencies is achieved in the blocks 11, 12 and 13 comprising the "front end" or tuner of the receiver. The FM mixer 11 is shown with an input connection 14 to which FM signals may be supplied, typically from a whip antenna, while the AM mixer 13 is shown without external provision for the reception of AM signals. Normally, the AM mixer 13 depends upon the pick-up of a ferrite element contained within the unit. The FM mixer 11 receives load oscillations from an FM local oscillator 12 and produces an output at a fixed intermediate frequency (IF) of 10.7MHz; this IF (to the exclusion of other frequencies) is developed by the IF filter 15 connected to the output of FM mixer 11. The AM mixer 13, which also includes an AM local oscillator, produces an output at a fixed intermediate frequency of 455 KHz. The AM output is applied to the intermediate frequency filter 16. The AM mixer is provided with a pair of AGC connections to the "primary control bus" or primary bus 18, and the "secondary control bus" or "secondary bus" 19, whose many other functions will be described in greater detail below. The AM mixer receives its B+ currents from the main power supply (6V) of the radio receiver. The tuner is provided with means, not shown, for selecting AM or FM mode operation in conjunction with other mode selection elements of the radio receiver.

The filtered IF frequency output from the FM filter 15 or the AM filter 16, is then applied to the input of the IF amplifier 10 whose connections will now be described.

The IF amplifier 10 is of plural two-transistor-stages and has substantial d.c.

feedback. It comprises the differentially connected NPN transistor pairs Q1, Q2; Q5, Q6; and Q7, Q8. The input signal is applied to the base of transistor Q1 having its emitter coupled to ground through emitter load resistance 17, and its collector coupled to primary bus 18 which provides B+ type bias. The bus 18, as will be described, is also used to provide gain control in the sense that the overall FM IF gain is greater than the overall AM IF gain, and to provide automatic gain control of the individual stages of the IF amplifier in AM operation. The base of Q1 is connected via the windings 15B and 16B of the filters 15 and 16 to the secondary bus 19. The output of Q1, which appears at its emitter and across the emitter load resistance 17, is applied to the emitter of Q2. The base of Q2 is coupled to the secondary control bus 19 used to provide balanced biasing to the differential stages and for secondary AGC. The bus 19 is by-passed to ground by a 1 μ f bypass or filter capacitor 31. The collector of Q2 is coupled through a collector load resistance 20 to the bus 18. With another stage of IF amplification normally intervening, the signal output from the collector of transistor Q2 is then applied to the transistor Q5 in the next to last stage of the IF amplifier 10. This stage has the same general configuration as the first stage and is also subject to automatic gain control. In particular, the input signal is applied to the base of Q5, the collector is returned to the primary bus 18 for B+ type bias and for gain control (overall FM gain vs overall AM gain; AGC in AM) purposes, and the emitters of Q5 and Q6 are connected together and led to ground through emitter load resistance 21. Signal coupling from Q5 and Q6 is achieved by this interconnection. The base of Q6 is led to the secondary control bus 19, and the collector of Q6 is led through a collector load resistance 22 to the primary bus 18.

The IF amplifier is provided with feedback for reducing drift; a d.c. feedback resistance 23 coupled between the collector of Q6 and the secondary bus 19. The secondary bus 19, in turn, is coupled to the bases of the even-numbered transistors (Q2 . . . Q6 and even Q8) and is also coupled via the winding 15B and 16B of filters 15 and 16 to the base of Q1. The d.c. connection between the busses 18 and 19 causes the bus 19 to have a voltage which varies with the d.c. voltage present on the primary control bus 18, and provides a convenient means of gain control of the IF amplifier in AM operation, and achieving additional automatic gain control in the AM mixer (inclusive of the AM oscillator) in the AM mode. As will be seen hereinafter, the current and voltage relations are as

follows: Bus 18 is at higher potential (+2.4 volts) and carries greater current in the FM-mode; but is at lower potential (+1.65 volts approximate nominal) and carries lesser current in the AM-mode. Bus 19 is also at higher potential in the FM-mode than in the AM-mode. In the AM-mode, further distinction is made between: condition (1) normal IF input signal-higher IF gain-"normal AGC"; and condition (2) stronger IF input signal-lower IF gain-"stronger AGC". In condition (1) the bus 18 carries the higher current at a higher potential (nominal +1.65 volts) and the bus 19 is also at higher potential, than in condition (2). This is to be expected, because condition (1) should more nearly approach FM-mode, than condition (2). By these connections, amplified output signals at one of the two IF frequencies appear at the collector of Q6, and are applied to a final stage of the IF amplifier 10.

The final IF stage employs the transistors Q7, Q8. They are differentially connected; the base of Q7 is coupled to the collector of Q6 and the base of Q8 is coupled to the secondary AGC bus 19. The emitters of Q7, Q8 are connected together and led through the further current source 24, which is a constant current source, to ground. The output current appearing at the collector of Q8 (and also of Q7) contains either FM or AM signals at their respective IF frequencies; the collector currents of Q7 and Q8 are passed to B+ (6V), that of Q8 via a tuned circuit 25 suitable for final amplification, filtering and signal coupling to the AM-FM detector 26; thus transistors Q7 and Q8 receive their B+ currents from the main power supply line (6 volts) of the radio receiver; not from the primary bus 18.

Noting the 1 μ f value of bypass capacitor 31, and the 2K (kilohm) value of the feedback resistor 23, it follows that in either the AM or FM, the feedback is completely bypassed, so that the IF amplifier operates at these IFs at full a.c. gain, which is necessarily greater than its d.c. gain by virtue of the full effective feedback for d.c. purposes.

The AM-FM detector 26 is designed to provide detection for either an AM or FM signal dependent upon the mode setting and produces an output voltage containing d.c. components, and also both the audio and unfiltered intermediate frequency components. In particular, in the AM mode, a dynamic d.c. output voltage appears on line 65 which is proportional to the AM carrier amplitude, while in the FM mode a dynamic d.c. output voltage appears on line 65, which is proportional to the FM error in centre tuning. As the radio receiver is newly tuned in to a desired broadcast station, for example in the course of changing from one broadcast station to 130

another, in either the AM-mode or the FM-mode, the dynamic d.c. voltage on line 65 will usually include a relatively slowly-varying dynamic constituent of the long-time-constant, 400 μ f capacitor 30 — connected between the primary bus 18 and earth (ground) — requires some time to recharge and to accommodate to the changed situation.

By "static level" or "static signal" (static d.c. voltage or static d.c. current) at a particular stage in the radio receiver, is meant that d.c. level which exists at that particular stage with the radio receiver turned on, but detuned from receiving any broadcast station. By "dynamic level" or "dynamic signal" is meant the change in d.c. level, relative to the static level, at that particular stage, which change results from tuning the radio receiver to receive a broadcast station.

More particularly, the line 65 will carry the dynamic d.c. voltage — in the AM-mode proportional to the AM carrier, in the FM-mode proportional to the FM error in centre tuning — superimposed on a static d.c. voltage level which is provided in part or in whole by means contained within the current source 29. Referring preliminarily to Fig. 2 the static level is provided by the +1.2 volt d.c. source to pad 53, and thence via a resistor 56 to the line 65 and also to base of the NPN-transistor Q25, which receives the output signal of the AM-FM detector via line 65. The AM-FM detector 36, especially if it of the type shown in Peil I, will also make a contribution to establish the static level on line 65, in either AM-mode or FM-mode. The +1.2 volt d.c. source may be considered to be a secondary reference d.c. potential source, with the +6 volt source considered as the primary power supply source, and the earth-point or earth-line, considered as the primary reference line or primary reference point.

The static level on line 65, together with the dynamic d.c. component inclusive of the long time-constant dynamic d.c. constituent which appears on line 65, make a definite contribution towards establishing the magnitude of the d.c. output voltage and output current of the main current source 29. However, as will be seen hereinafter more dominant in establishing the ranges — one range of higher d.c. output voltage (+2.4 volts nominal) and higher d.c. output current in the FM-mode, another range of lesser d.c. output voltage (+1.65 volts nominal) and lesser d.c. output current in the AM-mode — for the main current source 29, is a primarily static signal applied to the current source 29 (see both Fig. 1 and 2) via a mode selection switch 32 and a 2K resistor

58. The signal is said to be "primarily static" for reasons now to be described; the magnitude and significant of this signal is determined in a most realistic manner not at the switch 32, but rather to the "right" (in the sense of Fig. 1 or Fig. 2) of the resistor 58.

Referring again preliminarily to Fig. 2, but considering Fig. 1 and 2 concurrently, in the FM-mode, the switch 32 places, via line 66 (which may be considered to be a "mode switching bus" 66), ground potential on the "left" of the resistor 58. At its "right", the resistor 58 is connected to the emitter of the NPN-transistor Q26, whose base is connected to the secondary d.c. reference potential source +1.2 volts. As has been stated previously herein, the d.c. equivalent circuit between base and emitter of a transistor is represented by a semiconductor diode, which takes a voltage difference (called " V_{BE} -drop") of a magnitude which is substantially fixed, and is substantially independent of the d.c. base current. For integrated transistors, the usual typical value for the V_{BE} -drop is taken at about 0.7 volts. Therefore, with the base of the transistor Q26 at +1.2 volts, its emitter will be at +0.5 volts, and hence the emitter current, i.e. the current through the 2K resistor in the FM-mode will be 0.25 milliamperes (ma). Hence in the FM-mode, the "primarily static" signal is in fact a purely static signal, 0.25 ma on a current-basis, 0.5 volts on a voltage basis. The 0.25 ma is also deemed to be the collector current of Q26.

In the AM-mode, the resistor 58 is at both its "left" (via line 66) and its "right" at the potential of bus 18, i.e. nominally +1.65 volts. The transistor Q26 cannot conduct emitter current under these conditions — recall its base is at +1.2 volts — and indeed this is the desired result; Q26 should cut off. Hence in the AM-mode, on a current basis, which is a more realistic basis, the primarily static signal is zero ma. On a voltage basis, the signal is the potential of bus 18 (V_{18}) which contains a dynamic component, which however does not affect the desired result, namely cut-off of Q26.

Continuing briefly the description of the operation of the transistor Q26 — and continuing to digress from the description of the detector 26 and the IF amplifier 10 — the fact of its conduction in the FM-mode and non-conduction in the AM-mode, establishes a higher range of potentials in AM-operation than in FM-operation at the collector of Q26, and hence at the base of the PNP output-transistor Q27 of the main current source 29. Tied together with the base of Q27 at circuit junction point 94 are: (1) the collector of NPN transistor Q24 which makes a composite dynamic plus

static contribution to establishing the potential of the base of the output PNP-transistor Q27, in accordance with V_{B5} , the output signal (on line 65) of the AM-FM detector 26; (2) the collector of Q26, which as just stated establishes for Q27 the higher (AM-mode) or lower (FM-mode) ranges of base potential ($V_{B/Q27}$); (3) the together-connected base and collector of PNP-transistor Q23, which in effect constitutes a diode.

The emitter of transistor Q23 — in effect the anode of the diode just mentioned — is connected via the 820 ohm resistor 51 to 6 Volt B+ line; the resistor 51 and diode-connected transistor Q23 form a collector-load impedance in common to Q24 and Q26, whereby the potential at the base of the output transistor Q27 is completely established. Q27 inverts the relative magnitudes of these voltage ranges; thus the range of $V_{C/Q27} = V_{18}$ (voltage at collector of Q27) is relatively higher (+2.4V nominal) in the FM-mode, and relatively lower in the AM-mode (+1.65V nominal). The operation of Q26, Q24 and Q27 has just been given on a voltage-basis; on a current basis, it will be given when the main current source 29 is described in greater detail. "Nominal" voltages are given for $V_{C/Q27}$ for several reasons; for one, we are dealing with ranges; for another, even the +2.4 and +1.65 volt values are subject to drift with any drift in the B+ 6V (and for that matter in the +1.2V) due to fluctuation in voltage in the power line mains, or due to aging of a battery used instead. The radio receiver operates correctly despite such drifts; it compensates by d.c. feedback arrangement and by AFC or AGC action. For a third reason, it must be remembered that Q27 is primarily a current-oriented device, and not a voltage-oriented device; hence $V_{C/Q27} = V_{18}$ is established by whatever equivalent d.c. resistance is seen looking "outward" from the collector of Q27; such equivalent d.c. resistance depends on tolerance variations of the transistors and resistors; the radio receiver is designed also to operate correctly despite component variations. The output of PNP-transistor 27 ($V_{C/Q27} = V_{18}$) is specified in terms of voltages (+2.4 volts or +1.65 volts nominal), rather than currents, because voltages are readily measured in operational use, whereas currents are not. Thus the ratings in terms of nominal voltages, rather than currents, are given for the benefit of the person who tests the radio receiver — as is customary in literature published by the radio manufacturer — more so than the benefit of the person who designs the radio receiver. Also, in radio manufacturer's literature, the d.c. voltage ratings are customarily stated in the absence of radio signal, that is under static conditions.

The sense of change in the composite static plus dynamic levels of the voltages on lines 18 to 65 are important. For example, in the AM mode are increasing strength of IF signal to the first stage Q1 of the amplifier 10 causes an increased voltage on line 65 which reduces the voltage on line 18 thus reducing the amplifier gain and thus the output signal of the IF amplifier and the voltage on line 65.

Considering the AM-FM detector 26, its detected output voltage is filtered to remove high frequency components, and as so filtered, is a.c. coupled to the audio amplifier 27. The amplifier 27 then produces an output for driving the capacitively coupled loudspeaker 28. The output of detector 26 before filtering, i.e. containing IF ripple components, audio, d.c. components, is combined with a selectable static d.c. level by means internal to block 26. The resulting composite static plus dynamic signal is coupled via line 65 to the main current source 29, which responds to this signal, and also the primarily static signal on line 66. The current source 29 then supplies an "adjustable" current to the bus 18 as a function of the detected output quantities. The d.c. output level of source 29 is tied in with mode selection, being smaller for AM operation (1.65 volts nominal) and higher (2.4 volts nominal) for FM operation. Since the detected signal is superimposed on these settings, two ranges of voltages will be produced on the primary bus 18. As will be shown in detail below, the AM voltage setting is selected to be one in which the IF amplifier stages exhibit a substantial gain variation. The FM voltage range setting produces a higher IF gain, but with some gain variation due to the d.c. changes which are proportional to the AFC voltage. Since these changes are relatively small and occur only during pull-in (or out) of the AFC loop, the variation is not objectionable. The voltage setting for FM is accordingly one which provides the requisite variation in B+ bias to provide automatic frequency control action of the local FM oscillator 12.

The overall control functions in AM and FM modes of operation may now be summarized. The primary bus 18 performs the five functions of providing B+ bias for the FM mixer and local oscillator, B+ biasing for the IF amplifier stages (Q1, Q2; Q5, Q6), automatic frequency control of the FM local oscillator 12, automatic gain control of the IF stages and, finally, an automatic gain control of the AM local oscillator contained in block 13. The secondary AGC bus 19, while primarily serving to assure d.c. stability of the IF amplifier and to co-operate with the primary bus 18 to provide AGC for the IF amplifier 10, also provides for

additional automatic gain control of the AM mixer 13.

The consolidation of functions on the bus 18 permits a single capacitor coupled to bus 18 to perform a plurality of functions. Capacitor 30 (400 μ f, 4v) is that capacitor. Capacitor 30 has a value selected to provide the requisite B+ bypass of bus 18 for the IF stages connected thereto and provides AGC and AFC filtering of IF ripple and audio stemming from detector 26. Its value is selected to provide the requisite AFC time constant for AM and the requisite AFC time constant for FM. The AM and FM time constants are normally chosen to have approximately the same value, the values being suitable for the dial tuning process, wherein time constants of one half-second or so are customary. The time constants are thus adequate for IF decoupling and for ripple filtering.

The practical embodiment is illustrated in greater detail in Fig. 2. The arrangement is adapted for integrated circuit (IC) fabrication. The partitioning places the FM tuner, the capacitors, inductors, tuned circuits, FM- or AM-mode selection switches, and the filters for signal separation and for the control functions off the IC chip. The FM-tuner, i.e. the FM local oscillator 12 and the FM mixer being "off the chip", implies that the respective transistors Q12 and Q11, as well as the resistors in the circuits of Q12 and Q11, are discrete. The balance of the receiver, including the AM local oscillator and mixer; the IF amplifier 10, the AM-FM detector 26, the audio amplifier 27, and the main or adjustable current source 29, are on the chip. For brevity, the details of the AM-FM filter or tuned circuit 25, the AM-FM detector 26, and the audio amplifier 27 have not been indicated. The AM-FM detector may take several forms. A suitable form is that illustrated in Peil I, as previously stated.

Reverting to the on-the-chip/off-the-chip arrangements of components of Fig. 2, it should be noted that the components stated to be off-the-chip in the preceding paragraph, insofar as they are returned to earth, they are so returned to an off-the-chip earth. This is true even of the resistors contained in the circuits of the FM local oscillator 12 and the FM mixer 11. Components which are on-the-chip, insofar as they are returned to earth, are connected to on-the-chip earth. The conductor 70 is the on-the-chip earth line. Notice that the earth-line 70 connects to a pad 70A, and then continues electrically as off-the-chip earth-line 70¹, and moreover an arrow appears in the conductor 70¹ to indicate direction of direct current flow. This convention is used for other conductors which appear on-the-chip, connect to a pad, and thence continue electrically off-the-

chip. Note for example the B+ 6V which is designated as 72 and without arrow-on-the-chip, and as 72¹ and with arrow off-the-chip. In the subsequent description, where on-the-chip and off-the-chip location of a conductor is not important, the conductor will be simply identified by reference numeral without prime in collective sense, i.e. intended to apply to both the on-the-chip and the off-the-chip part of the conductor, e.g. primary bus 18, secondary bus 19, B+ 6V-line 72 etc.

Another convention applicable to Fig. 2, concerns the capacitance-values of the capacitor shown therein. Utilizing the practice of radio manufacturers, unless otherwise specified, capacitance values less than 1 are in microfarads (μ f), and capacitance values greater than 1 are in picofarads (pf).

The IF amplifier 10 of Fig. 2 is modified vis-a-vis the IF amplifier 10 of Fig. 1 in the following respects:

(1) Whereas in Fig. 1, the emitters of the transistors Q7 and Q8 — the final IF stage — are returned to earth through the additional current source 24, a constant current source, in Fig. 2 a simple resistor 24¹ provides the return path. Either a resistor, or a constant current source can be utilized in Fig. 1 or Fig. 2.

(2) In Fig. 1, input from the FM mixer 11 to the base of Q1 is via a transformer 15 whose primary winding 15A is part of a tuned circuit, whereas its secondary winding 15B is shown untuned. Similarly, input from the AM mixer 13 is via a transformer 16 whose primary winding 16A is part of a tuned circuit, whereas the secondary winding 16B is shown untuned. Moreover, the direct current path from the secondary bus 19 to the base of Q1 is via the entire winding 16B, and then the entire winding 15B, these two windings being d.c. connected in series, or cascade. In Fig. 2, the FM mixer 11 is provided with a tank circuit 41 which itself is comprised of two tuned circuits, of which the first includes an inductance 41A and the second includes an inductance 14B. The two tuned circuits are inter-coupled by a capacitor 81. IF input from the inductance 41B to the base of Q1 is from the indicated lower, tapped-down portion 41C of the winding 41B, via conductor 74. The AM mixer 13A — it is separately designated as such in Fig. 2, the AM local oscillator being separately designated by 13B — is provided with a tank circuit 50 having a primary inductive winding 50A itself a part of a tuned circuit, and a secondary winding 50B inductively coupled to the winding 50A. The winding 50B, considered *per se*, is not in parallel with a tuning capacitor, but instead is coupled via a capacitor 82 to another tuned circuit which includes inductance 50C. IF input from the inductance

50C to the base of Q1, is from the lower, tapped-down portion 50D of the inductance 50C, via line 73¹ through the winding portion 41C in the FM mixer circuit, and then

5 via the aforementioned line 74. The direct current path from the secondary bus 19 to the base of Q1 is via the inductance portion 50D, line 73, the inductance portion 41C, and line 74.

10 In Fig. 2, the FM mixer 11 is shown at the lower lefthand portion of the drawing. The FM signals are coupled to the input terminal 14, coupled through input tuned circuit 40 to the base of mixer NPN transistor Q11. The emitter of Q11 is grounded, and the collector is coupled through the output tuned circuit 41 to the base of IF input transistor Q1, as described above.

20 The signals appearing at the base of the mixer Q11 are mixed with oscillations derived from the FM local oscillator 12. The FM local oscillator comprises the NPN transistor Q12, coupled in emitter common configuration, and the tank circuit 42 coupled to the collector thereof. Oscillations from the local oscillator are coupled through capacitor 43 to the base of Q11.

25 FM selection is achieved by the switching means 44. In the AM position, the means 44 removes the B+ bias supplied by primary bus 18 from both the mixer transistor Q11 and the local oscillator transistor Q12. In the FM position, the nominal 2.4 volts on bus 18 (during FM) is applied to the collector of the mixer Q11 through inductance 41A of the tuned output circuit 41, and through the tank circuit 42 to the collector of local oscillator Q12. Suitable base bias for both Q11 and Q12 are also provided.

30 The FM mixer-local oscillator configuration is essentially conventional except that the circuit frequency is allowed to remain B+ bias dependent (i.e. dependent on V_{b+}), and no effort has been made to remove that dependency. The circuit values indicated on the figure provide for adequately sensitive AGC operation to satisfy conventional home receiver requirements.

35 As has been stated in the preceding paragraph, the FM local oscillator is conventional, and therefore its characteristics are known. The local oscillator 12 is tuned above the frequency of the received FM radio frequency signal. The current I_{Q12} drawn by the local oscillator transistor Q12, from the primary bus 18 increases or decreases, as the voltage on bus 18, V_{b+} , increases or decreases, respectively.

40 The IF amplifier 10 of Fig. 2 has been previously detailed, save for the addition of one stage of amplification.

45 The additional stage includes the transistors Q3 and Q4; the stage is configured similar to the lowest order stage, except that the input to the base of Q3 is by a con-

ductor connection to the collector of Q2. Similarly, the output from the collector of Q4 is conductor-coupled to the base of Q5.

Thus the inter-stage coupling is by conductor connection; the coupling within a given stage is by way of conductor-connecting together the emitters, with an in-common resistor to earth; and the connections from base to the secondary bus 19 are conductor connections for the even-numbered transistors, even Q8; and even for Q1, its base-to-bus 19 connection is d.c. wise in effect a conductor-connection (via the inductance windings 41C and 50D).

70 The AM mixer 13A is illustrated at the upper lefthand portion of the drawing. It comprises a four quadrant multiplier, having differentially paired transistors Q13, Q14; Q15, Q16 in the upper rank and Q17, Q18 in the lower rank. The AM signal derived from the input tuned circuit 45 is applied to the base of one lower rank transistor Q17 which is at the d.c. potential of the secondary AGC bus 19. The other lower rank transistor is coupled to the secondary AGC bus 19 and by-passed to ground by capacitor 31. Thus the secondary bus 19 provides automatic gain control for the AM mixer 13A. The paired emitters of Q17, Q18 are returned to ground through the current source CS which provides delayed automatic gain control. The controlled current source CS comprises the transistor Q19, diode D1, and resistances 47 and 48. The transistor Q19 has its emitter grounded, its base coupled through diode D1, and resistance 48 to the FM terminal of switch 32. In AM operation, the switch 32 couples the resistor 48, via mode switching bus 66, to the AGC bus 18. The collector of Q19 is coupled through resistance 47 to the emitter of Q17, Q18. The controlled current source CS thus provides a measure of additional AGC to the AM mixer, "delayed additional AGC" or normal AGC depending on the mode of operation of the diode D1.

75 Continuing with the upper rank of the AM mixer 13A, the paired transistors Q13, Q14 and Q15, Q16 receive AM signal injection into their paired emitters from the lower rank pair Q17, Q18 and local oscillator injection into their bases. The local oscillator 13B comprises a pair of differentially connected transistors Q20, Q21, whose emitters are coupled to ground through current source Q22 and whose collectors are returned to the 6 volt B+ bus through small (100 ohm) resistances. The transistors Q20, Q21 are cross-coupled collector to base, and one collector (Q20) is coupled to the oscillating tank circuit 49. The local oscillator (13B) output is coupled from Q20 to the bases of upper rank transistors Q14, Q15 where mixing takes place. The mixer output is derived from the collector of Q16, and

applied through tuned circuit 50 to the base of Q1 (the circuit path including the FM tuned circuit 41). The base of Q22 is coupled to the mode switching bus 66, i.e. in effect to the primary bus 18; thus the local oscillator 13B is also subjected to automatic gain control.

The mode switch 32 controls the AM section of the tuner. The switch 32 is a single pole, double throw switch, having one terminal grounded and the other coupled to the bus 18. The pole is coupled through resistance 48 to the diode D1. Operation of the switch 32 to the ground position, back biases the diode D1 and cuts off current injection from current source Q19, thus cutting off all current to the AM mixer. Operation of the switch 32 to the other position, on the other hand, permits current to flow into the current source Q19 and activates the AM section of the tuner. Mode switches 32 and 44 operate in synchronism.

The adjustable or main current source 29 is in the lower righthand portion of Fig. 2b. It comprises transistors Q23 to Q27, and resistive and capacitive components 51 to 58. It comprises an adjustable current reference and the current source proper, which is controlled by that reference. The reference will be described first.

The adjustable reference comprises a diode connected transistor Q23, whose emitter is returned to the B+ bus 72 (+6 volts) through resistance 51. The current path from Q23 is completed from node 94 to ground through two paths. One path is through Q24, whose current is in turn controlled through Q25. The emitter of Q24 is returned to ground through resistance 52 and its base is held at a constant value of +1.2 volts by connection to the supply source (+1.2V) coupled to the pad 53. The pad 58 is also provided with a large (160 μ f) filter capacitor for hum reduction and signal decoupling, relative to the audio amplifier.

The current flow in Q24, as noted, is adjusted by Q25 in response to the AM-FM detector output. The output of the AM-FM detector 26 is coupled via line 65 to the base of Q25, whose emitter is led through 600 ohm resistance 55 to the emitter load resistance of Q24. The base of Q25 is returned through resistance 56 to +1.2 volts at pad 53. The collector of Q25 is coupled through a load resistance 57 to the B+ 6V bus 72. The detected signal from the detector 26 is thus coupled to the base of Q25, where by shared emitter load coupling, a signal induced change is produced in emitter current in Q24, and a corresponding change produced in the reference current in Q23. This mechanism operates in both the AM and FM settings to cause a change in the current flow in current reference Q23,

greater direct current in FM and lesser direct current in AM.

The mode switching adjustment of Q23 from a low current output for AM to a high current output for FM is provided by the transistor Q26. The collector of Q26 is coupled to the base-collector of Q23, and its base is returned to the +1.2 volt source at pad 53. The emitter of Q26 is led through resistance 58 and bus 66 to the pole of the FM mode switch 32. Earthing the mode switch for FM mode operation causes Q26 to conduct and steps the current in Q23 to a new plateau thereby raising the voltage on bus 18 by about three-quarters of a volt. Switching the pole of 32 to the AM position turns off Q26, and reduces the current of what is in effect the diode Q23. In either position of the mode switch 32, the current in Q23 is controlled by the detected output, but within different respective current ranges.

The final element in the adjustable current source 29 is the source of current itself. This is the transistor Q27 whose emitter is coupled through resistance 57 to the B+ 6V bias source. Its base is coupled to node 94, i.e. the base-collector of Q23, and its collector is coupled to the bus 18. Thus there are two current paths which both begin at the B+ 6V point and lead respectively to and including the emitter-base junction of Q27 on the one hand and to and including the emitter-base junction of Q23 on the other hand. These two current paths are more or less in shunt with each other; they are not exactly in shunt because Q25 diverts some current. Thus resistances 57 and 51 are scaled to produce equal junction potentials and to produce equal voltage drops. As may be seen in Fig. 2, the resistance values of the respective resistors 57 and 51 are 100 ohms and 820 ohms, i.e. substantially in inverse proportion (1:8) to their transistors' current-carrying capacities and areas. The geometry of Q27 is scaled to be 8 times that of Q23, the ratio of their emitter currents is the same, and the emitter current of Q27 is somewhat less than, but still about, 8 times that in the reference Q23.

In either AM or FM setting, the current available to the bus 18 flows through Q27, and is made dependent on the detected output and mode setting. As earlier noted, the nominal B+ bias on bus 18 for AM operation is about 1.65 volts, and that for FM operation is 2.4 volts.

While the invention may take other forms, the foregoing design is particularly economical of outboard components, and thus of overall cost. Assuming like performance requirements, the cost of a completed AM-FM radio receiver using a single chip with the indicated partitioning is substantially less than the costs in a non-integrated format.

Reference is made to our co-pending Application No. 2681/75 (Serial No. 1,503,171) from which this application was divided and which discloses and claims a current source/load combination for use in an AM-FM radio receiver as disclosed herein, and to Application No. 41909/77 (Serial No. 1,503,173) also divided from 2681/75 (Serial No. 1,503,171) and which discloses and claims a current source as disclosed herein.

WHAT WE CLAIM IS:—

1. An intermediate frequency (IF) amplifier for a radio receiver capable of receiving in the AM mode or FM mode, the IF amplifier being d.c. coupled and arranged to amplify signals at frequencies both in a frequency range centered about the higher FM IF, and centered about the lower AM IF, the amplifier comprising:

(a) a plurality of consecutive stages, said consecutive stages considered collectively, having wide band a.c. gain embracing both said ranges, each such consecutive stage including an emitter coupled transistor pair comprising an input transistor and an output transistor, there being provided for each such pair an emitter-resistor arranged to pass the emitter currents of both transistors of its respective pair, those ends of said emitter-resistors which are remote from the respective emitters being connected together and to an earth-line or earth-point,

(b) a primary bus through which is to be applied d.c. collector operating current to the individual transistors of said consecutive stages,

(c) a secondary bus for passing d.c. base current to the output transistor of each said pair and for applying degenerative feedback to provide balanced biasing of each said transistor pair,

(d) means for establishing said secondary bus at a potential which is a function of the potential of said primary bus and for applying said degenerative feedback to said secondary bus, including

(1) a collector load resistance connected between said primary bus and the collector of the output transistor of the last stage of said consecutive stages, and

(2) a degenerative feedback resistance having one end connected to the collector of the output transistor of the last stage and the other end connected to the base of said output transistor of the last stage and to said secondary bus,

wherein the said collector load resistance and feedback resistance, and the circuits associated with said consecutive stages are so designed or selected, that

(A) when there is applied via said primary bus the aforesaid d.c. collector operating current in the FM-mode at a first value lying in a first range of current values, the primary

bus is at a first d.c. potential, lying in a first range of potential values, with respect to earth, and the I.F. amplifier exhibits a first value of overall I.F. amplifier a.c. gain, and

(B) when there is applied via said primary bus the aforesaid d.c. collector operating current in the AM-mode at a second and different value lying in a second range of current values, the primary bus is at a second and different d.c. potential, lying in a second range of potential values, with respect to earth, and the I.F. amplifier exhibits a second and different values of overall I.F. amplifier a.c. gain lying in a range of gain values,

(C) the second value of gain being variable in accordance with the d.c. potential on said secondary bus, as derived from said potential of second value on said primary bus and as transmitted via said secondary bus to said output transistors.

2. An IF amplifier as claimed in Claim 1, wherein the I.F. amplifier's transistors and their associated circuitry are further so designed or selected, that when there is applied in the AM-mode via said primary bus d.c. potential in the said second potential range, which d.c. potential contains a dynamic d.c. component corresponding to the amplitude of the A.M. I.F. modulated carrier delivered by said I.F. amplifier, the overall gain of the I.F. amplifier is automatically controlled by such dynamic d.c. component via said secondary bus, so that the a.c. carrier plus modulation output signal delivered by the I.F. amplifier exhibits relatively small changes in amplitude with relatively large amplitude changes of the a.c. carrier plus modulation input signal to the I.F. amplifier.

3. An I.F. amplifier as claimed in Claim 1 or 2, wherein the I.F. amplifier's transistors and their associated circuitry are further so designed or selected to exhibit I.F. gain in FM-operation with greater d.c. collector operating current applied via said primary bus and higher d.c. primary-bus-potential with respect to earth in FM-operation, and lesser I.F. gain in AM-operation with lesser d.c. collector operating current applied via said primary bus and lower d.c. primary-bus-potential with respect to earth in AM-operation.

4. An I.F. amplifier as claimed in any preceding Claim, wherein each said transistor pair comprises a conductor-connection from the primary bus to the collector of the input transistor of the pair, a resistive connection from the primary bus to the collector of the output transistor of the pair, and a d.c. coupling connection from the collector of the output transistor of the pair to the base of the input transistor of the next higher stage.

5. An I.F. amplifier as claimed in Claim 1, 2 or 3, wherein each said transistor pair



Reference is made to our co-pending Application No. 2681/75 (Serial No. 1,503,171) from which this application was divided and which discloses and claims a current source/

5 load combination for use in an AM-FM radio receiver as disclosed herein, and to Application No. 41909/77 (Serial No. 1,503,173) also divided from 2681/75 (Serial No. 1,503,171) and which discloses and

10 claims a current source as disclosed herein.

WHAT WE CLAIM IS:—

1. An intermediate frequency (IF) amplifier for a radio receiver capable of receiving

15 in the AM mode or FM mode, the IF amplifier being d.c. coupled and arranged to amplify signals at frequencies both in a frequency range centered about the higher FM IF, and centered about the lower AM

20 IF, the amplifier comprising:

(a) a plurality of consecutive stages, said consecutive stages considered collectively, having wide band a.c. gain embracing both

25 said ranges, each such consecutive stage including an emitter coupled transistor pair comprising an input transistor and an output transistor, there being provided for each such pair an emitter-resistor arranged to pass the emitter currents of both transistors of its respective pair, those ends of said

30 emitter-resistors which are remote from the respective emitters being connected together and to an earth-line or earth-point,

(b) a primary bus through which is to be

35 applied d.c. collector operating current to the individual transistors of said consecutive stages,

(c) a secondary bus for passing d.c. base current to the output transistor of each

40 said pair and for applying degenerative feedback to provide balanced biasing of each said transistor pair,

(d) means for establishing said secondary bus at a potential which is a function of the

45 potential of said primary bus and for applying said degenerative feedback to said secondary bus, including

(1) a collector load resistance connected between said primary bus and the collector

50 of the output transistor of the last stage of said consecutive stages, and

(2) a degenerative feedback resistance having one end connected to the collector

55 of the output transistor of the last stage and the other end connected to the base of said output transistor of the last stage and to said secondary bus,

wherein the said collector load resistance and feedback resistance, and the circuits

60 associated with said consecutive stages are so designed or selected, that

(A) when there is applied via said primary bus the aforesaid d.c. collector operating

65 current in the FM-mode at a first value lying in a first range of current values, the primary

bus is at a first d.c. potential, lying in a first range of potential values, with respect to earth, and the I.F. amplifier exhibits a first value of overall I.F. amplifier a.c. gain, and

(B) when there is applied via said primary bus the aforesaid d.c. collector operating current in the AM-mode at a second and different value lying in a second range of current values, the primary bus is at a second and different d.c. potential, lying in a second range of potential values, with respect to earth, and the I.F. amplifier exhibits a second and different values of overall I.F. amplifier a.c. gain lying in a range of gain values,

(C) the second value of gain being variable in accordance with the d.c. potential on said secondary bus, as derived from said potential of second value on said primary bus and as transmitted via said secondary bus to said output transistors.

2. An IF amplifier as claimed in Claim 1, wherein the I.F. amplifier's transistors and their associated circuitry are further so designed or selected, that when there is applied in the AM-mode via said primary bus d.c. potential in the said second potential range, which d.c. potential contains a dynamic d.c. component corresponding to the amplitude of the A.M. I.F. modulated carrier delivered by said I.F. amplifier, the overall gain of the I.F. amplifier is automatically controlled by such dynamic d.c. component via said secondary bus, so that the a.c. carrier plus modulation output signal delivered by the I.F. amplifier exhibits relatively small changes in amplitude with relatively large amplitude changes of the a.c. carrier plus modulation input signal to the I.F. amplifier.

3. An I.F. amplifier as claimed in Claim 1 or 2, wherein the I.F. amplifier's transistors and their associated circuitry are further so designed or selected to exhibit I.F. gain in FM-operation with greater d.c. collector operating current applied via said primary bus and higher d.c. primary-bus-potential with respect to earth in FM-operation, and lesser I.F. gain in AM-operation with lesser d.c. collector operating current applied via said primary bus and lower d.c. primary-bus-potential with respect to earth in AM-operation.

4. An I.F. amplifier as claimed in any preceding Claim, wherein each said transistor pair comprises a conductor-connection from the primary bus to the collector of the input transistor of the pair, a resistive connection from the primary bus to the collector of the output transistor of the pair, and a d.c. coupling connection from the collector of the output transistor of the pair to the base of the input transistor of the next higher stage.

5. An I.F. amplifier as claimed in Claim 1, 2 or 3, wherein each said transistor pair

comprises a conductor-connection from the primary bus to the collector of the input transistor of the pair, a collector load resistor connected between the primary bus and the collector of the output transistor of the pair, a conductor-connection which interconnects the emitters of the transistors of the pair and also the non-earthed end of the respective said emitter-resistor, and a conductor-connection from the collector of the output transistor of the pair to the base of the input transistor of the next-higher stage.

6. An I.F. amplifier as claimed in Claim 5, wherein the bases of said output transistors are conductor-connected to said secondary bus.

7. An I.F. amplifier as claimed in Claim 6, comprising an additional I.F. amplifier stage itself comprised of an emitter-coupled transistor pair, with emitters connected together and via a d.c. passing connection to earth, the base of the input transistor of the additional pair being conductor-connected to the collector of the preceding output transistor of the highest order stage of the aforesaid consecutive stages, the base of the output transistor of the additional pair being conductor-connected to the secondary bus.

8. An I.F. amplifier as claimed in Claim 7, wherein the together-connected emitters of the additional stage are connected to earth via a resistor.

9. An I.F. amplifier as claimed in Claim 8, wherein the together-connected emitters of the additional stage are connected to earth via a current source.

10. An I.F. amplifier as claimed in any one of Claims 1 to 9, wherein integrated

together are the transistors, resistors and current source, as recited in the respective ones of Claims 1 to 9.

11. An I.F. amplifier as claimed in any one of Claims 1 to 10, further comprising a by-pass capacitor connected from the secondary bus to earth.

12. An I.F. amplifier as claimed in any one of Claims 1 to 11 comprising an FM-IF input circuit and an AM-IF input circuit, each latter input circuit comprising a respective inductance in which respectively FM-IF input signal, and AM-IF input signal to the I.F. amplifier, is produced in FM operational use or AM operational use respectively, said inductances being connected d.c. wise in series, and such series combination being connected from the secondary bus to the base of the input transistor of the lowest order stage, whereby to provide a d.c. base-current path for the latter input transistor also from the secondary bus.

13. An I.F. amplifier as claimed in Claim 7, wherein the collector of the input transistor of the additional stage is connected to the fixed d.c. potential point via a conductor-connection.

14. An I.F. amplifier as claimed in Claim 1 and substantially as described with reference to Figure 1 or Figures 2a and 2b of the accompanying drawings.

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