



FLOATING GATE FIELD ISOLATION DEVICE
AND METHOD OF MAKING SAID DEVICE

ABSTRACT

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An isolation structure providing electrical isolation in two dimensions between memory cells in semiconductor memory devices. The isolation structure comprises a trench formed in a substrate of a semiconductor memory device such as a Dynamic Random Access Memory (DRAM). The trench is lined with an insulating material and filled with polysilicon to form a floating gate. An electrical charge is then injected into the polysilicon floating gate. The isolation structure is located between memory cells in an array to provide isolation between cells in sub-micron spacing by combining the characteristics of trench and field isolation. The electrical charge is injected into the polysilicon floating gate by applying a charging voltage to the wordlines of the memory cell array. The charging voltage is applied periodically as necessary to maintain effective isolation. Two dimensional isolation is achieved by extending the trench to surround each pair of memory cells sharing a common bitline contact.

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