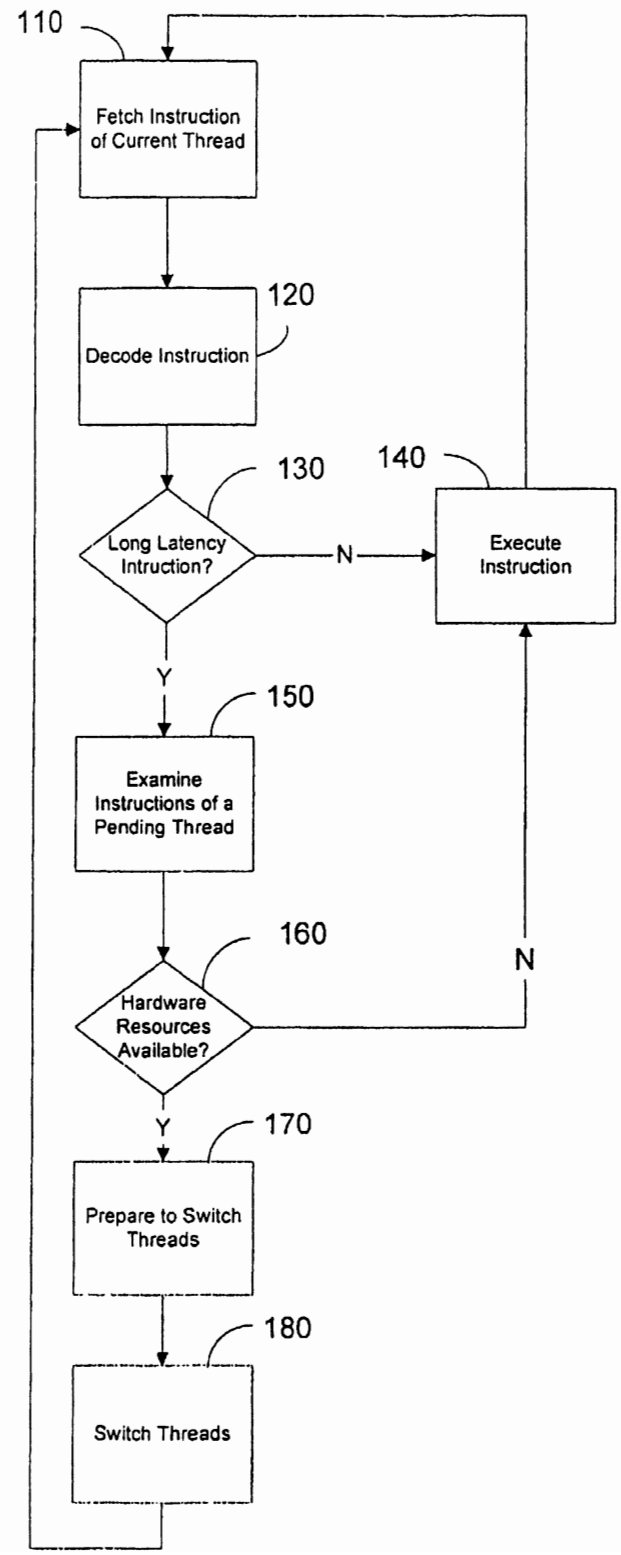
FIG. 1


100
110
Fetch Instruction of Current Thread
120
Decode Instruction
130
Long Latency Intruction?
N
140
Execute Instruction
Y
150
Examine Instructions of a Pending Thread
160
Hardware Resources Available?
N
Y
170
Prepare to Switch Threads
180
Switch Threads

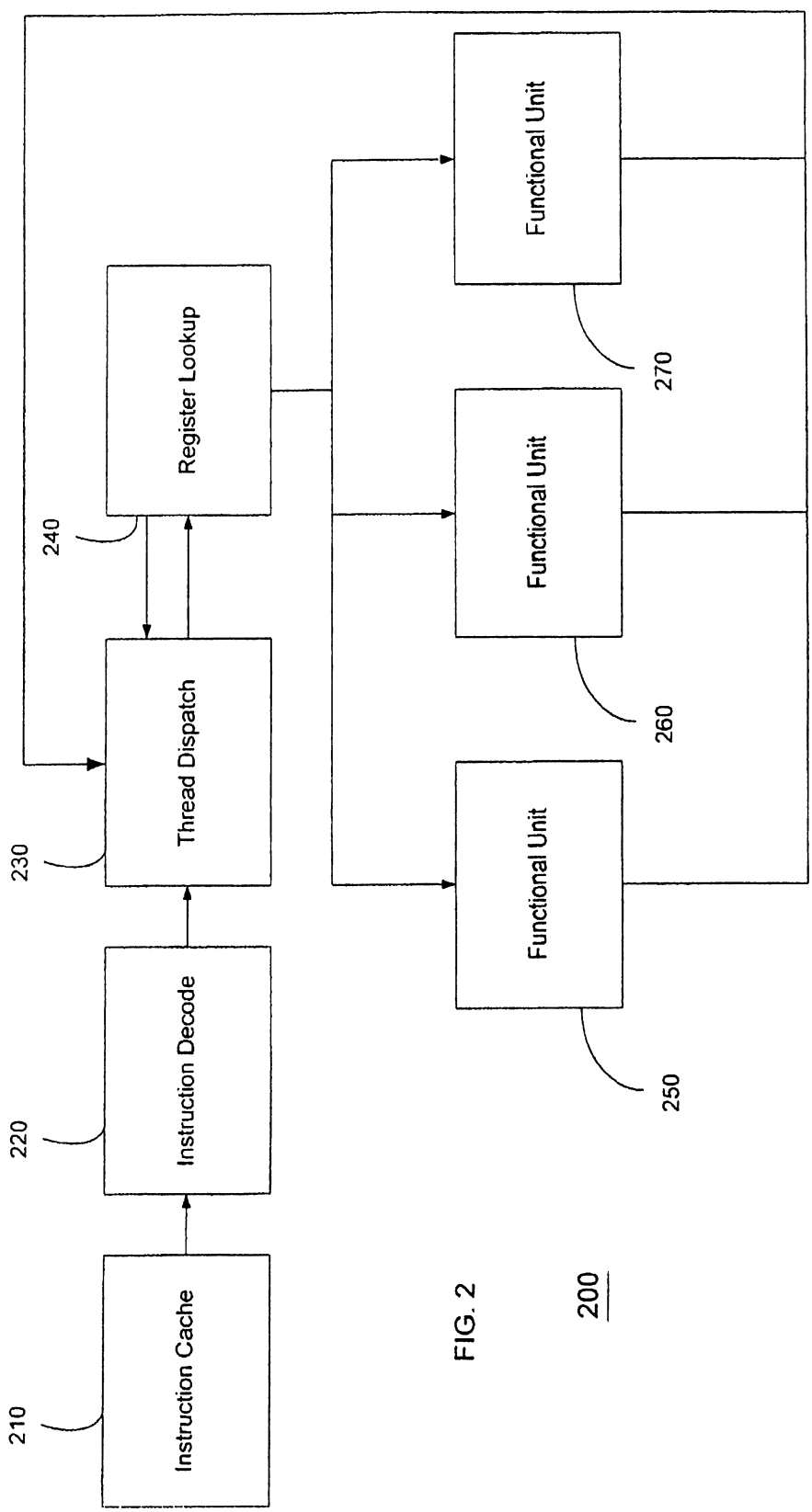

Instruction Cache
210
Instruction Decode
220
Thread Dispatch
230
Register Lookup
240
Functional Unit
250
Functional Unit
260
Functional Unit
270

FIG. 2

200

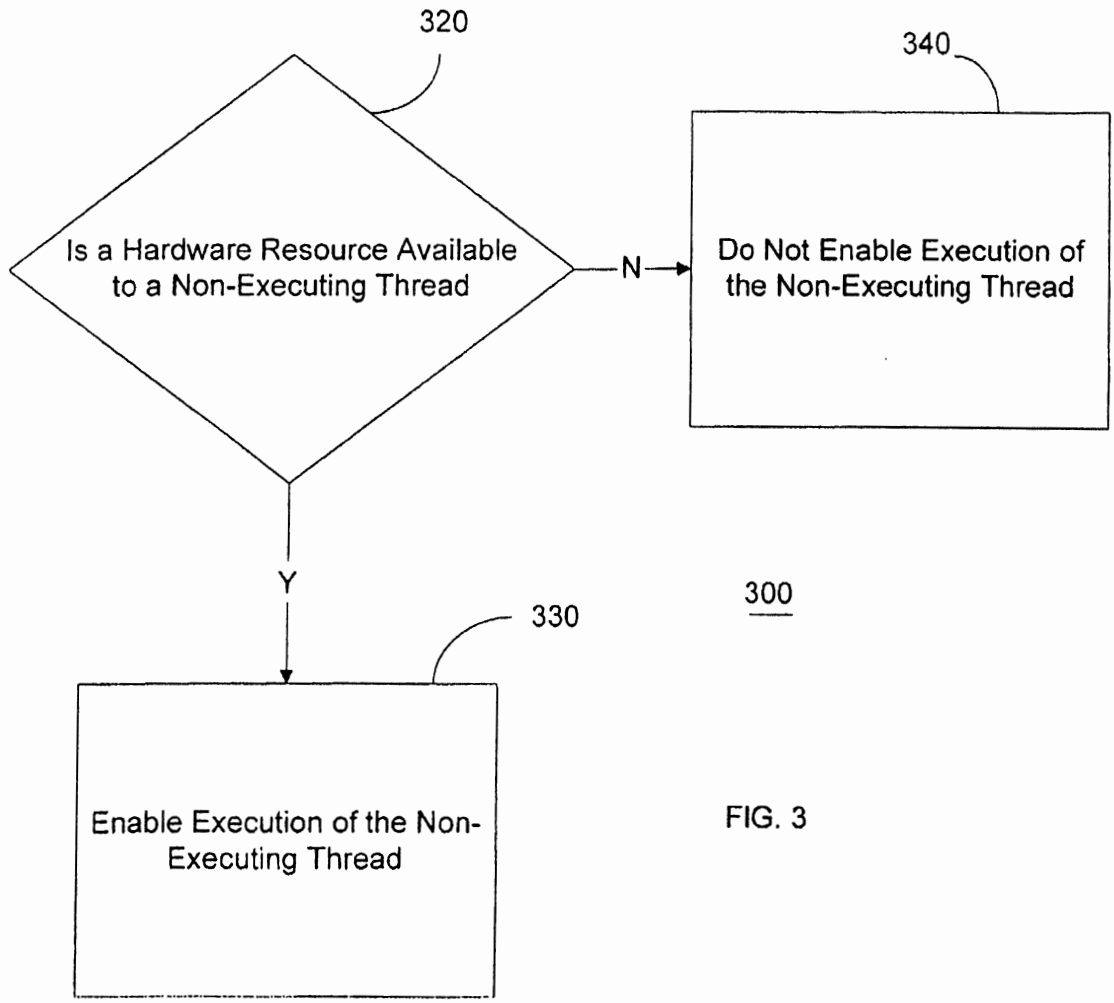

320
340
Is a Hardware Resource Available to a Non-Executing Thread
N
Do Not Enable Execution of the Non-Executing Thread
Y
330
Enable Execution of the Non-Executing Thread
300

FIG. 3

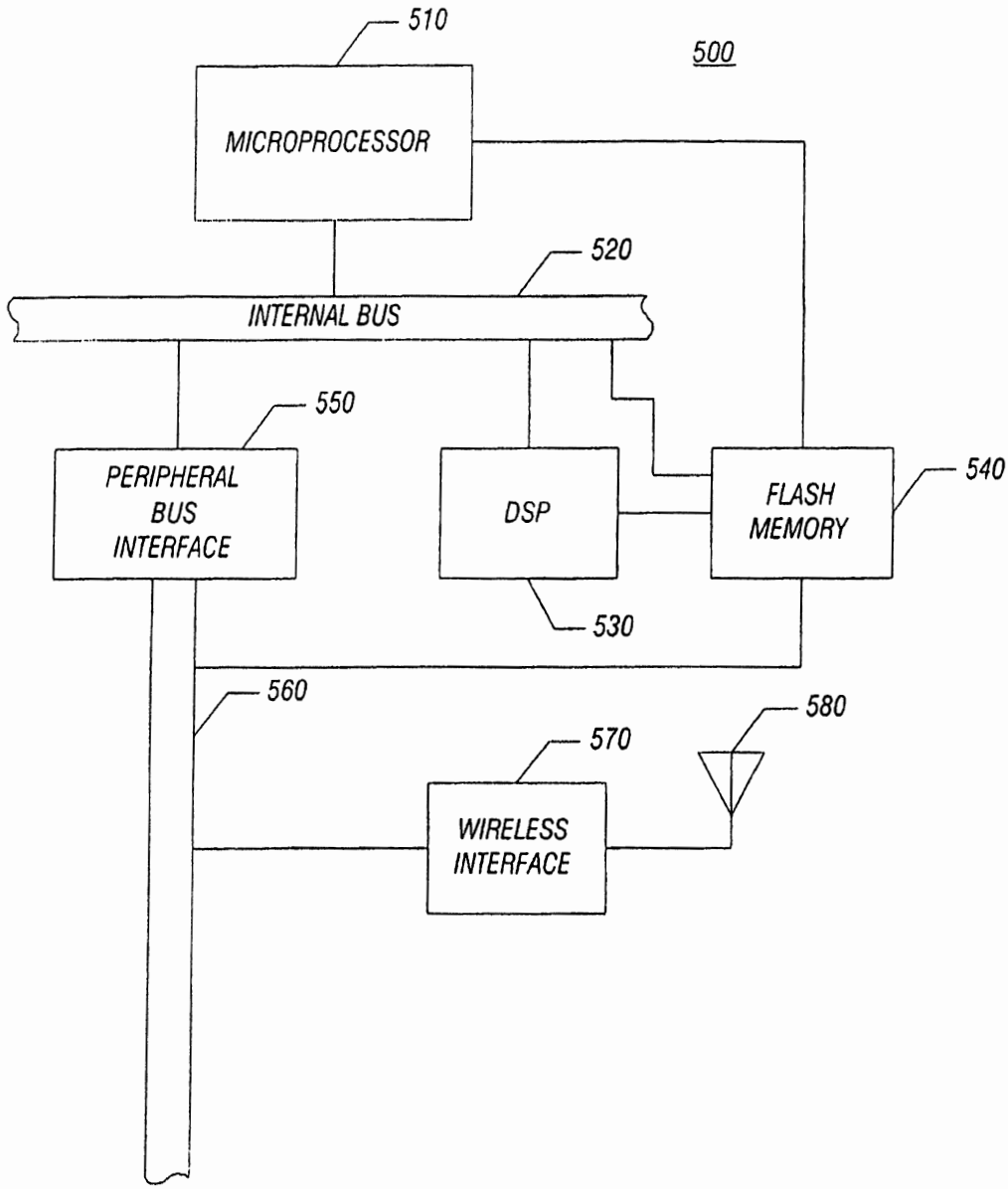

510
500
MICROPROCESSOR
520
INTERNAL BUS
550
PERIPHERAL BUS INTERFACE
DSP
FLASH MEMORY
540
530
560
580
570
WIRELESS INTERFACE

FIG. 4