PROCESSING WITH REDUCED LINE END SHORTENING RATIO

FIELD OF THE INVENTION

[0001] The present invention relates generally to semiconductor processing, and more particularly to a method for forming device features with reduced line end shortening (LES).

BACKGROUND OF THE INVENTION

[0002] To achieve feature sizes that are smaller than the lithographic ground rule, a process known as resist trimming is used. For example, to achieve transistor gate length smaller than ground rule, the patterned resist mask can be trimmed to reduce the critical dimension (CD) of the polysilion line to the target dimension. However, conventional resist trimming processes cause the polysilicon line end to pull back much more than do its sides.

[0003] The distance by which the photoresist line ends is shortened as compared to the reduction in line width is referred to as the line end shortening (LES) ratio. The LES ratio is typically >1.5 to 2. However, such a high LES ratio is not tolerable for some devices, such as SRAM ICs, particularly in light of shrinking device dimensions coupled with increased density. As shown in Figs. 1-2, high LES ratio can result in transistor leakage. Fig. 1 shows a portion of a substrate of an IC 100. Line end pull back can result in the ends of polysilicon gates 210, 212 of adjacent transistors 220, 222 (as shown in Fig. 2) to fall on an active region 240 of the substrate at location A, instead of on the field region 260. This results in current leakage, as represented by the dotted line in Fig. 1, between the transistors.

[0004] To reduce LES, the use of a silicon nitride or silicon oxynitride hard mask to pattern polysilicon gates has been proposed. Hard mask processes, however, besides contributing to higher costs and lower product yields, may be incompatible with some processes. For example, removal of the hard mask after etching is completed may cause erosion of a silicon nitride liner used in shallow trench isolations (STIs) due to lack of etch selectivity, forming divots at the edges of the STIs. This can lead to device leakage, impacting performance and reliability.

Additionally, the use of hard masks increases cost as well as making defect control more difficult.

SUMMARY OF THE INVENTION

[0005] The present invention relates to a process for forming device features with reduced line end shortening (LES). In accordance with one aspect of the invention, a method for reducing LES includes providing a substrate prepared with a device layer or layers of a gate conductor formed thereon with a patterned resist layer disposed above the device layer or layers of the gate conductor. The method further comprises partially trimming the resist layer to produce resist dimensions less than desired dimensions and patterning the device layer or layers of the gate conductor using the partially trimmed resist layer as a mask. The step of patterning the device layer or layers of the gate conductor trims the device layer or the layers to produce a patterned device layer or a patterned gate conductor with reduced LES ratio.

[0006] In yet another aspect of the invention, a semiconductor device with reduced LES ratio is disclosed. The semiconductor device comprises a substrate and a gate conductor disposed on the substrate. The gate conductor includes first and second sides forming a width W and first and second ends forming a length L, wherein the gate conductor comprises a LES ratio of less than 1.5.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figs. 1-2 show gate polysilicon line end pull back (LES) after gate patterning;

[0008] Fig. 3 shows a process for reducing LES in accordance with one embodiment of the invention; and

[0009] Figs. 4a-b, respectively, show SEM images of gate conductors patterned in accordance with one embodiment of the invention and by conventional processes using a hard mask.

DETAILED DESCRIPTION OF THE INVENTION

[0010] The present invention relates to semiconductor processing. More particularly, the present invention provides a process for forming patterned line features with reduced line end shortening. In one embodiment, the line feature comprises polysilicon lines which serve, for example, as gate conductors. Forming other types of line features is also contemplated and within the scope of the invention, particularly where low LES ratio is desirable.

[0011] In accordance with one embodiment of the invention, forming a line feature with sub-ground rule dimensions can be achieved as part of the etch that forms the line feature. The etch can include an initial etch with appropriate etch chemistry which substantially produces the feature based on a patterned resist mask and an over-etch to complete the patterning of the feature, wherein the initial etch uses an appropriate etch chemistry to trim the line feature to desired dimensions. By trimming the line feature as part of the etch that forms the line feature, LES is substantially reduced.

[0012] Fig. 3 shows a process for reducing LES in accordance with one embodiment of the invention. The process includes providing a substrate having a patterned resist layer thereon. Typically a BARC layer is provided beneath the resist layer to improve the lithographic process. The patterned resist layer is used to form a sub-ground rule line feature. The difference between the ground rule and the desired CD of the line feature is referred to as the gap dimension (GD).

[0013] In one embodiment, the patterned resist layer is partially trimmed at step 310. The partial resist trim reduces the CD to sub-ground rule dimensions, but insufficiently to satisfy the desired CD of the line feature. The partial trim should result in LES ratio of less than 1.5, preferably less than 1.4, more preferably less than 1.3 and even more preferably, from about 1.1-1.2. The partial trim, for example, trims up to about 40% of the GD, preferably about 10-40% of the GD and more preferably about 20-30% of the GD. In one embodiment, the partial trim trims less than about 10 nm of the resist. The amount of resist trimming can be adjusted to

accommodate different processes, so as to facilitate achieving the desired CD with low LES ratio. The partial resist trim can be performed using conventional O_2-based chemistry.

[0014] At step 320, exposed portions of the BARC layer unprotected by the resist layer are removed to expose portions of the layer beneath the BARC layer. The layer beneath the mask, in some applications, can include more than one layer. The layer stack at step 330 is patterned based on the resist mask to form a line feature. In accordance with one embodiment of the invention, the etch forms a line feature with the desired sub-ground rule CD. Unlike in resist trim processes, resist "foots" are not removed during the etch, thus reducing LES ratio. The etch comprises, in one embodiment, plasma etching. The etch employs appropriate chemistry for etching in the vertical direction with some etching in the horizontal direction. The desired ratio of vertical to horizontal etching (VE:HE) will depend on the height of the feature and the value of GD. The etch chemistry can be tailored to achieve the desired VE:HE ratio.

[0015] In one embodiment, the layer stack comprises layers for forming gate conductors. The gate conductor, for example, comprises a polysilicon layer over a gate dielectric layer. The gate dielectric layer comprises, for example, an oxide layer. Other types of line features are also useful. It is understood that the gate conductor need not be straight. The gate conductor can be S-shaped, L-shaped or other shapes. In one embodiment, a non-chlorine-based chemistry is used to etch the polysilicon layer. Using a non-chlorine based chemistry can reduce isotropic etching of the polysilicon sidewalls, minimizing profile bowing.

[0016] In one embodiment, the etch chemistry used to etch the polysilicon layer comprises first and second fluorine-based chemistries. The first chemistry comprises a high fluorine content while the second chemistry comprises a low fluorine/carbon ratio or high carbon content. The first chemistry etches the polysilicon layer while the second chemistry serves to passivate the polysilicon sidewalls to prevent bowing, maintaining the profile of the gate conductor. The first chemistry can comprise SF_6, C_2F_6 or CF_4 and the second chemistry can comprise CH_2F_2 or

C_4F_8. Preferably, the first and second chemistries respectively comprise SF_6 and CH_2F_2. Alternatively, the first and second chemistries respectively comprise SF_6 and C_4F_8. The molar ratio of the first and second chemistries is about 1:1 to 1:3. Other types of fluorine-based or non-fluorine based chemistries may also be useful. The etch can be performed with low bias power and relatively high source power. Under these conditions, a high density, low bombardment energy plasma is formed such that a high etch rate can be achieved while minimizing the degree of plasma damage to the gate dielectric layer.

[0017] In one embodiment, the etch to form the line feature with the desired sub-ground rule CD stops with a soft landing at step 340. The soft landing step, for example, is highly selective to the gate dielectric material to reduce or eliminate pitting of the gate dielectric layer. After the soft landing step, an over-etch is performed at step 350. The over-etch, for example, has an even higher selectivity to the gate dielectric material to prevent damage to the gate dielectric layer.

[0018] Fig. 4a shows a SEM image of gate conductors patterned in accordance with one embodiment of the invention, and Fig. 4b shows a SEM image of gate conductors patterned with a hard mask according to conventional processes. As shown in Fig. 4a, a LES ratio of about 1.2 can be achieved, with a polysilicon trim of about 30 nm. In contrast, as shown in Fig. 4b, conventional processes can only achieve a LES ratio of 2.4 with a smaller trim of 20 nm. As such, polysilicon line end pull back is significantly reduced using the present process. Additionally, with the present process, high functional yield, comparable to hard mask processes, was demonstrated for the fabrication of high density SRAM ICs.

[0019] As described, LES can be reduced by trimming the layer stack to achieve the desired CD during the etch to form the line feature. Furthermore, CD through pitch performance is improved because any microloading effect is counteracted by a greater reduction in line CD in isolated regions. Additionally, the present process is compatible with current STI /silicon nitride (SiN) liner schemes. It is thus readily integrated into existing processes with minimal expense in

terms of both resources and developmental time. Finally, as compared with conventional hard mask processes, lower long-term production costs can be achieved.

[0020] The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments, therefore, are to be considered in all respects illustrative rather than limiting the invention described herein. Scope of the invention is thus indicated by the appended claims, rather than by the foregoing description, and all changes that come within the meaning and range of equivalency of the claims are intended to be embraced therein.

What is claimed is:

Claims

1. A method for reducing line end shortening (LES) comprising:

providing a substrate prepared with a device layer formed thereon with a patterned resist layer disposed above the device layer;

partially trimming the resist layer to produce resist dimensions less than desired dimensions; and

patterning the device layer using the partially trimmed resist layer as a mask, wherein patterning the device layer trims the device layer to produce a patterned device layer with reduced LES ratio.

2. The method of claim 1 wherein the device layer comprises an oxide layer and a polysilicon layer over the oxide layer.

3. The method of claim 1 wherein the patterned device layer comprises gate conductors.

4. The method of claim 1 wherein partially trimming the resist layer up to about 40% of a gap dimension.

5. The method of claim 1 wherein partially trimming the resist layer up to about 10-40% of a gap dimension.

6. The method of claim 1 wherein partially trimming the resist layer up to about 20-30% of a gap dimension.

7. The method of claim 1 wherein the patterned device layer comprises a LES ratio of less than 1.5.

8. The method of claim 1 wherein the patterned device layer comprises a LES ratio of less than 1.4.

9. The method of claim 1 wherein the patterned device layer comprises a LES ratio of less than 1.3.

10. The method of claim 1 wherein the patterned device layer comprises a LES ratio of about 1.1 to 1.2.

11. The method of claim 1 wherein patterning the device layer comprises a patterning chemistry which includes first and second patterning chemistries, the first chemistry comprises a high fluorine content and the second chemistry comprises a low fluorine/carbon ratio.

12 The method of claim 11 wherein the first patterning chemistry is selected from the group consisting of SF_6, C_2F_6 and CF_4, and the second patterning chemistry is selected from the group consisting of CH_2F_2 and C_4F_8.

13. The method of claim 11 wherein the first patterning chemistry comprises SF_6 and the second patterning chemistry comprises CH_2F_2.

14. The method of claim 11 wherein the first patterning chemistry comprises SF_6 and the second patterning chemistry comprises C_4F_8.

15. A method of fabricating a semiconductor device comprising:

providing a semiconductor substrate prepared with layers of a gate conductor over the substrate;

forming and patterning a resist layer to contain a pattern of the gate conductor;

partially trimming the resist layer to produce resist dimensions less than desired dimensions; and

patterning the layers of the gate conductor using the partially trimmed resist layer as a mask, wherein patterning the layers trims the layers to produce a patterned gate conductor with a reduced line end shortening (LES) ratio.

16. The method of claim 15 wherein the LES ratio is less than 1.5.

17. A semiconductor device comprising:

a substrate; and

a gate conductor disposed on the substrate, the gate conductor includes first and second sides forming a width W and first and second ends forming a length L, wherein the gate conductor comprises a line end shortening (LES) ratio of less than 1.5.

18. The device of claim 1 wherein the gate conductor comprises a LES ratio of less than 1.4.

19. The device of claim 1 wherein the gate conductor comprises a LES ratio of less than 1.3.

20. The device of claim 1 wherein the gate conductor comprises a LES ratio of about 1.1 to 1.2.