CLAIMS

1. A method for forming a semiconductor device, the method comprising:

forming a bottom isolation structure over a substrate;

forming a nanosheet stack on the bottom isolation structure, wherein the bottom isolation structure is located between the nanosheet stack and the substrate;

forming a sacrificial region on top of the nanosheet stack, wherein the sacrificial region is in direct contact with the bottom isolation structure;

forming a dielectric pillar adjacent to the nanosheet stack, wherein the dielectric pillar is positioned directly on top of a shallow trench isolation region of the substrate, and wherein the dielectric pillar is in direct contact with the sidewall of the sacrificial region;

removing the sacrificial region to expose a surface of the bottom isolation structure and a surface of the shallow trench isolation region;

forming a source or drain (S/D) region directly on top of the exposed surface of the shallow trench isolation region;

forming a conformal liner over the S/D region and the dielectric pillar;

forming an interlayer dielectric over the conformal liner;

removing a portion of the interlayer dielectric and a portion of the conformal liner to form a contact trench exposing a surface of the S/D region and a surface of the dielectric pillar; and

forming a trench silicide in the contact trench.

2. The method of claim 1, wherein the dielectric pillar serves as an etch stop while forming the contact trench.

3. A semiconductor device comprising:

a nanosheet stack positioned over a substrate;

a dielectric pillar adjacent to the nanosheet stack, the dielectric pillar positioned on a shallow trench isolation region of the substrate and is in direct contact therewith;

a source or drain (S/D) region, wherein the S/D region is located on a surface of the shallow trench isolation region and is in direct contact therewith such that a bottom surface of the S/D region and a bottom surface of the dielectric pillar are coplanar; and

a trench silicide, wherein the trench silicide is located on a surface of the S/D region and is in direct contact therewith, and wherein the trench silicide is located on a top surface of the dielectric pillar and is in direct contact therewith.

4. The semiconductor device of claim 3, wherein the S/D region is confined between opposite sidewalls of the dielectric pillar.

5. The semiconductor device of claim 3 further comprising a bottom isolation structure between the substrate

and the nanosheet stack.

6. The semiconductor device of claim 3 further comprising a conformal liner over the dielectric pillar.

7. The semiconductor device of claim 6 further comprising an interlayer dielectric over the conformal liner, wherein the trench silicide is positioned between opposite sidewalls of the interlayer dielectric.