

Semiconductor Wafer

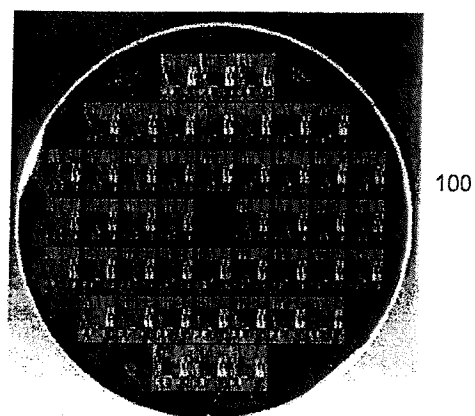


FIG. 1

Individual Device on Wafer

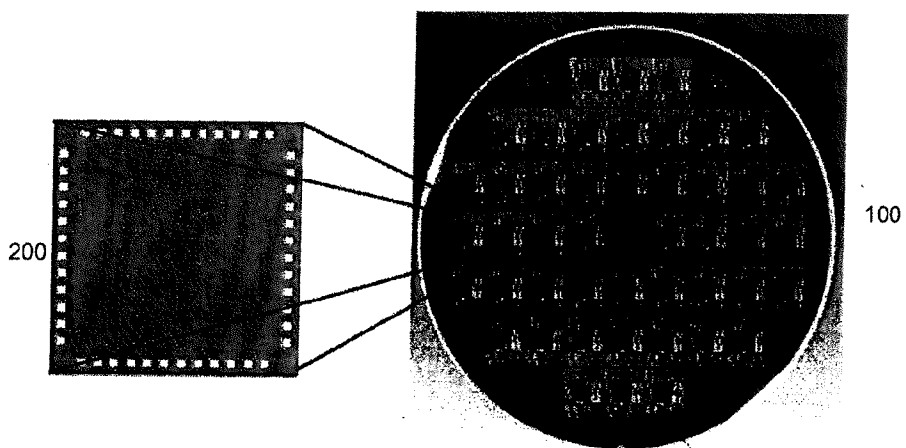
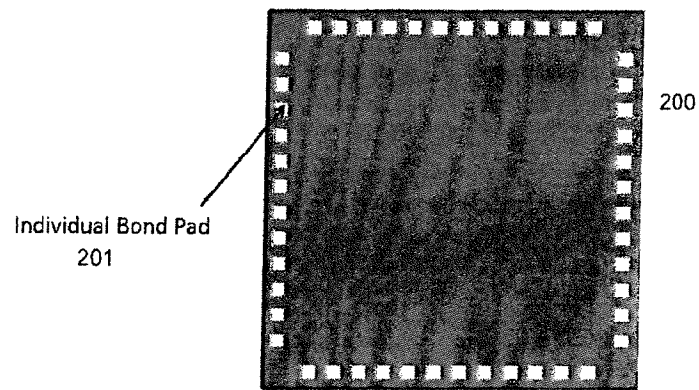
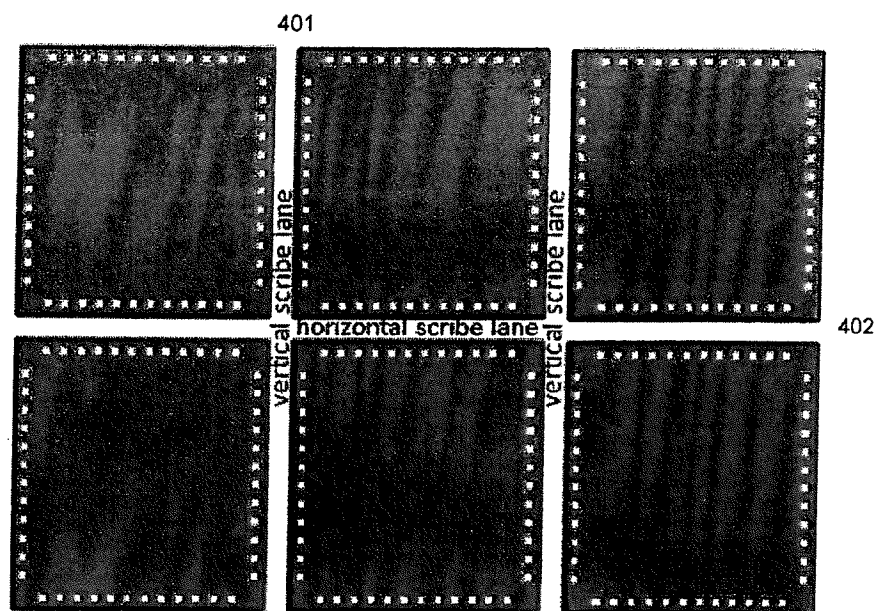


FIG. 2

Bond Pads on Device

**FIG. 3****FIG. 4**

Bond Wires To Package Lead Frame

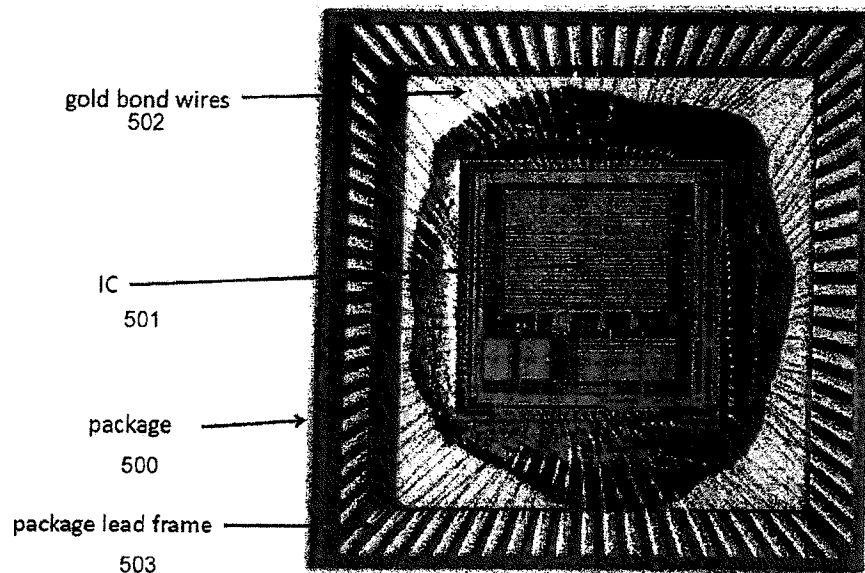


FIG. 5A

Bond Wires To Package Pins

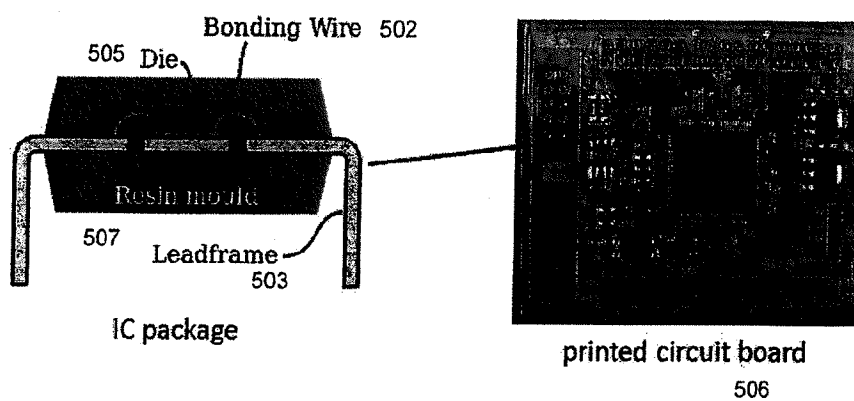
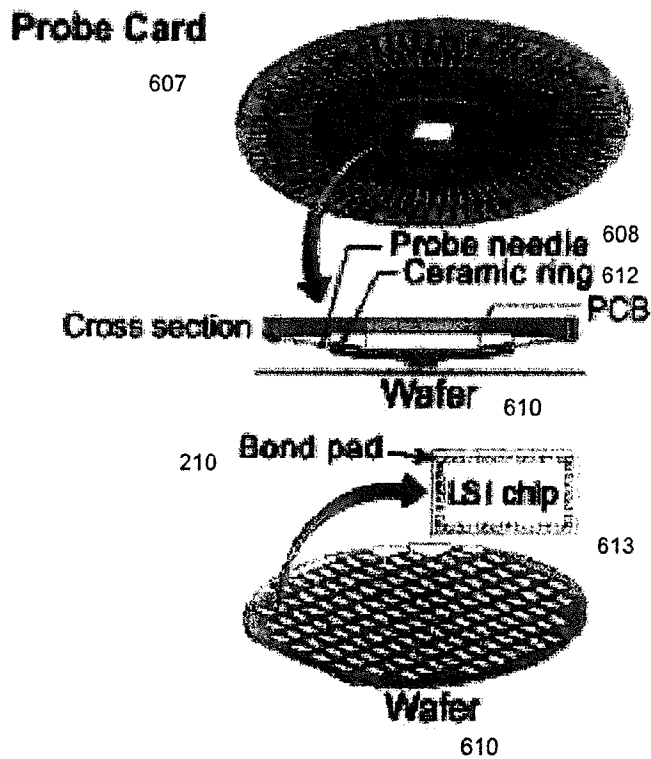
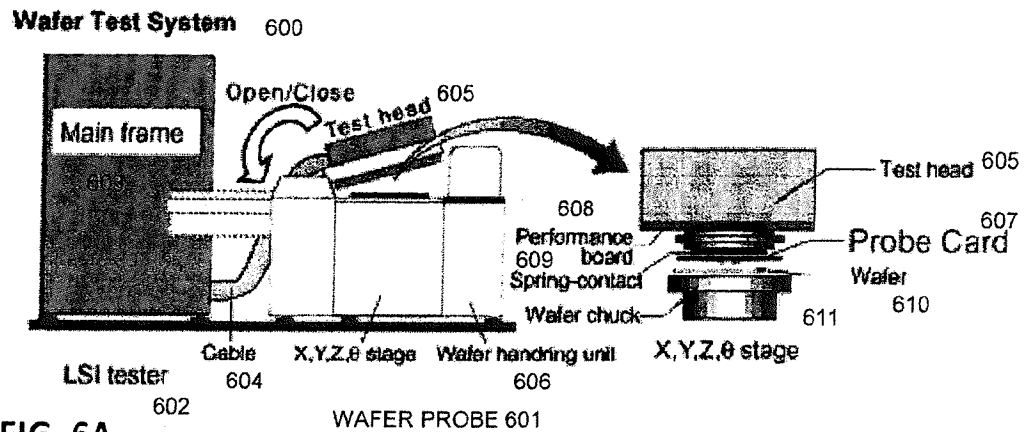


FIG. 5B



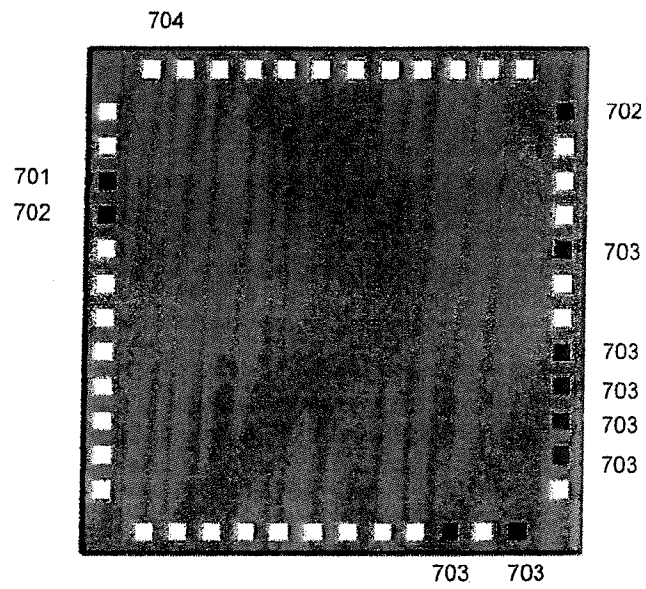


FIG. 7A

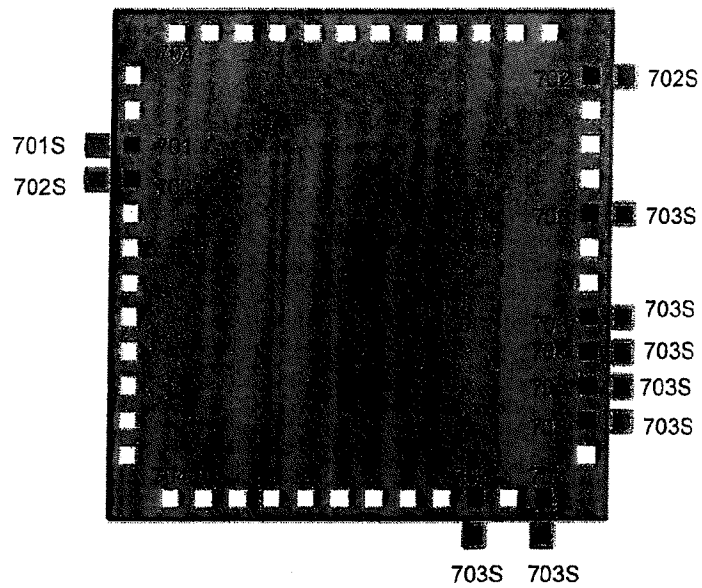
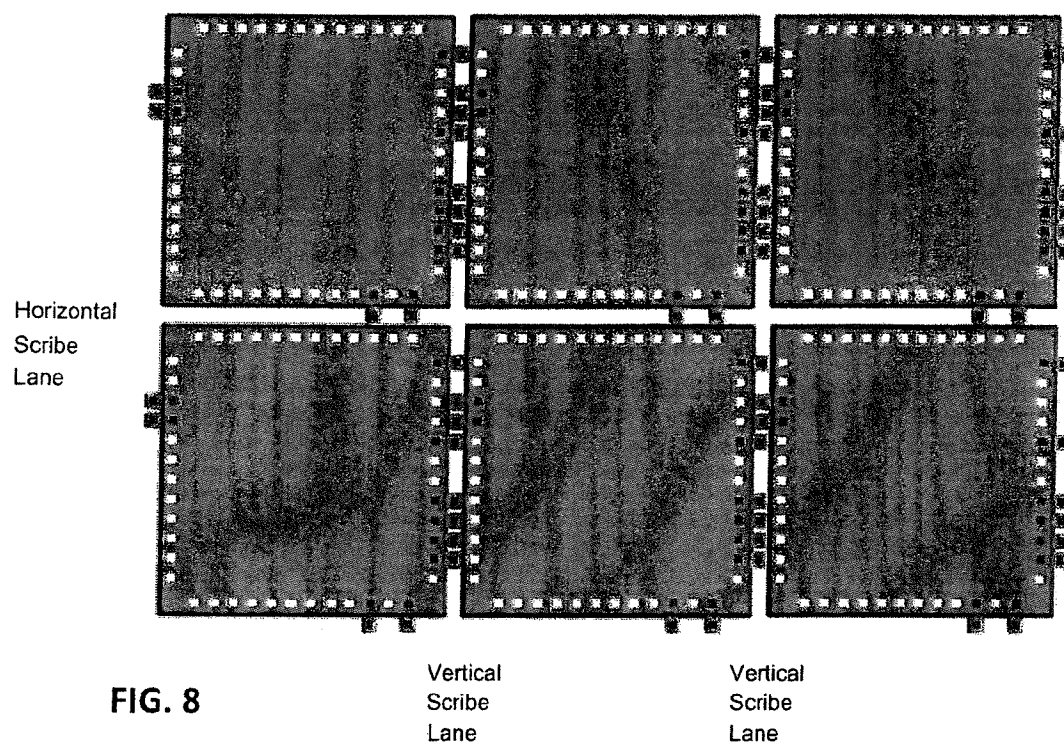
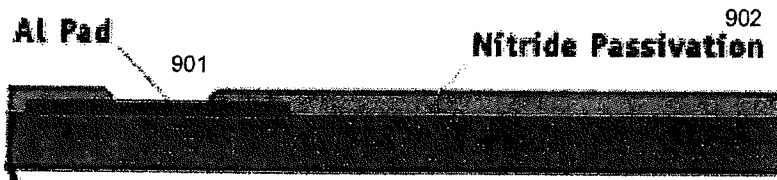


FIG. 7B





FIGs. 9A.

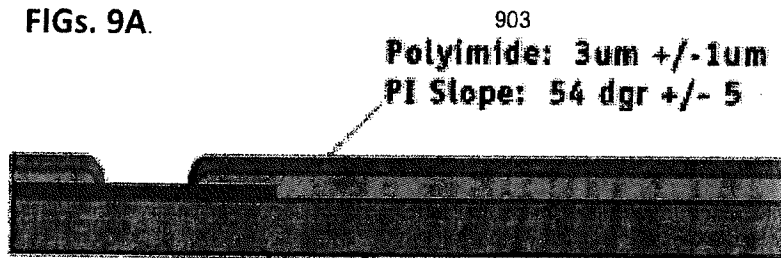


FIG. 9B

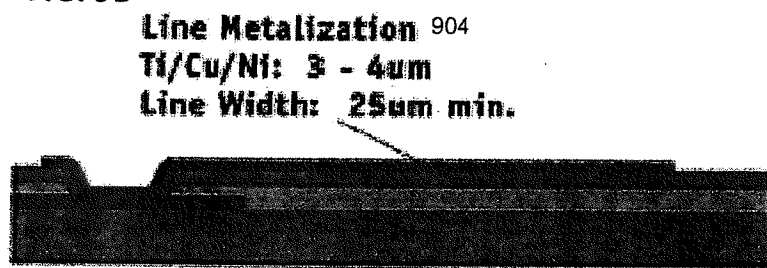


FIG. 9C

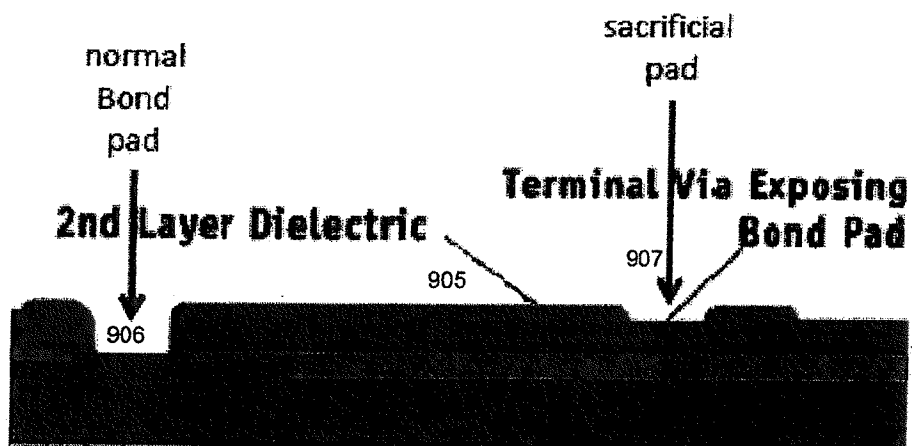


FIG. 9D

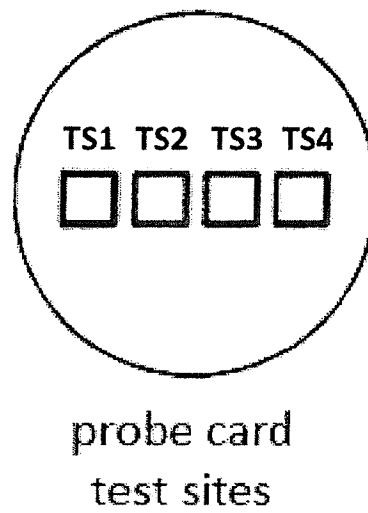


FIG. 10

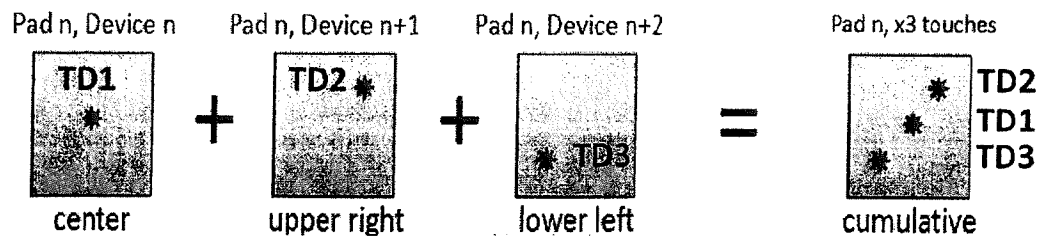
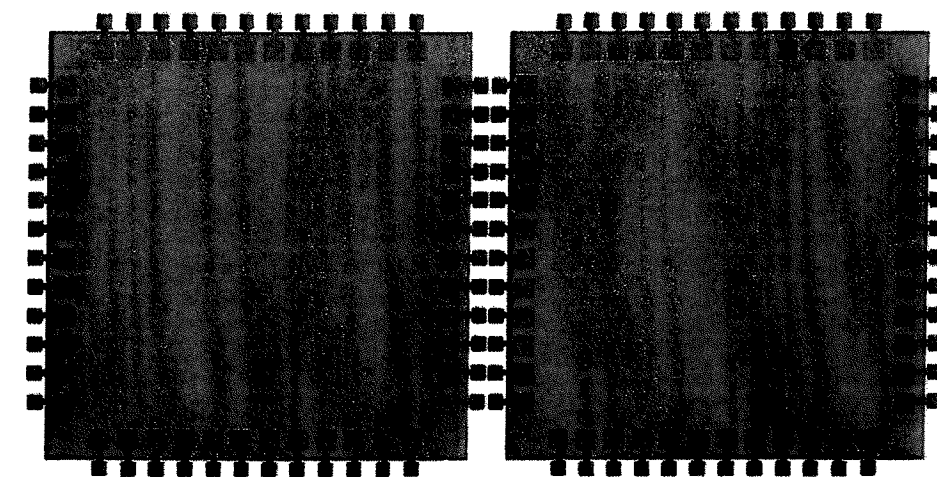
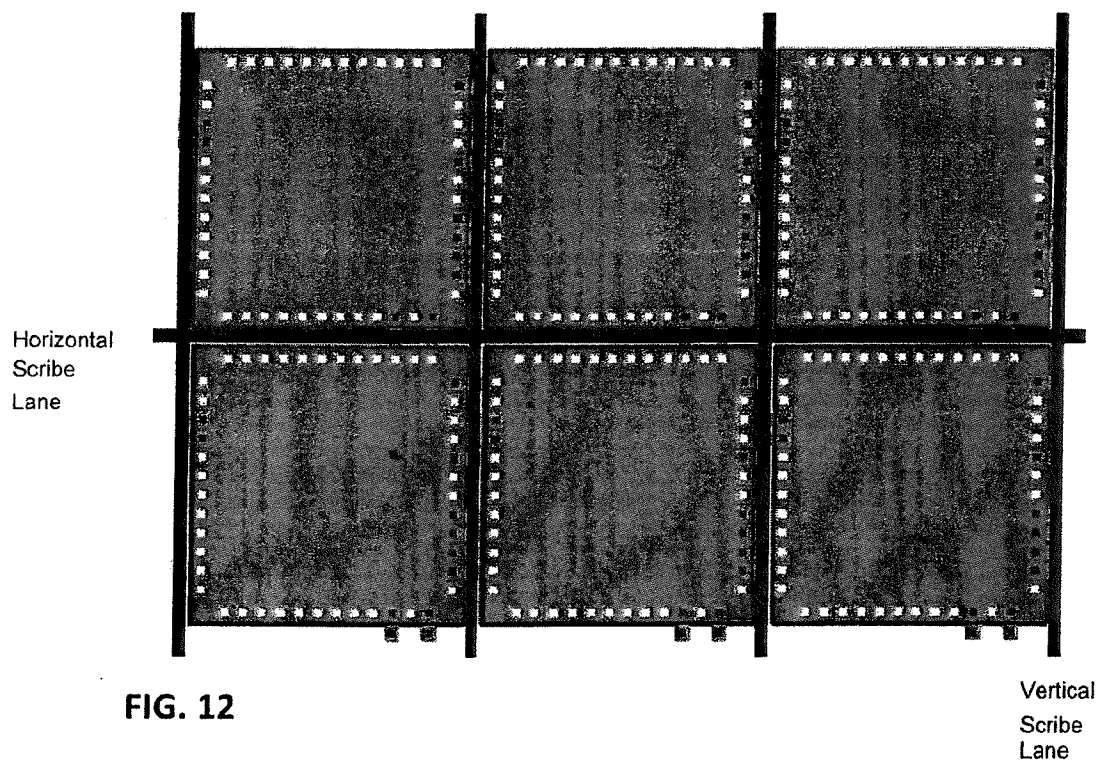


FIG. 11



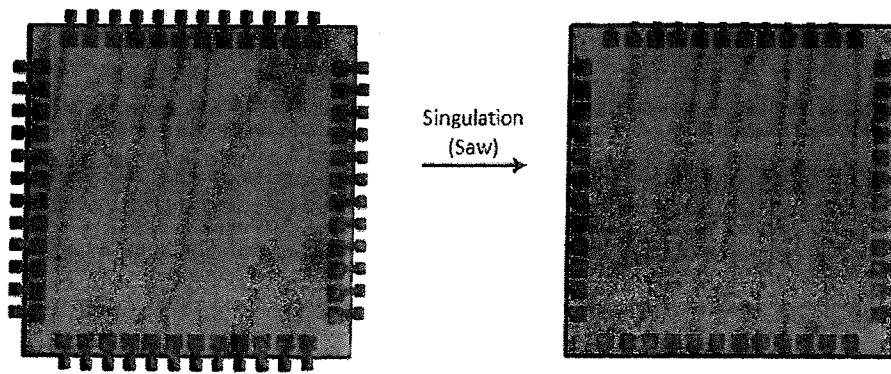


FIG. 14

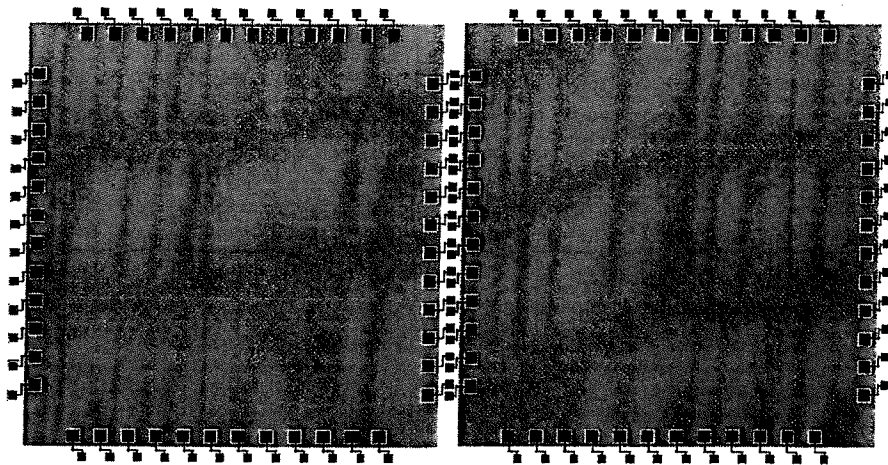


FIG. 15

11/11

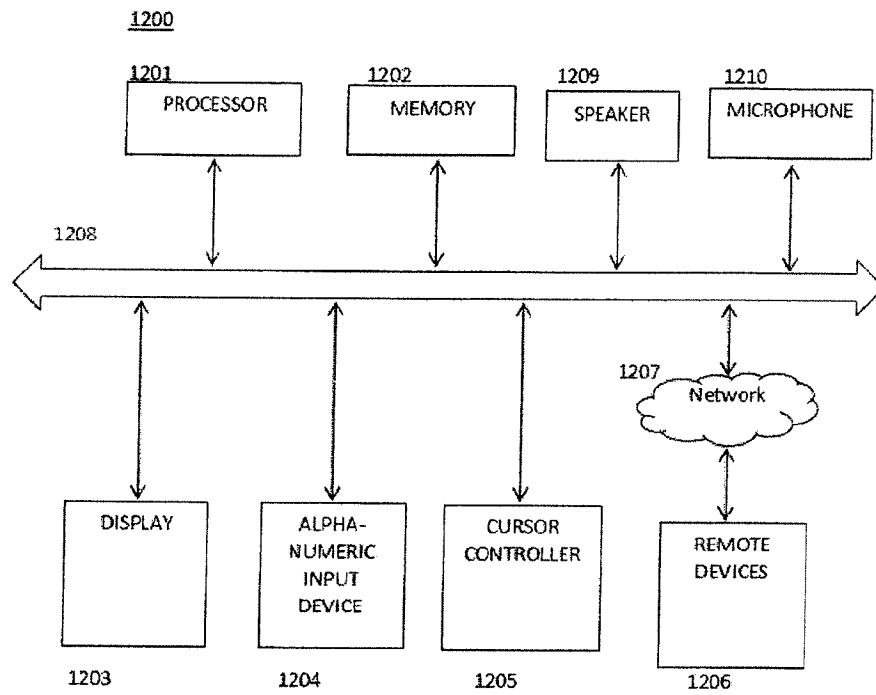


FIG. 16