

"A muting circuit".

The present invention relates to a muting circuit.

A known muting circuit providing a large signal attenuation has been previously disclosed by us in an electronic switching circuit which makes use of a differential transistor circuit such as the one shown in Figure 1 of the accompanying drawings.

In this circuit, the collector electrodes of differential amplification transistors Q_1 and Q_2 for signal transmission are connected in common to respective collector electrodes of differential transistors Q_3 and Q_4 for forming a D.C. signal at the time of muting operation. Constant current Q_5 , Q_6 are connected to

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common emitter electrodes of the respective pairs of differential transistors Q_1 , Q_2 and Q_3 , Q_4 . The constant current transistors Q_5 , Q_6 are selectively and alternately operated by a switch SW_1 .

5 An input signal is applied to the base electrode of the differential transistor Q_1 . A bias voltage V_{B1} is applied to the base electrode of transistor Q_1 via a bias resistor R_B , and also directly to the base electrode of the
10 differential transistor Q_3 . A negative feedback signal is applied to the base electrodes of the transistors Q_2 and Q_4 via a feedback circuit β , in order to set the gain of the differential amplification transistor circuit and also to
15 provide a D.C. bias voltage.

 This circuit operates as follows:
When the switch SW_1 is set to position a, the constant current transistor Q_5 becomes non-conductive whilst the constant current transistor
20 Q_6 becomes conductive so that the differential amplification transistors Q_1 and Q_2 are turned off whilst the differential transistors Q_3 and Q_4 are turned on. Consequently, only the same D.C. signal

as the bias voltage V_{B1} , that is formed by the differential transistors Q_3 and Q_4 , can be obtained from the output OUT.

On the other hand, when the switch SW_1 is set to the position b, the differential amplification transistors Q_1 and Q_2 become conductive and transmit the input signal IN. Accordingly, a large signal attenuation can be obtained without changing the D.C. output signal.

We have found that in this muting circuit when the input signal IN is applied via a coupling capacitor C_1 the following problem occurs.

It is to be assumed that the input terminal IN in Figure 1 is substantially earthed through the practically negligible impedance of a signal source (not shown), so that the bias voltage V_{B1} rises instantly at the time t_1 , immediately after the power is connected as shown in Figure 2 of the accompanying drawings, whereas the voltage V_{B1} , at the junction between the coupling capacitor C_1 and the bias resistor R_B , gradually rises/due to the time constant of the capacitor C_1 and the resistor R_B .

Accordingly, if the switch SW_1 is

set to the position a during a predetermined period from the time t_1 to the time t_2 , the base voltage of both differential amplification transistors Q_3 and Q_4 is equal to the bias voltage V_{B1} and consequently, the collector potential of the transistor Q_4 becomes V_{B1}/β . Since an output coupling capacitor C_o connected to the output terminal OUT and the impedance of a load (not shown) form a differential circuit together, the waveform obtained by differentiating the collector potential V_{B1}/β of the transistor Q_4 occurs at the output terminal OUT at the time t_1 , as shown in the waveform diagram of Figure 2. This transient response waveform occurring at the time t_1 eventually results in a popping noise, but can be prevented by arranging a muting circuit (not shown) at a subsequent stage in this circuit.

When the switch SW_1 is switched from position a to position b at the time t_2 , the base electrode of the transistor Q_2 is biased by the bias voltage V_{B1} whereas the base electrode of the transistor Q_1 is biased by the voltage V_{B1}' which is lower than the bias voltage V_{B1} . Consequently, since a voltage difference ΔV as shown in the

waveform diagram of Figure 2 is applied between the base electrodes of the differential amplification transistors Q_1 and Q_2 , the collector potential of the transistor Q_2 drastically drops at the time t_2 .

5 The waveform obtained by differentiating this collector potential by the output coupling capacitor C_o and the impedance of the load occurs at the output terminal OUT at the time t_2 as shown in the waveform diagram of Figure 2.

10 We have found that prevention of the popping noise at the time t_2 can be accomplished by reducing the time constant at the rise of the voltage V_{B1}' to an extremely small value. Accordingly, we have examined the idea of reducing
15 the capacitance of the coupling capacitor C_1 , but this idea was abandoned because a problem of phase inversion of low frequency signals arises.

Reducing the resistance of the bias resistor R_B was also attempted, but this idea was
20 also abandoned because of the lowering of the input impedance at the input terminal IN.

Occurrence of the popping noise due to the transient response waveform at the time t_2 can be prevented by arranging another muting circuit

(not shown) at a subsequent stage of this circuit, but when the capacitance of the coupling capacitor and the resistance of the bias resistor R_B are set to about $10\mu F$ and about $40Kohms$, respectively, the

5 muting time of the muting circuit arranged at the subsequent stage of this circuit must be set to about three seconds. However, if the muting operation is carried out for such a relatively long period after turning on the power source, the listener might

10 think that the radio receiver was out of order.

On the other hand, as one of the additional functions of an FM radio receiver, a muting circuit for eliminating offensive noise between stations during selection of the stations

15 has previously been known, such as that disclosed in "HI-FI FM TUNER", p. 193-199, published on August 20, 1976 by Nippon Hoso Kyokai.

FM radio receivers employing this muting circuit in a monolithic semiconductor

20 integrated circuit for FM intermediate frequency amplification and detection are commercially available from both RCA and Hitachi Ltd.

Figure 3 of the accompanying drawings shows a block diagram of an FM radio receiver

including the monolithic semiconductor integrated circuit. This radio receiver was examined by us prior to the filing of this patent application.

5 The FM radio receiver shown in Figure 3 includes a monolithic semiconductor integrated circuit IC_1 for FM intermediate frequency amplification and detection. This integrated circuit IC_1 includes an FM intermediate frequency amplification stage 1, an FM detection stage 2, a low frequency amplification
10 stage 3, a detuning detection circuit 4, and a mute control circuit 6 for controlling the muting operation at the low frequency amplification stage 3. Additionally, this monolithic semiconductor integrated circuit includes an AFC circuit and a level detection
15 circuit, the output signals of which are used as the input signals to the detuning detection circuit 4. A time constant circuit 5 is provided for removing high frequency components contained in the detuning detection signal.

20 The FM radio receiver also includes a monolithic semiconductor integrated circuit IC_2 for FM stereo demodulation. This integrated circuit IC_2 includes a pre-amplifier 7, a PLL (phase locked loop) circuit 8 for forming a 38KHz switching signal

synchronous with a 19KHz pilot signal contained in a stereo composite signal, and a stereo demodulation circuit 9. The stereo composite signal formed by the FM detection circuit 2 is applied to the input of the pre-amplifier 7 via a coupling capacitor C_{100} whilst the stereo demodulation circuit 9 forms stereo demodulated signals L, R of the left and right channels by receiving at its input the stereo composite signal passing through the pre-amplifier 7 and the 38KHz switching signal formed by the PLL circuit 8.

The monolithic semiconductor integrated circuit IC_2 also includes additional circuits for stereo-monaural detection, selection and display.

In the monolithic semiconductor integrated circuit IC_1 , the popping noise V_{pop} originates from the FM detection stage 2 due to changes in the D.C. voltage in the S characteristic curve of the FM detection circuit 2 as shown in Figure 4 of the accompanying drawings during the muting operation for changing over from tuning to detuning upon detection of detuning.

Accordingly, we have examined the possibility of providing a muting circuit 10 at the output of the stereo demodulation circuit 9 as the

subsequent stage. In such a case, the muting circuit 10 must exhibit fast mute-release timing for shifting from detuning to tuning and retarded mute timing for shifting from tuning to detuning in its muting operation in the monolithic semiconductor integrated circuit IC₁. Since these muting operations are independently controlled, the timings are difficult to set and are highly susceptible to variance of element characteristics.

Moreover, the coupling capacitor C₁₀₀ which is positioned between the two muting circuits 6 and 10, causes a time advance of the signal to the subsequent muting circuit, so that it becomes extremely difficult for the subsequent muting circuit 10 to eliminate the popping noise generated in the preceding muting circuit 6.

It is therefore an object of the present invention to provide a muting circuit which prevents the occurrence of a popping noise at the time of mute release after turning on the power source.

According to

present invention there is provided a muting circuit including:

- (a) first and second transistors having their emitter electrodes connected to each other;
- 5 (b) third and fourth transistors having their emitter electrodes connected to each other;
- (c) a first constant current source connected to the emitter electrodes of said first and second transistors;
- (d) a second constant current source connected to the
10 emitter electrodes of said third and fourth transistors;
- (e) a coupling capacitor for feeding an input signal to the base electrode of said first transistor;
- (f) a bias resistor having one end thereof connected to the base electrode of said first transistor and the
15 other end connected to the base electrode of said third transistor;
- (g) bias voltage generation means connected to the base electrode of said third transistor and to said other end of said bias resistor;
- 20 (h) load means connected to the collector electrode of said second transistor and to the collector electrode of said fourth transistor;
- (i) a feedback circuit connected between said load means and the base electrodes of said second and

fourth transistors;

- (j) means for alternatively controlling and bringing either one of said first and second constant current sources into the operative state and the other into the inoperative state; and
- 5 (k) a switching element connected between said one end and said other end of said bias resistor and actuated into the ON state for a predetermined period after the switching on of the power source of the
- 10 muting circuit.

The present invention will now be described in greater detail by way of example with reference to the remaining figures of the accompanying

drawings, wherein:-

Figure 5 is a circuit diagram of a preferred form of muting circuit;

Figure 6 is a waveform diagram to explain the operation of the muting circuit shown in Figure 5;

Figure 7 is a detailed circuit diagram of the preferred form of muting circuit;

Figure 8 is a block diagram of an FM radio receiver incorporating a muting circuit;

Figure 9 is a waveform diagram to explain the operation of the FM receiver shown in Figure 8; and

Figure 10 is a detailed circuit diagram showing the second part of the FM radio receiver shown in Figure 8.

Referring first to the muting circuit shown in Figure 5, the collector electrodes of differential amplification transistors Q_1 and Q_2 for signal transmission are connected in common to respective collector electrodes of differential transistors Q_3 and Q_4 for forming the D.C. signal at the time of the muting operation. Constant current transistors Q_5 and Q_6 are alternately operated

by a switch SW_1 and are connected to the common emitter electrodes of the respective pairs of differential transistors Q_1 , Q_2 and Q_3 , Q_4 .

5 The bias voltage V_{B1} is applied to the base electrode of the differential amplification transistor Q_1 , to which the input signal IN is also applied, via the bias resistor R_B , whilst the bias voltage V_{B1} is directly applied to the base electrode of the differential transistor Q_3 . A negative feedback
10 signal is applied to the base electrodes of the transistors Q_2 and Q_4 via a feedback circuit β , in order to/the gain of the differential amplification transistor circuit and provide the D.C. bias voltage.

A load resistor R_L is connected to the
15 collector electrodes of the transistors Q_2 and Q_4 and also to the output terminal OUT. An input signal IN is applied to the base electrode of the transistor Q_1 via a coupling capacitor C_1 .

A switching transistor Q_7 is arranged
20 in parallel to the bias resistor R_B in order to prevent occurrence of the popping noise at the time of mute release after turning on the power source, and is controlled by a voltage V applied via a switch SW_2 . This switch SW_2 is placed into position a',

when the power source is applied, thereby turning on the transistor Q_7 . The transistor Q_7 is kept ON until the switch SW_1 is changed over to position b or before the release of the muting operation, and is turned off after the release of the muting operation. It is therefore preferred that both switches SW_1 and SW_2 be operated in an interlocking arrangement by the same control signal.

The muting operation by the switch SW_1 when the power source in this circuit is turned on is the same as in the circuit shown in Figure 1, and so its explanation is omitted. The bias resistor R_B is short-circuited by the transistor Q_7 which is rendered conductive by the switch SW_2 immediately after the power source is turned on. Therefore, as shown in the waveform diagram of Figure 6, the base voltage V_{B1}' of the differential amplification transistor Q_1 substantially follows the bias voltage V_{B1} , which quickly rises immediately the power source is turned on at the time t_1 . Accordingly, when the switch SW_1 is changed over to position b at the time t_2 to release the muting operation, the bias voltage V_{B1} and the voltage V_{B1}' become equal to each other so that the popping noise does not occur.

Incidentally, the voltage fluctuation occurring at the time t_1 immediately after turning on the power source (or the popping noise) can be eliminated by the muting circuit of the subsequent stage which also functions to protect the speaker connected to a power amplifier that is simultaneously turned on. However, when the popping noise occurs at the time t_2 , the muting operation of the muting circuit at the subsequent stage has already released so that the amplification circuit at the subsequent stage is operative and the voltage fluctuation is amplified as a loud popping noise.

Referring now to the second preferred form shown in Figure 7, the muting circuit includes circuit elements that are formed on a single chip silicon substrate in accordance with a well known semiconductor manufacturing technique. However, a capacitor C_1 , a resistor R_{20} and a capacitor C_3 connected via terminals P_1 and P_2 are formed by external components. The muting circuit of this embodiment also functions as a pre-amplifier for a stereo demodulation circuit in an FM stereo tuner.

Accordingly, the differential amplification transistor circuit for signal transmission consists

of transistors Q_1 , Q_1' , and Q_2 , Q_2' connected in Darlington configuration in order to realize a high input impedance and also to increase the open loop gain. The emitter electrodes of the transistors Q_1' and Q_2' on the input side are provided with constant current source circuits formed by transistors Q_{11} and Q_{12} and resistors R_6 and R_7 respectively. The emitter electrodes of the transistors Q_1 and Q_2 are coupled via emitter resistors R_1 and R_2 . A resistor R_3 is located between the junction of these resistors and the collector electrode of the constant current transistor Q_5 .

A resistor R_4 is likewise located between the collector electrode of the constant current transistor Q_6 and the emitter electrodes of the differential transistors Q_3 and Q_4 which are connected to each other.

A current mirror circuit is arranged at the collector electrodes of the amplification transistors Q_1 and Q_2 as a load, and consists of transistors Q_8 and Q_9 .

This amplified output is applied to an emitter follower output circuit consisting of a transistor Q_{10} and a resistor R_5 .

An output signal is obtained from an output terminal OUT and is fed back to the base electrodes of the transistors Q_4 and Q_2' . A capacitor C_2 for preventing oscillation is connected to the base electrode of the emitter follower transistor Q_{10} , the capacitor being an MOS (metal oxide semiconductor) capacitor.

A resistor R_B' for preventing electrostatic breakdown is connected to the base electrode of the input amplification transistor Q_1' .

When the power source is turned on, an integration voltage from the RC circuit R_{20} , C_3 connected to the terminal P_2 is applied to the base electrode of a transistor Q_{13} via a resistor R_{11} .

Level shift diodes Q_{14} and Q_{15} (the term "diode" will hereinafter include diode connected transistors) and a resistor R_{13} are connected in series with the emitter electrode of the transistor Q_{13} .

The voltage drop across the resistor R_{13} is applied to the base electrode of the transistor Q_{16} via a resistor R_{12} . Resistor R_{10} is arranged between the collector electrode of this transistor Q_{16} and a voltage source V_{cc2} , which is higher than the bias voltage V_{B1} . The collector voltage of the

transistor Q_{16} is applied to the base electrode of the transistor Q_7 as its controlling signal.

Accordingly, the transistor Q_{16} and the resistor R_{10} together form the switch SW_2 .

5 The voltage drop across the resistor R_{13} is applied to the base electrode of the transistor Q_{17} , and a diode Q_{18} is connected between the emitter electrode of this transistor Q_{17} and earth to act as a constant voltage source. Further, a
10 resistor R_{14} is located between the collector electrode of the transistor Q_{17} and a stabilized voltage source V_{ccl} . A voltage from the stabilized voltage source V_{ccl} which has been level-shifted by level shift diodes Q_{21} , Q_{22} and a resistor R_{19} is
15 applied to the base electrode of a transistor Q_{20} whilst the collector voltage of the transistor Q_{17} is applied to the base electrode of a transistor Q_{19} through a resistor R_{15} . The emitter electrodes of these transistors Q_{19} and Q_{20} are connected to each
20 other and to the stabilized voltage source V_{ccl} through a resistor R_{16} .

These transistors Q_{19} and Q_{20} are p-n-p transistors whose collector electrodes are connected to earth through resistors R_{17} and R_{18} ,

respectively. The collector voltages of these transistors Q_{19} and Q_{20} are applied as the controlling signals to the base electrodes of the constant current transistors Q_5 and Q_6 through resistors R_8 and R_9 respectively. Accordingly, these circuit elements form the switch SW_1 .

The operation of these switches SW_1 and SW_2 is as follows.

During the period from immediately after the power source is turned on until its integrated voltage at the terminal P_2 reaches $4V_{BE}$ (base-emitter voltage of the transistor or forward voltage of the diode), the transistor Q_{16} is held non-conductive so that the base voltage of the transistor Q_7 is as high as the voltage source V_{cc2} , and hence the transistor Q_7 is turned on.

When the voltage exceeds the above-mentioned voltage $4 V_{BE}$, the transistor Q_{16} is turned on so that the transistor Q_7 is turned off.

On the other hand, since the transistor Q_{17} is held non-conductive during the period before the abovementioned integration voltage reaches $5 V_{BE}$, the differential transistor Q_{19} is held non-conductive whilst the differential transistor Q_{20}

is held conductive. Accordingly, the constant current transistor Q_6 is operative whilst the constant current transistor Q_5 is inoperative, thereby performing the same operation as when the switch SW_1 is set to the position a. Thus, the muting operation is carried out.

When the voltage at the terminal P_2 exceeds $5 V_{BE}$, the transistor Q_{17} is turned on so that the differential transistor Q_{19} is turned on with the differential transistor Q_{20} being turned off. Consequently, the constant current transistor Q_5 is operative whilst the constant current transistor Q_6 is inoperative, thereby performing the same operation as when the switch SW_1 is set to the position b. Hence, muting is released and signal transmission is started.

Accordingly, the circuit operates so that the switching transistor Q_7 is turned off before the muting operation is released.

It should be noted that it is possible to employ a construction in which the constant current transistors Q_5 and Q_6 are alternatively turned off when the switching transistors are turned on.

As the switching means for short-circuiting the base bias resistor R_B , a MOSFET can be employed in

a modified form of the circuit.

Figure 8 is a block diagram showing the principal portions of a preferred form of an FM radio receiver which incorporates the above described muting circuit.

The FM radio receiver includes an FM intermediate frequency amplification-detection monolithic semiconductor integrated circuit IC_1 which includes an FM intermediate frequency amplification stage 1, an FM detection stage 2, a low frequency amplification stage 3 and a detuning detection circuit 4 and in which the mute control circuit is deleted in the low frequency amplification stage 3. Except in that the mute control circuit is omitted, this integrated circuit is the same as the above referred to monolithic semiconductor integrated circuit IC_1 for FM intermediate frequency amplification and detection as shown in Figure 3. However, the above described monolithic semiconductor integrated circuit IC_1 for FM intermediate frequency amplification and detection can be used in this embodiment by rendering its mute control circuit 6 inoperative.

The FM radio receiver also includes a monolithic semiconductor integrated circuit IC_2 for

FM stereo demodulation. Except those features which will hereinafter be described, this circuit is analogous to the above described monolithic semiconductor integrated circuit IC₂ such as one disclosed in the magazine "ELECTRONICS", pages 62 - 66, November, 1971 or to the "HA1196" circuit available commercially from us.

In the monolithic semiconductor integrated circuit IC₂' for FM stereo demodulation in this embodiment, the muting function is added to the pre-amplifier 7. A first mute control circuit 11 for controlling this muting function as well as a second mute control circuit 12 for controlling the muting circuit 10 are provided in the stereo demodulation output. A detection signal formed by the detuning detection circuit 4 is applied to both these mute control circuits 11 and 12, and different detection levels V_{L1} , V_{L2} are provided to discriminate the necessary mute control.

As shown in Figure 9, the discrimination level V_{L1} of the first mute control circuit 11 is set to the high level whilst the discrimination level V_{L2} of the second mute control circuit 12 is set to the low level so as to read the level difference

from a detuning detection signal V_M of the detuning detection circuit 4, which reaches the high level when the tuning frequency deviates excessively from the centre frequency f_0 of the S characteristic of the FM detection stage 2 and reaches the low level when tuning is established.

Accordingly, when detuning changes to tuning and the muting operation is released, the detuning detection signal V_M reaches a level below the first discrimination level V_{L1} so that the muting operation in the pre-amplifier 7 is released before the muting operation of the muting circuit 10 is released. In this instance, the voltage fluctuation V_{pop} occurs due to the change in the D.C. voltage in the S characteristic but since the muting operation in the muting circuit 10 is not yet released, the occurrence of the popping noise is eliminated.

On the other hand, when tuning changes to detuning and the muting operation starts, the detuning detection signal V_M first reaches a level above the second discrimination level V_{L2} so that muting of the pre-amplifier 7 is started after the muting operation of the muting circuit 10.

Accordingly, the popping noise occurring for the reason noted above is eliminated by muting circuit 10 which has already started its muting operation.

Since the mute control circuits 11 and 12 are formed in the same monolithic semiconductor integrated circuit IC_2 , the discrimination levels V_{L1} and V_{L2} for restricting their mute control operation are not affected by variance of the semiconductor elements, and consequently the mute control operation can be set to a high level of accuracy as described above.

Since no circuit element for shortening the signal transmission time such as a coupling capacitor C_{100} is positioned between the muting circuit in the pre-amplifier 7 and the muting circuit 10 for the stereo demodulation circuit 9, it is possible to make the timing difference for the start and release of the muting operation, corresponding to the level difference of the discrimination levels V_{L1} and V_{L2} , coincide with the time difference for the elimination of the popping noise.

In other words, the popping noise can be reliably eliminated by a simple circuit design in which the level difference between V_{L1} and V_{L2}

is set in accordance with the pulse width of the popping noise.

Incidentally, sufficient attenuation to eliminate noises between broadcasting stations cannot be obtained by use of only the muting circuit 10. Hence, it is necessary to arrange two muting circuits as described above.

Referring to the detailed circuit diagram shown in Figure 10, the circuit elements of the portion IC_2 encircled by dotted lines are formed on one silicon semiconductor chip by a known semiconductor manufacturing technique, and numerals in circles represent terminal numbers.

In the pre-amplifier 7, differential amplification transistors Q_1 , Q_2 and Q_3 , Q_4 for the signal transmission of the input signal IN from the low frequency amplification stage 3 are connected to each other in Darlington configuration with their collector electrodes respectively connected together, whilst the collector electrodes of differential transistors Q_{10} and Q_{11} for forming the D.C. signal at the time of the muting operation are connected to the collector electrodes of the Darlington pairs Q_1Q_2 and Q_3Q_4 respectively. Constant current circuits

consisting of transistors Q_6 and Q_7 and resistors R_5 and R_6 , respectively, are connected to the emitter electrodes of the input transistors Q_1 and Q_3 respectively. A constant bias voltage V_{B2} is applied to the base electrodes of these transistors Q_6 and Q_7 . The emitter electrodes of the transistors Q_2 and Q_4 are connected to each other via emitter resistors R_1 and R_2 respectively. A resistor R_3 is located between the junction of these resistors and the collector electrode of the constant current transistor Q_5 . A resistor R_4 is likewise located between the emitter electrodes of the differential transistors Q_{10} and Q_{11} and the collector electrode of the constant current transistor Q_{12} .

A current mirror circuit consisting of transistors Q_8 and Q_9 is connected as a load to the mutually connected collector electrodes of the differential amplification transistors Q_1 , Q_2 and Q_3 , Q_4 and to the mutually connected collector electrodes of the differential transistors Q_{10} and Q_{11} .

This amplification output is applied to an emitter follower output circuit consisting of a transistor Q_{13} and a resistor R_9 . A negative

feedback signal is obtained from the output of the emitter follower output circuit to be fed back to the base electrodes of the transistors Q_3 and Q_{11} and an output signal (composite signal V_{CON}) to be applied to a stereo demodulation circuit 9 which will be described in greater detail hereinafter. The composite signal is produced as an output from a second terminal via an inverting amplifier circuit consisting of a transistor Q_{14} , a collector resistor R_{10} and an emitter resistor R_{11} , and via an emitter follower circuit consisting of a transistor Q_{15} and an emitter resistor R_{12} .

A capacitor C_1 for preventing oscillation is connected to the base electrode of the transistor Q_{13} , and in a preferred form this capacitor is composed of an MOS (metal oxide semiconductor) capacitor.

The base bias voltage V_{B1} is applied to the base electrode of the input differential amplification transistor Q_1 via a base bias resistor R_7 and resistor R_8 and is applied directly to the base electrode of the differential transistor Q_{10} .

The base electrode of the transistor Q_1 is connected to the first terminal via the resistor R_8

which is provided in order to prevent dielectric breakdown. A composite input signal IN (in the case of the stereo broadcasting) is applied to this first terminal as an FM detection output signal through a coupling capacitor C_{100} . A bias circuit 13a constitutes the bias voltages V_{B1} and V_{B2} .

In the pre-amplifier 7, either one of the constant current transistors Q_5 and Q_{12} is alternatively rendered conductive in order to carry out the signal transmission of the input signal IN or the muting operation.

When the constant current transistor Q_5 is conductive and the constant current transistor Q_{12} non-conductive, the differential transistors Q_{10} and Q_{11} are turned off whilst the differential amplification transistors Q_2 and Q_4 are rendered conductive so that the input signal IN is transmitted. In the opposite case, the differential amplification transistors Q_2 and Q_4 are turned off with the differential transistors Q_{10} and Q_{11} being conductive so that the signal transmission of the input signal IN is inhibited and muting is carried out. In this case, only the same D.C. signal as the bias voltage V_{B1} is obtained at the emitter output of the

transistor Q_{13} due to the operation of the differential transistors Q_{10} and Q_{11} .

A transistor Q_{16} for short-circuiting the bias resistor R_7 is arranged across both ends of this resistor in order to prevent occurrence of the popping noise when the power source is turned on.

Emitter electrodes of differential transistors Q_{35} and Q_{36} are connected to a stabilized voltage source V_{cc3} through a resistor R_{34} , and resistors R_{32} and R_{33} are connected between the collector electrodes of these transistors and earth respectively. The transistors Q_{35} and Q_{36} together form a switching circuit for alternatively actuating either one of the constant current transistors Q_5 and Q_{12} .

A voltage ($V_{cc3} - 2V_{BE}$) generated by level shift diodes Q_{37} and Q_{38} (the term "diode" will hereinafter include transistors of the diode type) and a resistor R_{35} is applied to the base electrode of the transistor Q_{36} . A diode Q_{34} is connected to the emitter electrode of the transistor Q_{33} as a constant voltage element and a resistor R_{30} is connected to its collector electrode. A control voltage is applied to the base electrode of this

transistor Q_{33} , whose collector voltage is in turn applied to the base electrode of the transistor Q_{35} through a resistor R_{31} . Accordingly, when the transistor Q_{33} is held conductive, the transistor Q_{35} is turned on whilst the transistor Q_{36} is turned off so that the constant current transistor Q_5 is rendered conductive to transmit the input signal IN to the preamplifier 7. On the other hand, when the transistor Q_{33} is held non-conductive, the transistor Q_{35} is turned off whilst the transistor Q_{36} is turned on so that the constant current transistor Q_{12} is rendered conductive to carry out the muting operation in the preamplifier 7.

A resistor R_{48} is located between a voltage source V_{cc2} , which is higher than the bias voltage source V_{B1} , and the collector electrode of a transistor Q_{32} , and a control signal similar to the abovementioned control signal is applied to the base electrode of the transistor Q_{32} , the collector voltage of which is in turn applied to the base electrode of a switching transistor Q_{16} .

An integration voltage of the voltage

source V_{cc} due to an integration circuit R_{103} and C_{107} formed by external components at the eighth terminal is applied to the base electrode of a transistor Q_{23} through a resistor R_{21} , and level shift diodes Q_{24} and Q_{25} and a resistor R_{22} are connected in series between the emitter electrode of this transistor Q_{23} and earth. The voltage drop across the resistor R_{22} generates the above-mentioned control signal that is to be applied to the base electrode of the transistor Q_{32} . The terminal voltage of this resistor R_{22} is applied to the base electrode of transistor Q_{32} through a resistor R_{29} and to the base electrode of transistor Q_{33} through a resistor R_{23} , respectively.

The integrated voltage from this eighth terminal when the power source is turned on is utilized for eliminating the popping noise when the power source is turned on.

On the other hand, a detuning detection signal V_M generated by the detuning detection circuit 4 is converted into D.C. by an RC time constant circuit consisting of resistors R_{104} and R_{105} and a capacitor C_{108} , and is then applied to the seventh terminal. This detuning detection signal is applied

to the base electrode of a transistor Q_{26} which is provided with a diode Q_{27} to act as a constant voltage element being connected between the emitter electrode of the transistor Q_{26} and earth. The collector electrode of the transistor Q_{26} is connected to the base electrode of the transistor Q_{33} .

Accordingly, the circuit including this transistor Q_{26} forms the first mute control circuit 11.

The detuning detection signal is applied to the second mute control circuit 12 via a resistor R_{24} and the base and emitter electrodes of transistors Q_{28} and Q_{29} .

The second mute control circuit 12 employs: a Schmidt circuit consisting of a reference voltage circuit formed by differential transistors Q_{39} and Q_{40} provided with a resistor R_{38} at their common emitter electrodes, a resistor R_{41} , a transistor Q_{45} connected in diode configuration, a diode Q_{46} , and voltage dividing resistors R_{39} and R_{40} arranged between the collector and emitter electrodes of the transistor Q_{45} for generating a reference voltage to be applied to the base electrode of the transistors Q_{40} . A current feedback circuit formed as a current mirror circuit is interposed between

the collector and the base electrodes of the other transistor Q_{39} and is composed of transistors Q_{43} and Q_{44} and emitter resistors R_{36} and R_{37} . This Schmidt circuit has hysteresis with respect to an applied

5 voltage which turns it on and an applied voltage which turns it off. Diodes Q_{41} and Q_{42} for performing the voltage clamp are connected to the base electrode of the transistor Q_{39} and the detuning detection signal obtained from the emitter electrode of the transistor

10 Q_{29} is applied, via a resistor R_{27} , to an inverter circuit consisting of a transistor Q_{30} and a resistor R_{50} . A transistor Q_{31} , which is controlled by the collector output of the transistor Q_{30} , is connected to the base electrode of the transistor Q_{39} .

15 The output signal from the preamplifier 7 generated at the second terminal via the dielectric breakdown prevention resistor R_{13} is applied to a PLL circuit 8 from the third terminal via a capacitor

20 C_{101} . In the PLL circuit a 38KHz switching signal for stereo demodulation in synchronism with 19KHz pilot signal is formed, and is applied to the stereo demodulation circuit 9.

The stereo demodulation circuit 9 is composed of a known switching type stereo demodulation

circuit. This stereo modulation circuit 9 consists of transistors Q_{17} to Q_{22} forming a balanced-differential type multiplication circuit and resistors R_{16} to R_{20} . The stereo demodulation circuit 9 of this switching type has been disclosed in the periodical "IEEE TRANSACTIONS ON BROADCAST AND TELEVISION RECEIVERS", VOLUME BTR-14, NUMBER 3, pp. 58 to 73, October 1968, and a semiconductor integrated circuit for an FM stereo demodulation circuit using the PLL circuit has been disclosed in "Electronics" above referred to.

A bias circuit 13b is provided for generating a bias voltage V_{B3} .

The output of this stereo demodulation circuit 9 passes through post-amplifiers 14L, 14R so that the left-hand channel output is obtained from the fourth terminal and the right-hand channel output is obtained from the fifth terminal. Lowpass filters 15L, 15R are also connected to the fourth and fifth terminals, respectively. Pairs of capacitors C_{103} , C_{104} and C_{105} , C_{106} are connected in series and are also connected to the fourth and fifth terminals, respectively. Transistors Q_{100} and Q_{101} are located between the respective junctions

of these series capacitors and earth. These capacitors and transistors together form the muting circuit 10.

The base electrodes of these transistors
 5 Q_{100} and Q_{101} are connected to the sixth terminal through resistors R_{101} and R_{102} , respectively.

The collector voltage of transistor Q_{36} , which permits the muting operation in the pre-amplifier 7, is applied to the base electrode
 10 of transistor Q_{48} through a resistor R_{44} , and transistor Q_{51} generates a mute control output signal. Diodes Q_{49} and Q_{50} connected to the collector electrode of the transistor Q_{48} apply an operating voltage to this transistor Q_{51} . A resistor R_{45} is
 15 located between the series diodes Q_{49} and Q_{50} and the collector electrode of the transistor Q_{48} , and a resistor R_{46} is connected in parallel with the series diodes Q_{49} and Q_{50} .

The feedback output current of the
 20 above referred to Schmidt circuit is also applied to the base electrode of the output transistor Q_{47} , and a mute control output signal to the sixth terminal is generated via a resistor R_{49} from the commonly connected collector electrodes of the output

transistors Q_{51} and Q_{47} .

The above described circuit operates as follows.

First, when the power source is turned on, transistor Q_{32} is held non-conductive and transistor Q_{16} is held conductive until the integration voltage to the eighth terminal reaches $4 V_{BE}$ (base-to-emitter voltage of the transistor or forward voltage of the diode). Accordingly, in response to the rising bias voltage which is following the voltage source V_{cc1} , the coupling capacitor C_{100} charges and the bias voltage of the transistor Q_1 rises rapidly so that the bias voltage of the transistors Q_3 and Q_{11} generated by the feedback also rises rapidly.

On the other hand, during the period until the above-mentioned integration voltage reaches $5 V_{BE}$, the transistors Q_{33} and Q_{35} are held non-conductive so that the constant current transistor Q_5 is turned off whilst the constant current transistor Q_{12} is turned on. When the transistor Q_{36} is turned on, the transistors Q_{48} and Q_{51} are also turned on. Accordingly, the transistors Q_{100} and Q_{101} of the muting circuit 10

are turned on and carry out the muting operation in the pre-amplifier 7 and in the muting circuit 10.

Before the integration voltage reaches $5V_{BE}$, the transistor Q_{32} is turned on and hence the transistor Q_{16} is turned off. When the integration voltage reaches $5V_{BE}$, the transistors Q_{33} and Q_{35} are turned on whilst the transistors Q_{48} and Q_{51} are turned off so that the muting operation ceases in the pre-amplifier circuit 7 and in the muting circuit 10.

Since during the rise of the bias voltage of the transistor Q_1 no delay is caused by the time constant determined by the capacitor C_{100} and the resistor R_7 , no difference is generated between the bias voltage V_{B1} and the bias voltage formed by the feedback operation. Consequently, the popping noise can be prevented.

On the other hand, when tuning to a desired station, the integration voltage at the eighth terminal is fully charged to the power source voltage V_{cc} , so at the time of detuning the voltage at the seventh terminal is at the high level and transistor Q_{26} is turned on. Accordingly, the transistor Q_{33} is turned off, whereby the muting operation is carried out in the pre-amplifier 7 and in the muting

circuit 10. In this case, since the eighth terminal is at the high level, the transistor Q_{32} is turned on and the switching transistor Q_{16} which is connected to the bias resistor R_7 , is turned off.

5 Since the seventh terminal is at the high level due to the detuning detection signal, the transistor Q_{39} forming the Schmidt circuit is turned on and the muting circuit 10 is also made to perform the muting operation by this mute control circuit 12.

10 When the detuning detection signal V_M drops below $2 V_{BE}$ upon tuning, the transistor Q_{26} is turned off and the transistor Q_{33} is turned on so that the muting operation in the pre-amplifier 7 ceases. In this case, due to the S characteristic of the FM detection
15 output, the voltage fluctuation occurs but is removed by the continued muting performed by the muting circuit 10.

 When the detuning detection signal V_M drops further below V_{BE} , the transistor Q_{30} is turned off
20 and thereby turns on the transistor Q_{31} so that the differential transistor Q_{39} is turned off, and the action of the muting circuit 10 ceases at this time.

 When the detuning is again effected and the rise voltage of its detection signal V_M reaches

V_{BE} , the transistor Q_{30} is turned on, turning off the transistor Q_{31} . In this case, however, a voltage higher than V_{BE} , e.g. about $1.5 V_{BE}$, is applied to the base electrode of the transistor Q_{40} by the transistors Q_{45} and Q_{46} and the resistors R_{39} and R_{40} , and consequently the transistor Q_{39} is kept off and the muting circuit 10 does not operate as yet.

When the detuning detection signal V_M reaches the reference voltage ($1.5 V_{BE}$), the transistor Q_{39} is turned on, and muting is effected in the muting circuit 10.

In this manner, the mute control circuit 12 has a hysteresis characteristic which has its discrimination levels at V_{BE} and $1.5 V_{BE}$.

Next, when the detuning detection signal reaches $2 V_{BE}$, transistor Q_{26} is turned on in order to actuate transistor Q_{33} and begin muting in the pre-amplifier 7. In this case, too, due to the S characteristic in the FM detection output, the voltage fluctuation occurs but is eliminated because the muting circuit 10 has already started operating.

The hysteresis characteristic is provided by use of the Schmidt circuit because, as can be clearly understood from the operation waveform diagram

shown in Figure 9, no problem occurs even if the difference of timing between the start of the muting operation in the preamplifier 7 and the start of the muting operation in the muting circuit 10 at the beginning of the muting operation is made smaller than the difference of timing at the release of the muting operation. In other words, since the differential waveform in the D.C. voltage fluctuation of the S characteristic is produced as the popping noise, it is necessary for the timing difference to correspond to the pulse width of this popping noise in order to stop the muting operation silently, and the timing of muting circuit 10 should be slightly advanced at the start of the muting operation. Additionally, the hysteresis characteristic is an extremely effective means for compensating for unstability of the detuning detection signal.

It should be understood that the monolithic semiconductor integrated circuit IC₂, forming the FM stereo demodulation circuit can be provided with additional circuits such as a circuit for FM stereo-monoaural detection, selection and display, and a circuit for cancelling the 19KHz pilot signal.

Any signal can be used as the detuning

5 detection signal so long as it is capable of discriminating between tuning and detuning, and the polarity of its signal level may become simultaneously high levels. In this case, the discrimination level may be set to the reverse level difference.

Attention is drawn to our Application No.82.29214 (Serial No.) which has been divided out of the present Application in which there is claimed in claim 1, an F.M. radio receiver including:

- 10 (a) an FM intermediate frequency amplification stage;
- (b) an FM detector having its input terminal connected to the output terminal of said FM intermediate stage;
- (c) a detuning detection circuit responsive to the intermediate frequency signal of said FM intermediate
- 15 frequency amplification stage;
- (d) a pre-amplifier having its input terminal responsive to the output signal of said FM detector, the signal transmitting operation of said pre-amplifier being substantially inhibited when a control input signal is applied to the
- 20 control input terminal of said preamplifier;
- (e) a phase locked loop circuit for obtaining a switching signal in synchronism with a pilot signal contained in a stereo composite signal obtained from said FM detector via said pre-amplifier;
- 25 (f) a stereo demodulation circuit for providing right-hand and left-hand channel demodulation output signals when applied with said stereo composite signal from said pre-amplifier and said switching signal from said phase

locked loop circuit;

- (g) a muting circuit having first and second input terminals, first and second output terminals and a control input terminal, said first and second input terminals
5 receiving said right-hand and left-hand channel demodulation output signals, respectively, and said control input terminal receiving the control input signal, thereby substantially inhibiting the signal transmitting operation between said first input terminal and said
10 first output terminal and the signal transmitting operation between said second input terminal and said second output terminal respectively;
- (h) a first mute control circuit receiving at its input terminal the output signal of said detuning detection
15 circuit and applying an output signal to said control input terminal of said pre-amplifier, said first mute control circuit further having a first discrimination level with respect to the output signal of said detuning detection signal to be applied to the input terminal
20 thereof; and
- (i) a second mute control circuit receiving at its input terminal the output signal of said detuning detection circuit and applying an output signal to the control input terminal of said muting circuit, said second mute
25 control circuit further having a second discrimination level with respect to the output signal of said detuning detection circuit to be applied to the input terminal thereof; whereby a level difference is set between said first discrimination level and said second discrimination
30 level so that when the reception condition of said FM radio receiver changes from the tuning state to the detuning state, the signal transmitting operation of said muting circuit is substantially inhibited and thereafter the signal transmitting operation of said pre-amplifier is substantially inhibited.



CLAIMS.

1. A muting circuit including:

(a) first and second transistors having their emitter electrodes connected to each other;

(b) third and fourth transistors having their emitter electrodes connected to each other;

(c) a first constant current source connected to the emitter electrodes of said first and second transistors;

(d) a second constant current source connected to the emitter electrodes of said third and fourth transistors;

(e) a coupling capacitor for feeding an input signal to the base electrode of said first transistor;

(f) a bias resistor having one end thereof connected to the base electrode of said first transistor and the other end connected to the base electrode of said third transistor;

(g) bias voltage generation means connected to the base electrode of said third transistor and to said other end of said bias resistor;

(h) load means connected to the collector electrode of said second transistor and to the collector electrode of said fourth transistor;



(i) a feedback circuit connected between said load means and the base electrodes of said second and fourth transistors;

(j) means for alternatively controlling and bringing
5 either one of said first and second constant current sources into the operative state and the other into the inoperative state; and

(k) a switching element connected between said one end and said other end of said bias resistor and
10 actuated into the ON state for a predetermined period after the switching on of the power source of the muting circuit.

2. A muting circuit according to Claim 1, wherein said first constant current source includes a
15 fifth transistor having its collector and emitter electrodes connected to the emitter electrodes of said first and second transistors and to a reference potential, respectively; and wherein said second constant current source includes a sixth transistor
20 having its collector and emitter electrodes connected to the emitter electrodes of said third and fourth transistors and to said reference potential respectively.

3. A muting circuit according to Claim 2, wherein said switching element includes a seventh
25 transistor having the collector-to-emitter path thereof connected in parallel to both ends of said bias resistor.



4. A muting circuit according to claim 3,
wherein a time constant circuit is connected between
said power source and said reference potential and
the base electrodes of said fifth, sixth and seventh
5 transistors are controlled on the basis of the output
signal of said time constant circuit.
5. A muting circuit constructed and arranged
to operate substantially as herein described with
reference to and as illustrated in Figures 5 and 7
10 of the accompanying drawings.
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