CLAIMS

1. An apparatus, comprising:

a memory cell including:

a memory element; and

a selector device electrically coupled to the memory element;

a first memory access line coupled to the memory cell;

a second memory access line coupled to the memory cell;

a first access line driver coupled to the first memory access line; and

a second access line driver coupled to the second memory access line,

wherein the first and second access line drivers are configured to:

provide a first voltage at a first polarity across the memory cell to write a first logic state to the memory cell,

provide a second voltage at a second polarity across the memory cell to write a second logic state to the memory cell,

provide a third voltage at the first polarity across the memory cell to write a third logic state to the memory cell, and

provide a fourth voltage at the second polarity across the memory cell to write a fourth logic state to the memory cell,

wherein, during a read operation on the memory cell, the memory cell exhibits a threshold voltage, wherein the threshold voltage is dependent on a logic state written to the memory cell.

2. The apparatus of claim 1, wherein the first, second, third, and fourth logic states correspond to values of a first bit and a second bit of data stored in the memory cell.

3. An apparatus, comprising:

a memory cell including:

a memory element; and

a selector device electrically coupled to the memory element;

a first memory access line coupled to the memory cell;

a second memory access line coupled to the memory cell;

a first access line driver coupled to the first memory access line; and

a second access line driver coupled to the second memory access line,

wherein the first and second access line drivers are configured to:

provide a first voltage at a first polarity across the memory cell to write a first logic state to the memory cell,

provide a second voltage at a second polarity across the memory cell to write a second logic state to the memory cell,

provide a third voltage at the first polarity across the memory cell to write a third logic state to the memory cell, and

provide a fourth voltage at the second polarity across the memory cell to write a fourth logic state to the memory cell, wherein the first, second, third, and fourth logic states correspond to values of a first bit and a second bit of data stored in the memory cell, wherein the first bit is stored in the memory element and the second bit is stored in the selector device.

4. The apparatus of claim 3, wherein a value of the first bit is based, at least in part, on whether the first or second voltage was applied across the memory cell.

5. The apparatus of claim 3, wherein a value of the second bit is based, at least in part, on whether the first or second polarity was applied across the memory cell.

6. The apparatus of claim 1, wherein the memory cell comprises a chalcogenide material.

7. The apparatus of claim 1, wherein the memory cell comprises at least one of silicon (Si), selenium (Se), arsenic (As), and germanium (Ge).

8. An apparatus, comprising:

a memory cell including:

a memory element; and

a selector device electrically coupled to the memory element;

a first memory access line coupled to the memory cell;

a second memory access line coupled to the memory cell;

a first access line driver coupled to the first memory access line; and

a second access line driver coupled to the second memory access line,

wherein the first and second access line drivers are configured to:

provide a first voltage at a first polarity across the memory cell to write a first logic state to the memory cell,

provide a second voltage at a second polarity across the memory cell to write a second logic state to the memory cell,

provide a third voltage at the first polarity across the memory cell to write a third logic state to the memory cell, and

provide a fourth voltage at the second polarity across the memory cell to write a fourth logic state to the memory cell,

wherein the first and second voltages are equal magnitudes and the third and fourth voltages are equal magnitudes.

9. The apparatus of claim 1, wherein the third and fourth logic states correspond to a same logic state.

10. The apparatus of claim 1, wherein the first access line driver is configured to provide a negative voltage and the second access line driver is configured to provide a non-negative voltage to provide the first or third voltage having the first polarity.

11. The apparatus of claim 1, wherein the first access line driver is configured to provide a first non-negative voltage and the second access line driver is configured to provide a second non-negative voltage to provide the first or third voltage having the first

polarity, wherein the second non-negative voltage is greater than the first non-negative voltage.

12. An apparatus, comprising:

a memory cell configured to store multiple bits of data, wherein the multiple bits of data correspond to logic states of the memory cell, wherein the memory cell includes a memory element and a selector device coupled to the memory element;

a first memory access line coupled to the memory cell; and

a second memory access line coupled to the memory cell,

wherein at least one of the multiple bits of data is determined by a magnitude of a current applied across the memory cell during a write pulse, and wherein at least one of the multiple bits of data is determined by a polarity of a voltage applied across the memory cell during the write pulse, wherein the at least one of the multiple bits of data determined by the polarity of the voltage are stored in the selector device..

13. The apparatus of claim 12, wherein the at least one of the multiple bits of data determined by the magnitude of the current are stored in the memory element.

14. The apparatus of claim 12, wherein the first memory access line is configured to provide a first non-negative voltage and the second memory access line is configured to provide a second non-negative voltage to provide the write pulse having the first polarity, wherein the second non-negative voltage is greater than the first non-negative voltage.

15. The apparatus of claim 12, wherein the magnitude of the current is one of a plurality of magnitudes, wherein a crystalline state of a phase change material of the memory cell depends, at least in part, on the magnitude of the current, and wherein a logic state of the memory cell depends, at least in part, on the crystalline state of the phase change material.

16. An apparatus, comprising:

a memory cell configured to store multiple bits of data, wherein the multiple bits of data correspond to logic states of the memory cell;

a first memory access line coupled to the memory cell; and

a second memory access line coupled to the memory cell,

wherein at least one of the multiple bits of data is determined by a magnitude of a current applied across the memory cell during a write pulse, and wherein at least one of the multiple bits of data is determined by a polarity of a voltage applied across the memory cell during the write pulse, wherein the memory cell exhibits one of a plurality of threshold voltages responsive to a read operation, wherein the plurality of threshold voltages correspond to the logic states of the memory cell.

17. The apparatus of claim 12, further comprising a memory array including a plurality of memory cells and a plurality of memory access lines coupled to at least some of the plurality of memory cells,

wherein the memory cell is one of the plurality of memory cells and the first and second memory access lines are each one of the plurality of memory access lines.

18. The apparatus of claim 17, wherein the memory array is a two-dimensional (2D) array or a three-dimensional (3D) array.

19. The apparatus of claim 12 further comprising a sense amplifier coupled to the first memory access line or the second memory access line, the sense amplifier configured to sense a current through the memory cell responsive to a read operation.

20. A method, comprising:

selecting a voltage of a write pulse from between a first voltage and a second voltage;

selecting a polarity of the write pulse from between a first polarity and a second polarity;

applying the write pulse having the selected voltage and polarity across a memory cell, wherein the write pulse:

writes a first logic state to the memory cell when the selected voltage is the first voltage and the selected polarity is the first polarity,

writes a second logic state to the memory cell when the selected voltage is the first voltage and the selected polarity is the second polarity,

writes a third logic state to the memory cell when the selected voltage is the second voltage and the selected polarity is the first polarity, and

writes a fourth logic state to the memory cell when the selected voltage is the second voltage and the selected polarity is the second polarity.

21. The method of claim 20, wherein selecting the voltage corresponds to selecting a value of a first bit to be written to the memory cell.

22. The method of claim 20, wherein selecting the polarity corresponds to selecting a value of a second bit to be written to the memory cell.