in-out line. The decode transistors T9, T10 are used to transfer data between the bit lines BL, /BL and the global bit lines IO, /IO.

Although sense amplifiers are technically necessary, from an economical point of view the sense amplifiers can be considered as service circuits of the memory array and therefore as overhead that increases the area of the entire circuit and thus also its cost of fabrication.

Therefore, continuous efforts are made to minimize the area consumption of such sense amplifiers.

Summary of the invention

~~The~~ Embodiments of the invention ~~aims~~ aim at ~~proposing~~ providing a simplified circuit for sensing a difference in voltage on a pair of dual signal lines.

~~In this respect, the invention proposes a~~According to ~~its~~ a first aspect of the present invention, there is provided a circuit for sensing a difference in voltage on a pair of dual signal lines comprising a first signal line (BL) and a second signal line (/BL) complementary to the first signal line, comprising:

- a pair of cross-coupled inverters arranged between the first and the second signal lines, each inverter having a pull-up transistor (T1, T2) and a pull-down transistor (T3, T4), the sources of the pull-up transistors or of the pull-down transistors being respectively connected to a first (V_{HIO}) and a second ($V_{H/IO}$) pull voltage signals,
- a decode transistor (T11, T12) having source and drain terminals respectively coupled to one of the first and second signal lines and a gate controlled by a decoding control signal (CSL), whereby when the decode transistor is turned on by the decoding control signal, a short circuit is established between the first and the second signal lines through which current flows from one of the first and second pull voltage signals, thereby generating a disturb in between the first and the second pull voltage signals.

~~Other p~~Preferred, although non limitative, ~~aspects~~ embodiments of this circuit are as follows:

- the sources of the pull-up transistors are connected to the first and second pull up voltage signals;
- it further comprises a foot switch transistor intercalated between the sources of the pull-down transistors and a pull-down voltage source, the foot switch transistor being controlled by a sense signal;

- the decode transistor, the pull-up and the pull-down transistors are dual gate transistors;
- it is made on a semiconductor-on-insulator substrate comprising a thin layer of semiconducting material separated from a substrate by an insulating layer, and the

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dual gate transistors each comprises a first and a second gate, one of which is a back gate formed in the substrate below the insulating layer;

- the decode transistor has a first gate controlled by the decoding control signal and a second gate controlled by an equalization control signal;
- the first gate of the decode transistor is a back gate;
- the first and second signal lines are bit lines of a memory cell array.

According to another aspect, the invention relates to a semiconductor memory comprising at least one array of memory cells and at least one circuit according to the first aspect of the invention.

According to yet another aspect, the invention relates to ~~a method of operating~~ a method for sensing a difference in voltage on a pair of dual signal lines comprising a first signal line and a second signal line complementary to the first signal line, comprising the steps of turning on the decode transistor of a circuit according to the first aspect of the invention, and of sensing the difference of current or of voltage between the pull voltage signals with a current sense amplifier or a voltage sense amplifier.

Brief description of the drawings

Other aspects, goals and advantages of the invention will become more apparent upon reading the following detailed description of preferred embodiments thereof, given by way of examples and with reference to the accompanying drawings upon which:

- figure 1, already described above, shows on conventional sense amplifier circuit;
- figure 2 shows a circuit according to a possible embodiment of the invention;
- figure 3 shows a sense amplifier circuit with dual gate transistors as previously proposed by the Applicant with no dedicated precharge transistors;
- figure 4 shows a circuit according to another embodiment of the invention, based on the design of figure 3;
- figure 5 shows a circuit according to yet another embodiment of the invention.

On these figures, functionally similar transistors have identical numerical references.

Detailed description of preferred embodiments of the invention

In its broader aspect, the invention relates to a new manner of sensing a difference in voltage on a pair of dual signal lines. Although it will be described here below in relation to a sense amplifier circuit and dual signal lines in the form of a bit line and a complementary bit

CLAIMS

1. A circuit for sensing a difference in voltage on a pair of dual signal lines comprising a first signal line (BL) and a second signal line (/BL) complementary to the first signal line, comprising:

- a pair of cross-coupled inverters arranged between the first and the second signal lines, each inverter having a pull-up transistor (T1, T2) and a pull-down transistor (T3, T4), the sources of the pull-up transistors or of the pull-down transistors being respectively connected to a first (V_{HIO}) and a second ($V_{H/IO}$) pull voltage signals,
- a decode transistor (T11, T12) having source and drain terminals respectively coupled to one of the first and second signal lines and a gate controlled by a decoding control signal (CSL), whereby when the decode transistor is turned on by the decoding control signal, a short circuit is established between the first and the second signal lines through which current flows from one of the first and second pull voltage signals, thereby generating a disturb in between the first and the second pull voltage signals.

2. Circuit according to claim 1, wherein the sources of the pull-up transistors are connected to the first and second pull up voltage signals.

3. Circuit according to claim 2, further comprising a foot switch transistor intercalated between the sources of the pull-down transistors and a pull-down voltage source, the foot switch transistor being controlled by a sense signal.

4. Circuit according to any one of the preceding claims, wherein the decode transistor, the pull-up and the pull-down transistors are dual gate transistors.

5. Circuit according to the preceding claim, made on a semiconductor-on-insulator substrate comprising a thin layer of semiconducting material separated from a substrate by an insulating layer, wherein the dual gate transistors each comprise a first and a second gate, one of which is a back gate formed in the substrate below the insulating layer.

6. Circuit according to one of claims 4 or 5, wherein the decode transistor has a first gate controlled by the decoding control signal and a second gate controlled by an equalization control signal.