

HIGH-SPEED SERIAL INTERFACE AND DATA TRANSMISSION METHOD

ABSTRACT

Embodiments of this application relate to the field of chip technologies, and provide a high-speed serial interface and a data transmission method, to reduce power consumption of a physical layer circuit of a high-speed serial interface when no service data is being sent. The high-speed serial interface includes a physical layer circuit at a transmit end, a monitor, a clock gating circuit, a control bitstream generation circuit, and a random bitstream generation circuit, and further includes: The monitor is configured to: when no service data is being sent, indicate the clock gating circuit to stop sending a clock signal to partial modules in the physical layer circuit at the transmit end. The control bitstream generation circuit sends a first control bitstream through a serializer/deserializer, to indicate that the transmit end has turned off partial modules in the physical layer circuit at the transmit end, or indicate that the transmit end is to turn off partial modules in the physical layer circuit at the transmit end, or indicate a receive end to turn off partial modules in a physical layer circuit at the receive end. The random bitstream generation circuit sends a random bitstream. Embodiments of this application are used in a process of reducing power consumption of a physical layer circuit.

Figure 3A