Thus, the existing double-BOX technology for digital applications is incompatible with radiofrequency applications.

BRIEF DESCRIPTION OF THE INVENTION

One aim of the invention is to provide a semiconductor-on-insulator structure allowing the aforementioned drawbacks to be overcome. The invention aims to provide such a structure allowing digital applications and radiofrequency applications to be combined.

An aspect of the invention provides a semiconductor-on-insulator multilayer structure, comprising in succession from a back side to a front side of the structure:

- a semiconductor carrier substrate having an electrical resistivity comprised between 500 Ω.cm and 30 kΩ.cm,
- a first electrically insulating layer,
- an intermediate layer,
- a second electrically insulating layer, which has a thickness smaller than that of the first electrically insulating layer,
- an active semiconductor layer,

the multilayer structure being characterized in that it comprises:

- at least one FD-SOI region, in which the intermediate layer is a semiconductor layer,
- at least one RF-SOI region, adjacent to the FD-SOI region, in which the intermediate layer is a third electrically insulating layer, said RF-SOI region comprising at least one radiofrequency component plumb with the third electrically insulating layer.

According to example embodiments, the structure has the following various features, which may be implemented alone or in technically feasible combinations thereof:

- the sum of the thicknesses of the first electrically insulating layer, of the second electrically insulating layer, and of the third electrically insulating layer is comprised between 50 nm and 1500 nm;
- the structure furthermore comprises a charge-trapping layer arranged between the carrier substrate and the first electrically insulating layer;
- the charge-trapping layer is made of polysilicon or of porous silicon;
- the intermediate semiconductor layer is made of crystalline or polycrystalline material;
- the intermediate semiconductor layer is made of amorphous material;
- the first electrically insulating layer is a layer of silicon oxide;
- the second electrically insulating layer is a layer of silicon oxide;
- the third electrically insulating layer is a layer of silicon oxide;

- the first electrically insulating layer has a thickness comprised between 20 nm and 1000 nm;
- the second electrically insulating layer has a thickness comprised between 10 nm and 100 nm;
- the active semiconductor layer has a thickness comprised between 3 nm and 30 nm.

Another aspect of the invention provides a process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:

- providing a first donor substrate,
- forming a weakened zone in said first donor substrate, so as to delineate an intermediate first semiconductor layer,
- transferring said intermediate first semiconductor layer to a semiconductor carrier substrate, a first electrically insulating layer being at the interface between the donor substrate and the carrier substrate so as to form an intermediate structure comprising the carrier substrate, the first electrically insulating layer and the transferred intermediate first semiconductor layer,
- locally removing one segment of the intermediate first semiconductor layer down to the first electrically insulating layer in order to form a cavity,
- depositing an electrically insulating layer, called the third electrically insulating layer, in the cavity,
- providing a second donor substrate,
- forming a weakened zone in said second donor substrate, so as to delineate an active second semiconductor layer,
- transferring said active second semiconductor layer to the intermediate structure, a second electrically insulating layer being at the interface between the second donor substrate and the intermediate structure,
- producing:
    - at least one digital component in the active second semiconductor layer plumb with the intermediate first semiconductor layer, in order to form an FD-SOI region, and
    - at least one radiofrequency component plumb with the third electrically insulating layer, in order to form an RF-SOI region.

Another aspect of the invention provides a process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:

- forming an intermediate structure by depositing an intermediate first semiconductor layer on a carrier substrate covered with a first electrically insulating layer,
- locally removing one segment of the intermediate first semiconductor layer down to the first electrically insulating layer in order to form a cavity,
- depositing an electrically insulating layer, called the third electrically insulating layer, in the cavity,
- providing a donor substrate,
- forming a weakened zone in said donor substrate, so as to delineate an active second semiconductor layer,
- transferring said active second semiconductor layer to the said intermediate structure, a second electrically insulating layer being at the interface between the donor substrate and the said intermediate structure,
- producing:
    - at least one digital component in the active second semiconductor layer plumb with the intermediate first semiconductor layer, in order to form an FD-SOI region, and
    - at least one radiofrequency component plumb with the third electrically insulating layer, in order to form an RF-SOI region.

According to example embodiments, the processes have the following various features, which may be implemented alone or in technically feasible combinations thereof:

- the radiofrequency component is produced in the active second semiconductor layer;
- the local removal of a segment of the intermediate first semiconductor layer and the deposition of a third electrically insulating layer in the cavity are carried out after the transfer of the second semiconductor layer to the intermediate structure;
- the process furthermore comprises forming a charge-trapping layer on the carrier substrate, said charge-trapping layer being arranged between the carrier substrate and the first electrically insulating layer;
- the local removal comprises depositing a mask by lithography and etching the intermediate first semiconductor layer through at least one aperture of said mask;
- the process furthermore comprises, before the transfer of said second semiconductor layer to the intermediate structure, treating the free surfaces of the intermediate first semiconductor layer and the third electrically insulating layer in order to decrease the roughness thereof.

The multilayer structure according to embodiments of the invention can serve as carrier for the fabrication of transistors, in particular MOSFETs. MOSFETs are semiconductor devices comprising three active electrodes, namely an input electrode called the

CLAIMS

1. Semiconductor-on-insulator multilayer structure, comprising in succession from a back side to a front side of the structure:
   - a semiconductor carrier substrate having an electrical resistivity comprised between 500 Ω.cm and 30 kΩ.cm,
   - a first electrically insulating layer,
   - an intermediate layer,
   - a second electrically insulating layer, which has a thickness smaller than that of the first electrically insulating layer,
   - an active semiconductor layer,

   the multilayer structure being characterized in that it comprises:
   - at least one FD-SOI region, in which the intermediate layer is a semiconductor layer,
   - at least one RF-SOI region, adjacent to the FD-SOI region, in which the intermediate layer is a third electrically insulating layer, said RF-SOI region comprising at least one radiofrequency component plumb with the third electrically insulating layer.

2. Structure according to Claim 1, wherein the sum of the thicknesses of the first electrically insulating layer, of the second electrically insulating layer, and of the third electrically insulating layer is comprised between 50 nm and 1500 nm.

3. Structure according to Claim 1 or Claim 2, furthermore comprising a charge-trapping layer arranged between the carrier substrate and the first electrically insulating layer.

4. Structure according to Claim 3, wherein the charge-trapping layer is made of polysilicon or of porous silicon.

5. Structure according to one of Claims 1 to 4, wherein the intermediate semiconductor layer is made of crystalline or polycrystalline material.

6. Structure according to one of Claims 1 to 4, wherein the intermediate semiconductor layer is made of amorphous material.

7. Structure according to one of the preceding claims, wherein the first electrically insulating layer is a layer of silicon oxide.

8. Structure according to one of the preceding claims, wherein the second electrically insulating layer is a layer of silicon oxide.

9. Structure according to one of the preceding claims, wherein the third electrically insulating layer is a layer of silicon oxide.

10. Structure according to one of the preceding claims, wherein the first electrically insulating layer has a thickness comprised between 20 nm and 1000 nm.

11. Structure according to one of the preceding claims, wherein the second electrically insulating layer has a thickness comprised between 10 nm and 100 nm.

12. Structure according to one of the preceding claims, wherein the active semiconductor layer has a thickness comprised between 3 nm and 30 nm.

13. Process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:
    - providing a first donor substrate,
    - forming a weakened zone in said first donor substrate, so as to delineate an intermediate first semiconductor layer,
    - transferring said intermediate first semiconductor layer to a semiconductor carrier substrate, a first electrically insulating layer being at the interface between the donor substrate and the carrier substrate so as to form an intermediate structure comprising the carrier substrate, the first electrically insulating layer and the transferred intermediate first semiconductor layer,
    - locally removing one segment of the intermediate first semiconductor layer down to the first electrically insulating layer in order to form a cavity,
    - depositing an electrically insulating layer, called the third electrically insulating layer, in the cavity,
    - providing a second donor substrate,
    - forming a weakened zone in said second donor substrate, so as to delineate an active second semiconductor layer,
    - transferring said active second semiconductor layer to the intermediate structure, a second electrically insulating layer being at the interface between the second donor substrate and the intermediate structure,
    - producing:
        - at least one digital component in the active second semiconductor layer plumb with the intermediate first semiconductor layer, in order to form an FD-SOI region, and

- at least one radiofrequency component plumb with the third electrically insulating layer, in order to form an RF-SOI region.

14. Process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:
    - forming an intermediate structure by depositing an intermediate first semiconductor layer on a carrier substrate covered with a first electrically insulating layer,
    - locally removing one segment of the intermediate first semiconductor layer down to the first electrically insulating layer in order to form a cavity,
    - depositing an electrically insulating layer, called the third electrically insulating layer, in the cavity,
    - providing a donor substrate,
    - forming a weakened zone in said donor substrate, so as to delineate an active second semiconductor layer,
    - transferring said active second semiconductor layer to the intermediate structure, a second electrically insulating layer being at the interface between the donor substrate and the intermediate structure,
    - producing:
        - at least one digital component in the active second semiconductor layer plumb with the intermediate first semiconductor layer, in order to form an FD-SOI region, and
        - at least one radiofrequency component plumb with the third electrically insulating layer, in order to form an RF-SOI region.

15. Process according to Claim 13 or Claim 14, wherein the local removal of a segment of the intermediate first semiconductor layer and the deposition of a third electrically insulating layer in the cavity are carried out after the transfer of the active second semiconductor layer to the intermediate structure.

16. Process according to one of Claims 13 to 15, furthermore comprising forming a charge-trapping layer on the carrier substrate, said charge-trapping layer being arranged between the carrier substrate and the first electrically insulating layer.

17. Process according to one of Claims 13 to 15, wherein the local removal comprises depositing a mask by lithography and etching the intermediate first semiconductor layer through at least one aperture of said mask.

18. Process according to one of Claims 13 to 15, furthermore comprising, before the transfer of said active second semiconductor layer to the intermediate structure,

treating the free surfaces of the intermediate first semiconductor layer and the third electrically insulating layer in order to decrease the roughness thereof.