

ABSTRACT

Embodiments of the disclosure relate to the technical field of semiconductors, in particular to a semiconductor layout structure and a semiconductor test structure. The semiconductor layout structure includes: active layers, each active layer including a first active area and a second active area arranged adjacent to the first active area, the first active area including first transistor areas spaced apart from each other, the second active area including second transistor areas spaced apart from each other, and the active layers corresponding to the first transistor areas adjacent to each other being separated from each other; and gate layers, each gate layer being arranged above a respective active layer, and including at least one first gate structure extending along a first direction, and second gate structures spaced apart from each other in the first direction, and the at least one first gate structure and the second gate structures being arranged adjacent to each other, the at least one first gate structure corresponding to the first transistor areas, and each second gate structure corresponding to a second transistor area.