ABSTRACT

INTEGRATED CIRCUIT SYSTEM EMPLOYING STRESS-ENGINEERED SPACERS

An integrated circuit system that includes: providing a substrate including a first region with a first device and a second device and a second region with a resistance device; configuring the first device, the second device, and the resistance device to include a first spacer and a second spacer; forming a stress inducing layer over the first region and the second region; processing at least a portion of the stress inducing layer formed over the first region to alter the stress within the stress inducing layer; and forming a third spacer adjacent the second spacer of the first device and the second device from the stress inducing layer.

Fig 16