

METAL DEPOSITION

BACKGROUND OF THE INVENTION

Field of the Invention

[01] This invention relates to the field of current-carrying devices and components. In particular, the invention relates to a current-carrying device in concert with a voltage switchable dielectric material.

Description of the Related Art

[02] Current-carrying structures are generally fabricated by subjecting a substrate to a series of manufacturing steps. Examples of such current-carrying structures include printed circuit boards, printed wiring boards, backplanes, and other micro-electronic types of circuitry. The substrate is typically a rigid, insulative material such as epoxy-impregnated glass fiber laminate. A conductive material, such as copper, is patterned to define conductors, including ground and power planes.

[03] Some prior art current-carrying devices are manufactured by layering a conductive material over a substrate. A mask layer is deposited on the conductive layer, exposed, and developed. The resulting pattern exposes select regions where conductive material is to be removed from the substrate. The conductive layer is removed from the select regions by etching. The

mask layer is subsequently removed, leaving a patterned layer of the conductive material on the surface of the substrate. In other prior art processes, an electroless process is used to deposit conductive lines and pads on a substrate. A plating solution is applied to enable conductive material to adhere to the substrate on selected portions of the substrate to form patterns of conductive lines and pads.

[04] To maximize available circuitry in a limited footprint, substrate devices sometimes employ multiple substrates, or use both surfaces of one substrate to include componentry and circuitry. The result in either case is that multiple substrate surfaces in one device need to be interconnected to establish electrical communication between components on different substrate surfaces. In some devices, sleeves or vias provided with conductive layering extend through the substrate to connect the multiple surfaces. In multi-substrate devices, such vias extend through at least one substrate to interconnect one surface of that substrate to a surface of another substrate. In this way, an electrical link is established between electrical components and circuitry on two surfaces of the same substrate, or on surfaces of different substrates.

[05] In some processes, via surfaces are plated by first depositing a seed layer of a conductive material followed by an electrolytic process. In other processes, adhesives are used to attach conductive material to via surfaces. In

these devices, the bond between the vias and conductive material is mechanical in nature.

[06] Certain materials, referred to below as voltage switchable dielectric materials, have been used in prior art devices to provide over-voltage protection. Because of their electrical resistance properties, these materials are used to dissipate voltage surges from, for example, lightning, static discharge, or power surges. Accordingly, voltage switchable dielectric materials are included in some devices, such as printed circuit boards. In these devices, a voltage switchable dielectric material is inserted between conductive elements and the substrate to provide over-voltage protection.

SUMMARY

[07] Various embodiments include a method for fabricating a current-carrying formation. Several embodiments address fabricating formations on or with a Voltage Switchable Dielectric Material (VSDM). A VSDM may include a characteristic voltage, whose magnitude defines a threshold below which the VSDM is substantially electrically insulative, and above which the VSDM is substantially electrically conductive.

[08] A method may include providing a conductive backplane, forming a layer of VSDM on at least a portion of the conductive backplane, and depositing an electrically conductive material on at least a portion of the voltage switchable dielectric material. A conductive backplane may include a metal, a conductive compound, a polymer and/or other materials. In some cases, a conductive backplane may include a substrate. In certain embodiments, a conductive backplane may also act as a substrate. In some cases, a substrate may be removed after deposition.

[09] Deposition may include electrochemical deposition, and may include creating a voltage greater than a characteristic voltage associated with the VSDM, causing current to flow and deposition and/or etching to occur.

[010] In certain embodiments, a package (*e.g.*, a polymer) may be attached to a VSDM and/or associated current-carrying formations. In some cases, components (*e.g.*, a substrate) may be removed after attaching a package.

Removal may be facilitated by a decohesion layer disposed between two materials whose separability be desired.

[011] In some embodiments, a method comprises providing a VSDM, depositing an intermediate layer on at least a portion of the VSDM, and depositing a material on at least a portion of the intermediate layer. An intermediate layer may improve adherence, mechanical properties, electrical properties, and the like. An intermediate layer may provide for a controlled release or decohesion. An intermediate layer may include a diffusion barrier. In some cases, an intermediate layer is deposited on a VSDM, and an additional material (*e.g.*, a polymer and/or electrical conductor) is deposited on at least a portion of the intermediate layer. An insulating material (*e.g.*, a polymer) may be deposited on an intermediate layer. A conductor may be deposited on an intermediate layer. An intermediate layer may be formed using electrografting.

[012] In some embodiments, a method comprises providing a substrate having a VSDM and depositing a current-carrying material on at least a portion of the VSDM. A package may be attached to at least a portion of the VSDM and/or at least a portion of the current-carrying formation. A package may include a polymer. A package and/or a VSDM may include one or more vias, which may be filled. Certain embodiments include a plurality of electrical connections through a package.

[013] In some embodiments, a method includes applying a contact mask to a surface of a VSDM. A contact mask may be removably attached such that it seals or otherwise blocks a first portion of the VSDM from deposition, and exposes a second portion of the VSDM for deposition of a material (*e.g.*, a current-carrying formation).

[014] A contact mask may include an insulating foot that contacts a surface of the VSDM and demarcates or defines one or more portions. A contact mask may also include an electrode, typically separated from the surface by the insulating foot. In some embodiments, a sandwich of the VSDM and contact mask may be immersed in (or otherwise exposed to) a solution that provides a source of ions associated with a desired material to be deposited. A voltage greater than the characteristic voltage of the VSDM may be created, that causes deposition of the desired material in or on the exposed portions of the VSDM.

[015] In some embodiments, a conductor deposited on a VSDM may be etched, typically using a mask, in a fashion that removes the conductor from certain regions of the VSDM. The unetched regions may form current-carrying formations according to certain embodiments.

[016] A VSDM may include regions having different characteristic voltages. Certain embodiments include a VSDM having first and second regions. A first region may have a first characteristic voltage, and a second region may have a second characteristic voltage. According to different processing

conditions, a material may be deposited on either of the first and second regions, or both regions. In some cases, deposition on both regions may be followed by a preferential etching of the deposited material from one region, but not the other region. In some embodiments, current-carrying formations are formed on different regions independently of each other.

[017] Any structural limitation described herein may be combined with another structural limitation provided they are not mutually exclusive. Any step described herei may be combined with another step provided they are not mutually exclusive.

BRIEF DESCRIPTION OF FIGURES

- [018] FIG. 1 illustrates a single-sided substrate device including a voltage switchable dielectric material, under an embodiment of the invention.
- [019] FIG. 2 illustrates electrical resistance characteristics of a voltage switchable dielectric material, under an embodiment of the invention.
- [020] FIGs. 3A-3F show a flow process for forming the device of FIG. 1.
- [021] FIG. 3A illustrates a step for forming a substrate of voltage switchable dielectric material.
- [022] FIG. 3B illustrates a step of depositing a non-conductive layer on the substrate.
- [023] FIG. 3C illustrates a step of patterning a non-conductive layer on the substrate.
- [024] FIG. 3D illustrates a step of forming a conductive layer using the pattern of the non-conductive layer.
- [025] FIG. 3E illustrates a step of removing the non-conductive layer from the substrate.
- [026] FIG. 3F illustrates the step of polishing the conductive layer on the substrate.
- [027] FIG. 4 details a process for electroplating current-carrying structures on a substrate formed from voltage switchable dielectric material, under an embodiment of the invention.

[028] FIG. 5 illustrates a dual-sided substrate device formed from voltage switchable dielectric material and including a via interconnecting current-carrying formations on both sides of the substrate, under an embodiment of the invention.

[029] FIG. 6 illustrates a flow process for forming the device of FIG. 5.

[030] FIG. 7 illustrates a multi-layered substrate device including substrates formed from voltage switchable dielectric material, under an embodiment of the invention.

[031] FIG. 8 illustrates a process for forming the multi-substrate device of FIG. 7.

[032] FIG. 9 illustrates an exemplary waveform for a pulse plating process according to an embodiment of the invention.

[033] FIG. 10 illustrates an exemplary waveform for a reverse pulse plating process according to an embodiment of the invention.

[034] FIG. 11 illustrates a segment of an interior structure of a connector, the segment having exposed pin receptacles according to an embodiment of the invention.

[035] FIG. 12 shows a perspective view of a portion of the segment of FIG. 11 with a mask disposed thereon, according to an embodiment of the invention.

[036] FIG. 13 illustrates certain embodiments associated with intermediate layers.

[037] FIG. 14 illustrates an exemplary method and structure that incorporates a conductive backplane.

[038] FIG. 15 is a diagrammatic illustration of attaching a package, according to some embodiments.

[039] FIGS. 16A and 16B illustrate cross section and perspective views (respectively) of a removable contact mask, according to certain embodiments.

[040] FIG. 17 illustrates deposition of a current-carrying material to form a current-carrying formation, according to certain embodiments.

[041] FIG. 18 illustrates a current-carrying formation fabricated using an etching process, according to certain embodiments.

[042] FIG. 19 illustrates a voltage switchable dielectric material (VSDM) 1910 having regions with different characteristic voltages, according to certain embodiments.

[043] FIGS. 20A-C illustrate the deposition of one or more current-carrying formations, according to certain embodiments.

DETAILED DESCRIPTION

[044] Embodiments of the invention use a class of material, referred to herein as voltage switchable dielectric materials, to develop current-carrying elements on a structure or substrate. The electrical resistivity of a voltage switchable dielectric material can be varied between a non-conductive state and a conductive state by an applied voltage. Methods of the invention render the substrate or structure conductive by applying a voltage to the voltage switchable dielectric material, and then subjecting the substrate or structure to an electrochemical process. This process causes current-carrying material to be formed on the substrate. The current-carrying materials can be deposited on select regions of the substrate to form a patterned current-carrying layer. The applied voltage is then removed so that the substrate or structure returns to the non-conductive state after the current-carrying layer has been patterned. As will be further described, embodiments of the invention provide significant advantages over previous devices having current-carrying structures. Among other advantages, current-carrying material can be patterned onto the substrate with fewer steps, thus avoiding costly and time-consuming steps such as etching and electroless processes.

[045] Voltage switchable dielectric materials may also be used for dual-sided and multi-substrate devices having two or more substrate surfaces containing electrical components and circuitry. Vias in substrates formed from voltage switchable dielectric materials can interconnect electrical components and

circuitry on different substrate surfaces. A via can include any opening of a substrate or device that can be provided with a conductive layer for the purpose of electrically interconnecting two or more substrate surfaces. Vias include voids, openings, channels, slots, and sleeves that can be provided with a conductive layer to interconnect electrical components and circuitry on the different substrate surfaces. Under embodiments of the invention, plating a via can be accomplished during a relatively simple electrochemical process. For example, vias in a voltage switchable dielectric material substrate may be plated using an electrolytic process. The vias can also be formed concurrently during the electrolytic process used to pattern one or more conductive layers on a substrate surface or surfaces of the device.

[046] In an embodiment of the invention, a current-carrying structure is formed from a voltage switchable dielectric material. A current-carrying formation can be formed on one or more selected sections of a surface of the substrate. As used herein, "current carrying" refers to an ability to carry current in response to an applied voltage. Examples of current-carrying materials include magnetic and conductive materials. As used herein, "formed" includes causing the current-carrying formation to form through a process in which a current-carrying material is deposited in the presence of a current applied to the substrate. Accordingly, current-carrying material may be electrodeposited onto the surface of the substrate through processes such as electroplating, plasma deposition, vapor deposition, electrostatic processes,

or hybrids thereof. Other processes may also be used to form the current-carrying formation in the presence of an electrical current. The current-carrying formation may be incrementally formed so that a thickness of the current-carrying formation is developed by deposition of like material onto selected sections of the substrate.

[047] An electrobonding interface is formed between the current-carrying formation and the substrate. The electrobonding interface comprises an interface layer of electrobonds between the current-carrying formation and the substrate. The electrobonds are bonds formed between molecules of the substrate and molecules of the current-carrying material that are electrodeposited onto the substrate. The electrobonds form in regions of the substrate where additional current-carrying material is deposited to form the current-carrying formation.

[048] As electrobonds form between molecules, electrobonds exclude bonds formed as a result of electroless processes where molecules of the current-carrying material may be mechanically or otherwise added to the surface. Electro bonds exclude bonds formed in processes that include, for example, seeding conductive material onto the substrate using adhesives and other types of mechanical or chemical bonds. Examples of processes where current-carrying material may be electrodeposited to form electrobonds include electroplating, plasma deposition, vapor deposition, electrostatic processes, and hybrids thereof.

[049] A nonconductive layer may be patterned onto the surface of the substrate to define the selected sections of the substrate. The substrate is then subjected to an electrochemical process to incrementally form the current-carrying formation on the selected regions of the substrate. The non-conductive layer may comprise a resist layer that is removed once the current-carrying formation is formed on the select regions of the substrate. The non-conductive layer can also be formed from screened resist patterns, which can either be permanent or removable from the substrate.

[050] A voltage switchable dielectric material is a material that is non-conductive until a voltage is applied that exceeds a characteristic threshold voltage value. Above the characteristic threshold voltage value the material becomes conductive. Therefore, a voltage switchable dielectric material is switchable between a non-conductive state and a conductive state.

[051] An electrochemical process includes a process in which conductive elements are bonded to a voltage switchable dielectric material while the voltage switchable dielectric material is in the conductive state. An example of an electrochemical process is an electrolytic process. In an embodiment, an electrode is immersed in a fluid along with another material. A voltage is applied between the electrode and the other material to cause ions from the electrode to transfer and form on the other material.

[052] In one embodiment, a device includes a single-sided substrate formed from voltage switchable dielectric material. A non-conductive layer is

patterned onto the substrate to define regions on the surface of substrate.

Preferably, the substrate is subjected to an electrolytic process when the voltage switchable dielectric material is in a conductive state. The electrolytic process causes conductive material to incrementally form on the substrate in the regions defined by the pattern of the non-conductive layer. One advantage of this embodiment is that the current-carrying formation can be fabricated on the structure with a reduced thickness relative to previous substrate devices. Also, the patterned current-carrying formation can be formed without implementing some fabrication steps used with prior art structures, such as, for example, steps of etching, or multiple steps of masking, imaging, and developing resist layers.

[053] In another embodiment of the invention, a dual-sided substrate is formed to include vias to electrically connect components on both sides of the substrate. A patterned current-carrying layer is formed on each side of the substrate. One or more vias extend through the substrate. The substrate can be subjected to one or more electrochemical processes while in the conductive state, causing current-carrying material to be formed on selected sections of the substrate, including on surfaces defining the vias. The selected sections of the substrate can be defined by a non-conductive layer, patterned in a previous step.

[054] Several shortcomings exist in previous processes that plate or otherwise provide conductive layers to surfaces of vias. In previous processes

that deposit seed layers on surfaces of vias and then subject those surfaces to an electroplating process, the plating material bonds only to the particles that comprise the seed layer. Seeding conductive particles can be problematic and costly, since it requires additional manufacturing steps. Further, the continuity and dispersion of the particles along surfaces defining the vias is often imperfect. As such, a substantial risk exists that the continuity of the plating of a surface of a via is broken at some juncture.

[055] Other previous processes use adhesives to form mechanical bonds between surfaces, or between particles in the surface of a via and a conductive material. The mechanical bonds are relatively weak in comparison to electrochemical bonds formed on surfaces of the substrate. The mechanical nature of the bonds formed between the surface of the via and the conductive material make devices prone to failure. To compound problems with previous devices, a failed plated via is detrimental to the entire substrate device.

[056] Typically, vias are plated only after the substrate is provided with conductive elements on the substrate's surfaces. Failures in the plated vias may not be noticed or caused until at least some or all of the substrates in the device are assembled. If plating a via fails, re-plating the via is not feasible in the assembled device. Often, the entire device has to be discarded. Thus, one failed via in a device having several vias and substrates is enough to cause the entire device, including all of the fabricated substrates, to be discarded.

[057] Among other advantages of this embodiment, problematic methods for forming current-carrying formations on surfaces defining vias are avoided.

According to prior art methods that require a surface modification to be conductive, additional materials are required to prepare vias to bond with a conductive material because the surfaces of the vias are not otherwise conductive without these materials. Thus, additional materials are not needed in embodiments of the invention because the voltage switchable dielectric material forming the substrate can be made conductive during the electroplating process. As such, bonds formed between surfaces of vias and the current-carrying material are electrical attraction bonds formed during the electrochemical process. The bond, herein referred to as an electrochemical bond, is stronger than bonds formed by seeded particles or adhesives.

Moreover, the surfaces of the vias are uniform surfaces of a voltage switchable dielectric material. Thus, electrical continuity through the vias is ensured.

[058] In another embodiment of the invention, a multi-substrate device includes two or more substrates each formed from a voltage switchable dielectric material. Each substrate can be subjected to an electrochemical process to form a conductive layer. A pattern of each conductive layer is predetermined by patterning a non-conductive layer to define the pattern for the current-carrying formation. One or more vias may be used to electrically connect current-carrying formations on one or more of the substrates. Each

via may be formed when the respective substrates are subjected to the electrochemical process.

[059] Among other advantages provided by embodiments of the invention, multi-substrate devices use the conductive state of the voltage switchable dielectric material to plate vias interconnecting the different substrate surfaces. Therefore, current-carrying materials can be formed on vias during an electrolytic processes without having to alter the substrate in regions that define the vias. The resulting current-carrying layers formed in the vias significantly reduce the risk that the vias will fail to establish electrical contact between substrates. In contrast, prior art multi-substrate devices have been plagued by occasionally ineffective vias, which often resulted in the entire multi-substrate device having to be discarded.

[060] Another advantage provided to embodiments of the invention is that inclusion of a substrate formed from a voltage switchable dielectric material also provides voltage regulation protection to the device as a whole.

Numerous applications for embodiments of the invention exist.

Embodiments of the invention may be employed for use with, for example, substrate devices such as PCBs, surface mount components, pin connectors, smart cards, and magnetically layered materials.

A. Single Substrate Devices

[061] FIG. 1 is a cross-sectional view of a device incorporating a voltage switchable dielectric material, under an embodiment of the invention. In this embodiment, the voltage switchable dielectric material is used to form a substrate 10 of the device. The voltage switchable dielectric material is non-conductive but, as previously noted, can be switched to a conductive state by applying a voltage having a magnitude that exceeds a characteristic voltage of the material. Numerous examples of a voltage switchable dielectric material have been developed, including those described below with reference to FIG.

2. Applications in which current-carrying substrates are used include, for example, printed circuit boards (PCBs), printed wiring boards, semiconductor wafers, flex circuit boards, backplanes, and integrated circuit devices. Specific applications of integrated circuits include devices having computer processors, computer readable memory devices, motherboards, and PCBs.

[062] The voltage switchable dielectric material in the substrate 10 allows for the fabrication of a patterned current-carrying formation 30. The current-carrying formation 30 is a combination of individual current-carrying elements 35 formed onto the substrate 10 according to a predetermined pattern. The current-carrying formation 30 includes conductive materials. The current-carrying formation 30 is formed from precursors deposited on the substrate 10 during an electrochemical process in which the voltage switchable dielectric material is rendered conductive by an applied voltage

(see FIG. 2). In an embodiment, the precursors are ions deposited from an electrode into a solution. The substrate 10 is exposed to the solution while the voltage switchable dielectric material is maintained in the conductive state.

[063] The precursors selectively deposit on the substrate 10 according to a predetermined pattern. The predetermined pattern is formed by patterning a non-conductive layer 20 such as a resist layer (see FIGS. 3B-3D). When the voltage switchable dielectric material is in the conductive state, the precursors deposit only on the exposed regions of the substrate 10. The voltage switchable dielectric material in the conductive state can form electrochemical bonds with the precursors in the exposed sections of the substrate 10. In an embodiment, the non-conductive layer 20 (FIGS. 3B-3D) is formed from a resist layer deposited over the substrate 10. The resist layer is then masked and exposed to create the pattern, as is well known.

[064] FIG. 2 illustrates the resistive properties of voltage switchable dielectric materials as a function of applied voltage. The voltage switchable dielectric materials that can be used to form the substrate have a characteristic voltage value (V_c) specific to the type, concentration, and particle spacing of the material's formulation. A voltage (V_a) can be applied to the voltage switchable dielectric material to alter the electrical resistance properties of the material. If the magnitude of V_a ranges between 0 and V_c , the voltage switchable dielectric material has a high electrical resistance and is therefore non-conductive. If the magnitude of V_a exceeds V_c , the voltage switchable

dielectric material transforms into a low electrical resistance state in which it is conductive. As shown by FIG. 2, the electrical resistance of the substrate preferably switches sharply from high to low, so that the transformation between states is immediate.

[065] In an embodiment, V_c ranges between 1 and 100 volts to render the voltage switchable dielectric material conductive. Preferably, V_c is between 5 and 50 volts, using one of the compositions for voltage switchable dielectric material listed below. In some embodiments, a voltage switchable dielectric material is formed having a thickness such that the material switches from an insulating to conducting state at a voltage characterized in terms of a field (*e.g.*, a voltage across the thickness of the material). In some embodiments, a switching field may be between 10 and 1000 volts/mil. In some embodiments, a switching field may be between 50 and 300 volts/mil.

[066] In an embodiment, a voltage switchable material is formed from a mixture comprising conductive particles, filaments, or a powder dispersed in a layer including a non-conductive binding material and a binding agent. The conductive material may comprise the greatest proportion of the mixture. Other formulations that have the property of being non-conductive until a threshold voltage is applied are also intended to be included as voltage switchable dielectric material under embodiments of this invention.

[067] A specific example of a voltage switchable dielectric material is provided by a material formed from a 35% polymer binder, 0.5% cross linking

agent, and 64.5% conductive powder. The polymer binder includes Silastic 35U silicone rubber, the cross-linking agent includes Varox peroxide, and the conductive powder includes nickel with a 10 micron average particle size. Another formulation for a voltage switchable material includes 35% polymer binder, 1.0% cross linking agent, and 64.0% conductive powder where the polymer binder, the cross-linking agent, and the conductive powder are as described above.

[068] Other examples of conductive particles, powders, or filaments for use in a voltage switchable dielectric material can include aluminum, beryllium, iron, silver, platinum, lead, tin, bronze, brass, copper, bismuth, cobalt, magnesium, molybdenum, palladium, tantalum carbide, boron carbide, and other conductive materials known in the art that can be dispersed within a material such as a binding agent. The non-conductive binding material can include organic polymers, ceramics, refractory materials, waxes, oils, and glasses, as well as other materials known in the art that are capable of inter-particle spacing or particle suspension. Examples of voltage switchable dielectric material are provided in references such as U.S. Patent No. 4,977,357, U.S. Patent No. 5,068,634, U.S. Patent No. 5,099,380, U.S. Patent No. 5,142,263, U.S. Patent No. 5,189,387, U.S. Patent No. 5,248,517, U.S. Patent No. 5,807,509, WO 96/02924, and WO 97/26665, all of which are incorporated by reference herein. The present invention is intended to encompass

modifications, derivatives, and changes to any of the references listed above or below.

[069] Another example of a voltage switchable dielectric material is provided in U.S. Patent No. 3,685,026, incorporated by reference herein, which discloses finely divided conductive particles disposed in a resin material. Yet another example of voltage switchable dielectric material is provided in U.S. Patent No. 4,726,991, incorporated by reference herein, which discloses a matrix of separate particles of conductive materials and separate particles of a semiconductor material coated with an insulative material. Other references have previously incorporated voltage switchable dielectric materials into existing devices, such as disclosed in U.S. Patent No. 5,246,388 (connector) and U.S. Patent No. 4,928,199 (circuit protection device), both of which are incorporated by reference herein.

[070] FIGS. 3A-3F illustrate a flow process for forming a single layer current-carrying structure on a substrate as shown in FIG. 1, under an embodiment of the invention. The flow process exemplifies a process in which the electrical properties of a voltage switchable dielectric material are used to develop a current-carrying material according to a predetermined pattern.

[071] In FIG. 3A, a substrate 10 is provided that is formed from a voltage switchable dielectric material. The substrate 10 has dimensions, shape, composition and properties as necessary for a particular application. The composition of the voltage switchable dielectric material can be varied so that

the substrate is rigid or flexible, as required by the application. In addition, the voltage switchable dielectric material can be shaped for a given application. While some embodiments described herein disclose essentially planar substrates, other embodiments of the invention may employ a voltage switchable dielectric material that is molded or shaped into a non-planar substrate, such as for use with connectors and semiconductor components.

[072] In FIG. 3B, a non-conductive layer 20 is deposited over the substrate 10. The non-conductive layer 20 can be formed from a photoimageable material, such as a photoresist layer. Preferably, the non-conductive layer 20 is formed from a dry film resist. FIG. 3C shows that the non-conductive layer 20 is patterned on the substrate 10.

In an embodiment, a mask is applied over the non-conductive layer 20. The mask is used to expose a pattern of the substrate 10 through a positive photoresist. The pattern of the exposed substrate 10 corresponds to a pattern in which current-carrying elements will subsequently be formed on the substrate 10.

[073] FIG. 3D shows that the substrate 10 subjected to an electrolytic process while the voltage switchable dielectric material is maintained in a conductive state. The electrolytic process forms a current-carrying formation 30 that includes current-carrying elements 35. In an embodiment, the electroplating process deposits current-carrying elements 35 on the substrate 10 in gaps 14 in the non-conductive layer 20 created by masking and exposing the photoresist.

Additional details of the electrolytic process as employed under an embodiment of the invention are described with FIG. 4.

[074] In FIG. 3E, the non-conductive layer 20 is removed as necessary from the substrate 10. In an embodiment in which the non-conductive layer 20 includes photoresist, the photoresist may be stripped from the surface of the substrate 10 using a base solution, such as a potassium hydroxide (KOH) solution. Still, other embodiments may employ water to strip the resist layer. In FIG. 3F, the resulting conductive layer 30 patterned onto the substrate 10 may be polished. An embodiment employs chemical-mechanical polishing (CMP) means.

[075] FIG. 4 details the development of current-carrying elements on the substrate by use of an electroplating process. In a step 210, the electroplating process includes forming an electrolytic solution. The composition of the current-carrying elements depends on the composition of an electrode used to form the electrolytic solution. Accordingly, the composition of the electrode is selected according to factors such as cost, electrical resistance, and thermal properties. Depending on the application, for example, the electrode can be gold, silver, copper, tin, or aluminum. The electrode can be immersed in a solution including, for example, sulfate plating, pyrophosphate plating, and carbonate plating.

[076] In a step 220, a voltage that exceeds the characteristic voltage of the voltage switchable dielectric material is applied to the substrate 10 while the

substrate 10 is immersed in the electrolytic solution. The substrate 10 switches to a conductive state, such as is illustrated by FIG. 2. The applied voltage makes the substrate 10 conductive, causing precursors in the electrolytic solution to bind to the voltage switchable dielectric material.

[077] In a step 230, ions from the electrolytic solution bond to the substrate 10 in areas of the substrate 10 that are exposed by the non-conductive layer 20. In an embodiment, ions are precluded from bonding to regions where the photoresist has been exposed and developed. Therefore, the pattern of conductive material formed on the substrate 10 matches the positive mask used to pattern the non-conductive layer 20. Exposed regions of the substrate 10 attract and bond to the ions, in some embodiments, because the substrate is maintained at a voltage relative to the electrode so that the substrate, the electrode, and the electrolytic solution together comprise an electrolytic cell, as is well known in the art.

[078] Among advantages provided by an embodiment of the invention, current-carrying elements 35 are patterned onto the substrate 10 in a process requiring fewer steps than prior art processes. For example, in an embodiment, current-carrying elements 35 are deposited to form circuitry on the substrate 10 without etching, and therefore also without deposition of a buffer or masking layer for an etching step. In addition, embodiments of the invention allow for the current-carrying elements 35 to be formed directly on the substrate 10 instead of on a seed layer. This allows a vertical thickness of

the current-carrying elements 35 to be reduced relative to that in similar devices formed by other processes.

B. Devices Having Dual-Sided Substrates

[079] Certain devices include substrates that employ electrical components on two or more sides. The number of current-carrying elements that can be retained on a single substrate increases when two sides are used. As such, dual-sided substrates are often used when a high-density distribution of components is desired. Dual-sided substrates include, for example, PCBs, printed wiring boards, semiconductor wafers, flex circuits, backplanes, and integrated circuit devices. In such devices, vias or sleeves are typically used to interconnect both planar sides of the substrate. The vias or sleeves establish an electrical connection between the current-carrying elements on each planar side of the substrate.

[080] FIG. 5 displays an embodiment in which a device includes a dual-sided substrate 310 having one or more plated vias 350. The vias 350 extend from a first planar surface 312 of the substrate to a second planar surface 313 of the substrate. The first surface 312 includes a current-carrying formation 330 having a plurality of current-carrying elements 335. The second surface 313 includes a current-carrying formation 340 having a plurality of current-carrying elements 345. The current-carrying formations 330, 340 are fabricated on the respective sides 312, 313 of the substrate 310 by an

electrochemical process. In an embodiment, an electrolytic process is used to form a solution of precursors that are deposited on the respective first or second surface of the substrate when a voltage switchable dielectric material is in a conductive state. The precursors deposit on the substrate 310 according to a pattern of a pre-existing non-conductive layer on the respective first or second surface 312, 313.

[081] In an embodiment, a via 350 is formed in the substrate 310 before the substrate is subjected to the electrolytic process. Each side 312, 313 of the substrate 310 includes a patterned non-conductive layer (not shown). In an embodiment, the patterned non-conductive layers are photoresist layers that are patterned to expose select regions on the first and second side 312, 313 of the substrate 310. The via 350 is positioned so that a plated surface of the via 350 subsequently contacts one or more of the current-carrying elements 335, 345 on the first and second side 312, 313. During the electrolytic process, the via 350 is plated while current-carrying formations 330 and 340 are fabricated. In this way the via 350 is provided with a conductive sleeve or side-wall 355 to extend an electrical connection from one of the current-carrying elements 335 on the first surface 312 with one of the current-carrying elements 345 on the second side 313 of the substrate 310.

[082] FIG. 6 displays a flow process for developing a dual-sided substrate 310, according to an embodiment of the invention. In a step 410, the substrate 310 is formed from a voltage switchable dielectric material and provided with

dimensions, shape, properties, and characteristics necessary for a desired application. In a step 420, a non-conductive layer 320 is deposited over the first and second side 312, 313 of the substrate 310. In a step 430, the non-conductive layer 320 is patterned on the first side 312 of the substrate 310. Preferably, non-conductive material on at least the first side 312 of the substrate 310 is a photo-imageable material, such as a photoresist that is patterned using a positive mask. The positive mask allows select regions of the substrate 310 to be exposed through the non-conductive layer 320. In a step 440, the non-conductive layer 320 is patterned on the second side 313 of the substrate 310. In an embodiment, the non-conductive layer 320 on the second side 313 of the substrate 310 is similarly also a photoresist that is subsequently masked and exposed to form another pattern. The resulting pattern exposes the substrate 310 through the photoresist layer.

[083] In a step 450, one or more vias 350 are formed through the substrate 310. On each side 312, 313 of the substrate 310, the vias 350 intersect an uncovered portion of the substrate 310. The vias 350 are defined by side-walls formed through the substrate 310. In a step 460, the substrate 310 is subjected to one or more electrolytic processes to plate the first side 312, second side 313, and the side-walls of the vias 350. In an embodiment, in step 460 the substrate 310 is subjected to a single electrolytic process while an external voltage is applied to the voltage switchable dielectric material so that the substrate is in a conductive state. The conductive state of the substrate 310

causes ions in the electrolytic solution to bond to the substrate 310 in uncovered regions on the first and second surfaces 312, 313. The electrolytic fluid also moves through the vias 350 so that ions bond to the side-walls of the vias 350, forming conductive sleeves 355 that extend through the vias 350. The vias 350 intersect current-carrying elements on the first and second sides 312, 313 to electrically connect the current-carrying formation 330 on the first side 312 with the current-carrying formation 340 on the second side 313.

[084] The non-conductive layer 320 is removed as necessary from the substrate in a step 470. In an embodiment in which the non-conductive layer 320 includes photoresist, the photoresist may be stripped from the surface of the substrate 310 using a base solution, such as a KOH solution. In a step 480, the resulting current-carrying formation 330 and/or 340 is polished. In an embodiment, CMP is employed to polish the current-carrying formation 330.

[085] Several variations can be made to the embodiment described with reference to FIGs. 5 and 6. In one variation, a first non-conductive layer can be deposited on the first surface 312, and a second non-conductive layer can be deposited on the second surface 313 in a separate step. The first and second non-conductive layers can be formed from different materials, and can provide different functions other than enabling patterns to be formed for plating the substrate. For example, the first non-conductive material can be formed from a dry resist, while the second non-conductive material can be formed from a photo-imageable insulative material. While the dry resist is

stripped away after a current-carrying layer is formed on the first side 312, the photo-imageable insulative material is permanent and retained on the second surface 313.

[086] Additionally, different plating processes can be used to plate the first surface 312, the second surface 313, and the surface 355 of the vias 350. For example, the second surface 313 of the substrate 310 can be plated in a separate step from the first surface 312 to allow the first and second surfaces 312, 313 to be plated using different electrodes and/or electrolytic solutions. Since embodiments of the invention reduce steps necessary to form current-carrying layers, forming current-carrying layers 330 and 340 on the dual-sided substrate 310 is particularly advantageous. The use of different plating processes facilitates the fabrication of different materials for the current-carrying formations on opposite sides of the substrate 310. Different types of current-carrying material can be provided as simply as switching the electrolytic baths to include different precursors.

[087] As one example, a first side of a device such as a PCB is intended to be exposed to the environment, but the opposite side requires a high-grade conductor. In this example, a nickel pattern can be plated on the first side of the substrate, and a gold pattern can be plated on the second side of the substrate. This enables the PCB to have a more durable current-carrying material on the exposed side of the PCB.

[088] Any number of vias can be drilled, etched, or otherwise formed into the substrate. Vias can interconnect current-carrying elements, including electrical components or circuitry. Alternatively, a via can be used to ground a current-carrying element on one side of the substrate to a grounding element accessible from a second side of the substrate.

[089] Among advantages included with dual-sided substrates under an embodiment of the invention, precursors from the electrode form an electrochemical bond to the surfaces of the vias 350. The vias 350 are therefore securely plated, with minimal risks of a discontinuity that would interrupt electrical connection between the two sides of the substrate 310.

C. Devices Having Multi-Layered Substrates

[090] Some devices may include two or more substrates into one device. Stacking substrates enables the device to incorporate a high density of current-carrying elements, such as circuitry and electrical components, within a limited footprint. FIG. 7 illustrates a multi-substrate device 700. In the embodiment shown, the device 700 includes first, second and third substrates 710, 810, 910. Each substrate 710-910 is formed from a voltage switchable dielectric material. As with previous embodiments, the substrates 710-910 are non-conductive absent an applied voltage that exceeds the characteristic voltage of the voltage switchable dielectric material. While FIG. 7 illustrates an embodiment of three substrates, other embodiments may include more or fewer substrates. It will be appreciated that substrates may also be aligned in

different configurations other than being stacked, such as adjacent or orthanormal to one another.

[091] Each substrate 710, 810, 910 is provided with at least one current-carrying formation 730, 830, 930 respectively. Each current-carrying formation 730, 830, 930 is formed from a plurality of current-carrying elements 735, 835, 935 respectively. The current-carrying elements 735, 835, 935 are each formed when their respective substrates 710, 810, 910 are subjected to an electrochemical process while in a conductive state.

Preferably, the substrates 710, 810, 910 are mounted on one another after the respective current-carrying layers 735, 835, 935 are formed.

[092] The device 700 includes a first plated via 750 to electrically connect current-carrying elements 735 on the first substrate 710 to current-carrying elements 935 on the third substrate 910. The device 700 also includes a second plated via 850 to electrically connect current-carrying elements 835 on the second substrate 810 with current-carrying elements 935 on the third substrate 910. In this way, the current-carrying formations 730, 830, 930 of the device 700 are electrically interconnected. The arrangement of plated vias 750, 850 shown in the device 700 is only exemplary, as more or less vias can also be employed.

[093] For example, additional vias can be used to connect one of the current-carrying elements 735, 835, 935 to any other of the current-carrying elements on another substrate. Preferably, the first and second plated vias 750, 850 are

formed in the substrates 710, 810, 910 before the substrates 710, 810, 910 are individually plated. Thus, prior to plating, the plated vias 750, 850 are formed through the substrates 710, 810, 910 in predetermined positions so as to connect the current-carrying elements 735, 835, 935 of the different substrates as necessary. For the first plated via 750, openings are formed in the substrates 710, 810, 910 at the predetermined positions before any of the substrates are plated. Likewise, for the second plated via 850, openings are formed in the substrates 810, 910 at predetermined positions prior to those substrates being plated. The predetermined positions for the first and second plated via 750 and 850 correspond to uncovered regions on surfaces of the respective substrates in which current-carrying material will form. During subsequent electrolytic processes, precursors deposit in these uncovered regions of the substrates, as well as within the openings formed in each substrate to accommodate the vias 750, 850.

[094] For simplicity, details of device 700 will be described with reference to the first substrate 710. The first substrate 710 includes gaps 714 between the current-carrying elements 735. In an embodiment, gaps 714 are formed by masking a photoresist layer and then removing remaining photoresist after the current-carrying elements 735 are fabricated on the substrate 710. Similar processes are used to form second and third substrates 810, 910. The first substrate 710 is mounted over the current-carrying formation 830 of the second substrate 810. As with the first substrate 710, the second substrate 810

is mounted directly over the current-carrying formation 930 of the third substrate 910.

[095] In a variation to embodiments described above, one or more substrates in the device 700 may be dual-sided. For example, the third substrate 910 may be dual-sided, since the location of the third substrate 910 at the bottom of the device 700 readily enables the third substrate to incorporate a double-sided construction. Therefore, the device 700 may include more current-carrying formations than substrates to maximize the density of componentry and/or minimize the overall footprint of the device.

[096] The composition of the substrates 710, 810, 910, as well as the particular current-carrying material used for each substrate, may vary from substrate to substrate. Thus, for example, the current-carrying formation of the first substrate 710 may be formed from nickel, while the current-carrying formation 830 of the second substrate 810 is formed from gold.

[097] FIG. 8 illustrates a flow process for developing a device having multi-layered substrates, such as the device 700, where two or more of the substrates are formed from a voltage switchable dielectric material. The device can be formed from a combination of single and/or double-sided substrates. In an embodiment, the multi-substrate device 700 comprises separately formed substrates having current-carrying formations. With reference to device 700, in a step 610, the first substrate 710 is formed from a voltage switchable dielectric material. In a step 620, a first non-conductive

layer is deposited over the first substrate 710. As with previously described embodiments, the first non-conductive layer can be, for example, a photo-imageable material such as a photoresist layer. In a step 630, the first non-conductive layer is patterned to form selected regions in which the substrate 710 is exposed. In an embodiment, a photoresist layer is masked and then exposed to form the pattern, so that the substrate is exposed according to the pattern of the positive mask.

[098] In a step 640, the first via 750 is formed in the substrate 710. The first via 750 is preferably formed by etching a hole in the substrate 710. Additional vias can be formed as needed in the substrate 710. The via 750 is etched in a location on the substrate that is predetermined to be where select current-carrying elements 735 will be located to connect to current-carrying elements of other substrates in the device 700. In a step 650, the first substrate 710 is subjected to an electrolytic process. The electrolytic process employs an electrode and a solution according to design requirements for the first substrate 710. Components of the electrolytic process, including the electrode and the composition of the electrolytic solution, are selected to provide the desired precursors, i.e. materials forming the conductive layer 730. In a step 660, the remaining non-conductive layer on the first substrate 710 is removed. The current-carrying elements 735 on the first substrate 710 may then be polished in a step 670, preferably using CMP.

[0099] Once the first substrate 710 is formed, additional substrates 810, 910 can be formed in step 680 to complete the multi-substrate device 700. Subsequent substrates 810, 910 are formed using a combination of the steps 610-670. One or more additional vias, such as the second via 850, may be formed in another substrate as described according to steps 640 and 650. The device 700 may include additional substrates formed as described in steps 610-680, or as described for double-sided substrates above.

[0100] Variations may be made to each of the substrates 710, 810 as needed. For example, substrates used in the device can have voltage switchable dielectric materials with different compositions. Accordingly, the external voltage applied to each substrate to overcome the characteristic voltage can vary between substrates. Materials used for the non-conductive layers can also be varied from substrate to substrate. Additionally, the non-conductive layers can be patterned with, for example, different masking, imaging, and/or resist development techniques. Further, the materials used to develop current-carrying elements on the surfaces of the substrates can also be varied from substrate to substrate. For instance, the electrodes used to plate each substrate can be altered or changed for the different substrates, depending on the particular design parameters for the substrates.

[0101] Under a variation, it can be preferable for the process to include the construction of at least one double-sided substrate, such as at an end of the stack of substrates. The third substrate 910, for example, can be formed to

include current-carrying elements 935 on both planar sides. In this variation, a non-conductive layer is deposited on the first side and the second side of the third substrate 910. The non-conductive layer on the second side can be made of the same material as the non-conductive layer on the first side, although in some applications the second side of the substrate may require a different type of photo-imageable material or other non-conductive surface. The non-conductive layers on each side of the third substrate 910 are then individually patterned. The third substrate 910 is uncovered on the first and second sides when the respective non-conductive layers are patterned. Exposed regions on each side of the substrate may be plated together or in separate plating steps.

[0102] Embodiments such as shown above can be used in PCB devices. PCBs have a variety of sizes and applications, such as for example, for use as printed wiring boards, motherboards, and printed circuit cards. In general, a high density of current-carrying elements, such as electrical components, leads, and circuitry, are embedded or otherwise included with PCBs. In multi-substrate devices, the size and function of the PCBs can be varied. A device including a PCB under an embodiment of the invention has a substrate formed from a voltage switchable dielectric material. A photoresist such as a dry film resist can be applied over the substrate. An example of a commercially available dry film resist includes Dialon FRA305, manufactured by Mitsubishi Rayon Co. The thickness of the dry film resist deposited on the

substrate is sufficient to allow the substrate to become exposed at selected portions corresponding to where the resist was exposed by the mask.

[0103] An electroplating process such as described with respect to FIG. 3 is used to plate conductive materials on exposed regions of the substrate.

Substrates formed from a voltage switchable dielectric material can be used for various applications. The voltage switchable dielectric material can be formed, shaped, and sized as needed for the various printed circuit board applications. Examples of printed circuit boards include, for example, (i) motherboards for mounting and interconnecting computer components; (ii) printed wiring boards; and (iii) personal computer (PC) cards and similar devices.

[0104] Further variations of the basic process are described below.

1. Pulse Plating Process

[0105] An embodiment of the invention employs a pulse plating process. In this process, an electrode and a substrate comprising a voltage switchable dielectric material are immersed in an electrolytic solution. A voltage is applied between the electrode and the substrate so that the voltage switchable dielectric material becomes conductive. The applied voltage also causes ions in the electrolytic solution to deposit onto exposed areas of the substrate, thereby plating a current-carrying formation. In the pulse plating process, the voltage is modulated and follows a waveform such as the exemplary

waveform 900 shown in FIG. 9. The waveform 900 resembles a square-wave, but further includes a leading edge spike 910. The leading edge spike 910 is preferably a very short duration voltage spike sufficient to overcome a trigger voltage, V_t , of the voltage switchable dielectric material, where the trigger voltage is a threshold voltage that must be exceeded in order for the voltage switchable dielectric material to enter the conductive state. In some embodiments, the trigger voltage is relatively large, such as between 100 and 400 volts.

[0106] Once the trigger voltage has been exceeded and the voltage switchable dielectric material is in the conductive state, the voltage switchable dielectric material will remain in the conductive state for as long as the voltage applied to the voltage switchable dielectric material remains above a lower clamping voltage, V_c . In the waveform 900 of FIG. 9, it will be appreciated that the leading edge spike 910 is followed by a plateau 920 at a voltage above the clamping voltage. The plateau 920 is followed by a relaxation period in which the voltage returns to a baseline 930, such as 0 volts, then the cycle repeats.

2. Reverse Pulse Plating Process

[0107] Another embodiment of the invention employs a reverse pulse plating process. This process is essentially the same as the pulse plating process described above, except that in place of the plateau 920 (FIG. 9) the polarity of the voltage is reversed so that plating occurs at the electrode instead of the

substrate. An exemplary waveform 1000 is shown in FIG. 10 in which the positive and negative portions have essentially the same magnitude but opposite polarity. The shape of the negative portion need not match that of the positive portion in either magnitude or duration, and in some embodiments the negative portion of the waveform 1000 does not include a leading edge voltage spike. An advantage to reverse pulse plating is that it produces smoother plating results. When the voltage is reversed, those areas on the plating surface where plating occurred most rapidly before the reversal become those areas where dissolution occurs most readily. Accordingly, irregularities in the plating tend to smooth out over time.

3. Depositing and Patterning Non-Conductive Layers

[0108] Another embodiment of the invention employs a silk-screening method to develop a patterned non-conductive layer on a substrate formed from a voltage switchable dielectric material. This embodiment avoids the use of materials such as photoresist to develop the pattern for depositing current-carrying materials on the substrate. In a silk screening process, a robotic dispenser applies a dielectric material to the surface of the substrate according to a preprogrammed pattern. The silkscreen liquid applicant is typically a form of plastic or resin, such as Kapton. In contrast to other embodiments using photoresist materials for the non-conductive layer, silk-screened Kapton, or another plastic or resin, is permanently applied to the

surface of the substrate. As such, silk-screening offers advantages of combining steps for depositing and patterning non-conductive material on the substrate, as well as eliminating steps for removing non-conductive material from the surface of the substrate.

4. Multiple Types of Conductive Materials on a Single Surface

[0109] In addition, current-carrying elements may be fabricated onto a surface of a substrate from two or more types of current-carrying materials. The substrate including the voltage switchable dielectric material is adaptable to be plated by several kinds of current-carrying materials. For example, two or more electrolytic processes can be applied to a surface of the substrate to develop different types of current-carrying particles. In one embodiment, a first electrolytic process is employed to deposit a first conductive material in a first pattern formed on the surface of the substrate. Subsequently, a second non-conductive layer is patterned on the substrate including the first conductive material. A second electrolytic process may then be employed to deposit a second conductive material using the second pattern. In this way, a substrate may include multiple types of conductive material. For example, copper can be deposited to form leads on the substrate and another conductive material, such as gold, can be deposited elsewhere on the same surface where superior conduction is necessary.

E. Other Applications for Embodiments of the Invention

[0110] Embodiments of the invention include various devices with a substrate of a voltage switchable dielectric material upon which a current-carrying formation has been deposited. The current-carrying formation can comprise circuits, leads, electrical components, and magnetic material. Exemplary applications for embodiments of the invention are described or listed below. The applications described or listed herein are merely illustrative of the diversity and flexibility of this invention, and should therefore not be construed as an exhaustive list.

1. Pin Connectors

[0111] In an embodiment, a pin connector is provided. For example, the voltage switchable dielectric material is used to form an interior structure of a female pin connector. The voltage switchable dielectric material can be used to form contact leads within the interior structure of the female pin connector. The voltage switchable dielectric material may be shaped into the interior structure using, for example, a mold that receives the voltage switchable dielectric material in a liquid form. The resulting interior structure includes a mating surface that opposes a corresponding male pin connector when the two connectors are mated. Pin receptacles are accessible through holes in the mating surface. The holes and pin receptacles correspond to where pins from the male connector will be received.

[0112] To provide conductive contact elements within the connector, and as shown in FIG. 11, the interior structure may be separated into segments 1100 to expose the lengths of the pin receptacles 1110 that extend to the holes in the mating surface 1120. A non-conductive layer 1200, shown in FIG. 12, such as a photoresist layer may be deposited on one of the segments 1100. The non-conductive layer 1200 may then be patterned so that a bottom surface 1210 of each pin receptacle 1110 is exposed through the non-conductive layer 1200. One or both segments 1100 of the interior structure may then be subjected to an electrolytic plating process. During the plating process, a voltage is applied to the interior structure so that the voltage switchable dielectric material is conductive. A conductive material is then plated on the bottom surface 1210 of each pin receptacle 1110 in the interior structure. Once the contact leads are formed in the pin receptacles 1110, the non-conductive layer 1200 can be removed and the segments 1100 rejoined. The interior structure may also be housed within a shell to complete the female pin connector.

[0113] Several advantages exist to forming a pin connector under an embodiment of the invention. Plating the interior structure enables a large number of pin receptacles to be included in the interior structure in one plating process. Further, because the lead contacts can be made thinner, pin receptacles can be formed closer together to reduce dimensions of the pin connector. The pin connector can also provide over-voltage protection properties that are inherent to voltage switchable dielectric materials.

2. Surface Mount Packages

[0114] Surface mount packages mount electronic components to a surface of a printed circuit board. Surface mount packages house, for example, resistors, capacitors, diodes, transistors, and integrated circuit devices (processors, DRAM etc.). The packages include leads directed internally or outwardly to connect to the electrical component being housed. Specific examples of surface mounted semiconductor packages include small outline packages, quad flat packages, plastic leaded chip carriers, and chip carrier sockets.

[0115] Manufacturing surface mount packages involves forming a frame for the leads of the package. The frame is molded using a material such as epoxy resin. Thereafter, leads are electroplated into the molded frame. In an embodiment of the invention, a voltage switchable dielectric material can be used to form the frame. A non-conductive layer is formed on the frame to define the locations of the leads. The non-conductive layer can be formed during the molding process, during a subsequent molding process, or through a masking process using a photo-imageable material such as described above. A voltage is applied to the frame during the electroplating process to rendering the frame conductive. The leads form on the frame in locations defined by a pattern of the non-conductive layer.

[0116] By using a voltage switchable dielectric material, leads can be made thinner or smaller, allowing for a smaller package that occupies a smaller

footprint on the PCB. The voltage switchable dielectric material also inherently provides over-voltage protection to protect contents of the package from voltage spikes.

[0117] FIG. 13 illustrates certain embodiments associated with intermediate layers. In some applications, it may be advantageous to incorporate one or more layers between a VSDM and a current-carrying material in a current-carrying formation. These layers may have appreciable thickness (*e.g.*, greater than tens of nm, a few microns, tens of microns, or even tens of mm), or may be as thin as monolayers (*e.g.*, having a thickness of the order of an atom, a few atoms, or a molecule). For the purposes of this specification, such layers are termed intermediate layers.

[0118] FIG. 13 includes a diagrammatic representation of exemplary processing steps (left side) and corresponding structures (right side) associated with the use of intermediate layers according to some embodiments. In step 1300, a VSDM 1302 is provided. In some cases, the VSDM may be provided as a layer or coating on a substrate 1304. A VSDM may have a characteristic voltage, above which the VSDM becomes conductive. In some embodiments, the characteristic voltage of a VSDM is above a typical “use” voltage associated with an electronic device (*e.g.*, above 3 Volts, 5 Volts, 12 Volts, or 24 Volts). In some embodiments, the characteristic voltage of a VSDM is above a typical voltage used for electroplating a material (*e.g.*, above 0.5 volts, 1.5 volts, or 2.5 volts). In some

cases, electroplating may require a voltage that is both above a typical plating voltage and above the characteristic voltage.

[0119] In step 1310, VSDM 1302 may be masked using mask 1312, although masking may not be required for certain applications. Typically, mask 1312 defines an exposed portion 1314 of the VSDM upon which a current-carrying formation will be formed, and a “masked” region (*e.g.*, beneath the mask) upon which a current-carrying material is not deposited. In the example shown in FIG. 13, mask 1312 defines an exposed portion 1314 of VSDM 1302 upon which a current-carrying formation may be fabricated.

[0120] In step 1320, an intermediate layer 1322 may be deposited on at least part of the exposed portion 1314. Intermediate layer 1322 may be sufficiently thick that certain desirable properties are manifest (*e.g.*, adherence, diffusion blocking, improved electrical properties and the like). In some cases, an intermediate layer may be used to attach a polymer to VSDM 1302. In some cases, an intermediate layer may be sufficiently thin and/or conductive that subsequent deposition of a current-carrying material on intermediate layer 1322 may be performed. Intermediate layer 1322 may form an insulating barrier, and in some cases, may provide for conductivity via tunneling and/or other nonlinear effects.

[0121] In step 1330, a current-carrying material 1332 may be deposited on the intermediate layer. In some embodiments, mask 1312 may be removed after formation of the current-carrying formation. In the example described in FIG.

13, step 1340 illustrates the removal of mask 1312, yielding a current-carrying formation 1342 comprising a current-carrying material and an intermediate layer.

[0122] An intermediate layer may include a diffusion barrier to reduce or prevent diffusion between a current-carrying material (*e.g.*, Cu) and a VSDM material. Exemplary diffusion barriers include metals, nitrides, carbides, silicides, and in some cases combinations thereof. Exemplary diffusion barriers include TiN, TaN, Ta, W, WN, SiC, Si₃N₄, TaTiN, SiON, Re, MoSi₂, TiSiN, WCN, composites thereof, and other materials.

[0123] An intermediate layer may be electrically conductive. For very thin intermediate layers (*e.g.*, less than 100nm, 50nm, or even less than 10nm), even relatively resistive materials may provide for sufficient current densities that electrical current may flow from the depositing current-carrying material to the VSDM phase. An intermediate layer may be a conductive polymer, such as certain doped polythiophenes and/or polyanilines.

[0124] Intermediate layers may be fabricated using line-of sight deposition, physical vapor deposition, chemical vapor deposition, electrodeposition, spin coating, spraying, and other methods.

[0125] Various embodiments include electrodeposition of current-carrying materials. In some embodiments, a VSDM (optionally including an intermediate layer) is immersed in a plating solution, after which a plating bias is created to cause electroplating of a current-carrying material. In some

cases, the plated VSDM is removed from the plating bath while still subject to the plating bias. Electrodeposition may include imposing electrical currents between 0.1 and 10 milliamps/square cm. An exemplary plating solution may include copper ions at a concentration between 0.4 and 100mM, a copper complexing agent such as [ethylamine, pyridine, pyrrolidine, hydroxyethyldiethylamine, aromatic amines, and nitrogen heterocycles] having a molar ratio between 0.1 and 2 and a pH between 3 and 7. Some embodiments may use procedures and materials as described in U.S. patent publication numbers 2007/0062817 A1 and 2007/0272560 A1, the disclosures of which are incorporated by reference herein.

[0126] Certain embodiments include electrografting one or more layers, as described, for example, in U.S. patent application publication number 2005/0255631 A1, the disclosure of which is incorporated by reference herein.

In some embodiments, depositing an intermediate layer may include electrografting the intermediate layer. Embodiments comprising electrografting may be used to deposit insulating layers (*e.g.*, insulating polymers) on a VSDM material by incorporating an electrografted intermediate layer. Electrografting may be described as the electrochemical bonding (*e.g.*, electrobonding) of a polymer, and may include immersing a VSDM in a solution having a dissolved organic precursor. Application of an appropriate voltage (including a voltage profile) may cause the VSDM to conduct electrons, which may result in an electrochemical deposition of the

dissolved polymer onto the surface of the VSDM. As such, a polymer may be electrobonded to the VSDM.

[0127] An exemplary electrografting embodiment may include immersing the VSDM in a solution comprising an organic precursor. An exemplary solution may include butylmethacrylate in a solution comprising $5\text{E-}2$ mol/L of tetraethylammonium perchlorate in DMF, in an amount of 5 mol of butylmethacrylate/L of solution. The VSDM may be the working electrode, with a Pt counterelectrode, and Ag reference electrode. The immersed VSDM may be subject to a voltage profile sufficient to cause the VSDM to conduct (*e.g.*, cyclic voltage between -0.1 and -2.6 V/(Ag+/Ag), and cycled (*e.g.*, at a rate of 100 mV/s) to deposit an organic film (*e.g.*, poly-butylmethacrylate).

[0128] In other embodiments, a poly-methyl-methacrylate (pMMA) film may be electrografted to a VSDM material by immersing the VSDM in a solution comprising MMA (*e.g.*, 3.125 mol/L of MMA, $1\text{E-}2$ mol/L of 4-nitrophenyldiazonium tetrafluoroborate and $2.5\text{E-}2$ mol/L of Na-nitrate in DMF), and subjecting the immersed VSDM to a voltage cycle sufficient to cause the VSDM to become conductive. An exemplary voltage cycle may include cycling between -0.1 and -3 V/(Ag+/Ag) at 100 mV/sec to form a pMMA layer on the VSDM.

[0129] FIG. 14 illustrates an exemplary method and structure that incorporates a conductive backplane. In some applications, it may be advantageous to provide a conductive backplane “beneath” or “behind” a

VSDM layer. FIG. 14 is a diagrammatic representation of exemplary processing steps (left side) and corresponding structures (right hand side) associated with a conductive backplane, according to certain embodiments.

[0130] In step 1400, a conductive backplane 1402 is provided. In some cases, the conductive backplane may be incorporated into or onto a substrate. In some embodiments, a conductive backplane may act as a substrate itself (*e.g.*, a thick metal foil or sheet). In step 1410, a voltage switchable dielectric material 1412 may be deposited on at least a portion of the conductive backplane (*e.g.*, by spin coating).

[0131] In some embodiments, VSDM 1412 may be masked to demarcate exposed regions for subsequent creation of a current-carrying formation. In other embodiments, VSDM 1412 may be unmasked. In optional step 1420, mask 1422 may be applied to VSDM 1412, defining a region 1424 where a current-carrying formation may be deposited.

[0132] In step 1430, a current carrying formation 1432 may be formed by depositing a conductive material on the VSDM 1412 (in this example, in region 1424). In optional step 1440, mask 1422 may be removed.

[0133] A conductive backplane may reduce the distance or thickness of VSDM through which electrical current passes (*e.g.*, the conductive backplane may act as a “bus bar”). A conductive backplane may improve (*e.g.*, smooth out or make more uniform) the current density distribution through the VSDM. Embodiments without a conductive backplane may require some current

passage in a horizontal dimension (*i.e.*, normal to the thickness of a VSDM layer). Embodiments with a conductive backplane may provide for reduced distances of current passage, in that electrical current may pass from a current-carrying formation through the VSDM layer to the conductive backplane in a direction orthogonal to the layer.

[0134] A conductive backplane may improve the uniformity of current density during deposition (*e.g.*, of a current carrying formation) and may improve the performance of a VSDM in certain electrostatic discharge (ESD) events. A conductive backplane may result in a reduced distance over which current passes, which may provide for lower resistance as compared to a VSDM layer not disposed on a conductive backplane. Alternately, a thinner VSDM layer may be combined with a conductive backplane to yield properties equivalent to a thicker VSDM layer without a conductive backplane. A conductive backplane may be metallic (*e.g.*, Cu, Al, TiN); a conductive backplane may include a conductive polymer.

[0135] FIG. 15 is a diagrammatic illustration of attaching a package, according to some embodiments. A package may be attached to a current-carrying formation and/or a voltage switchable dielectric material. The attached components may be protected (*e.g.*, from dust, moisture and the like) using the package. A package may provide for improved mechanical properties (*e.g.*, strength, stiffness, resistance to warping) and/or may improve the ease with which packaged components may be further processed (*e.g.*, attaching

leads to a device). Vias, studs, lines, wires and/or other connections to a device contained within the package may be included with a package.

[0136] FIG. 15 illustrates attachment of a package 1502 to a component including a current-carrying formation 1504 deposited on a voltage switchable dielectric material 1505. In this example, voltage switchable dielectric material 1505 may be disposed on an optional conductive backplane 1506, which may be disposed on an optional substrate 1508. In certain embodiments, a package may be attached to a current-carrying formation and/or VSDM without a conductive backplane and/or without a substrate.

[0137] In step 1500, a package 1502 is attached, typically to at least a portion of the voltage switchable dielectric material 1504 and current-carrying formation 1505. A package may include a polymer, a composite, a ceramic, a glass, or other material. A package may be insulating. In some embodiments, a package may include a polymer coating, such as a phenolic, an epoxy, a ketone (e.g., poly-ether-ether ketone, or PEEK) and/or various materials used in microelectronics packaging and/or the fabrication of printed wiring boards.

[0138] In optional step 1510, substrate 1508 may be removed. Certain embodiments include a substrate that is dissolvable, etchable, or meltable. A substrate may include a wax or other material that melts at temperatures below 50 Celsius. A substrate may include a metal foil. In certain embodiments, a decohesion layer may be incorporated at the interface between the substrate and the conductive backplane (or the VSDM, as the

case may be), which may provide for improved removability of the substrate.

A decohesion layer may include an intermediate layer.

[0139] In optional step 1520, conductive backplane 1506 may be removed. In some cases (*e.g.*, a conductive backplane comprising Cu) a conductive backplane may be dissolved or etched (*e.g.*, in an appropriate acid). In some cases, a conductive backplane comprising an electrically conducting polymer may be dissolved in an organic solvent. A conductive backplane may be thermally etched, plasma etched, ashed, or otherwise removed.

[0140] In some embodiments, a VSDM may be disposed directly on a substrate, and the substrate may be removed after formation of a current-carrying formation, and often after having attached a package. In some embodiments, a VSDM may be disposed on a conductive backplane without a substrate, and the conductive backplane may be removed after having formed a current-carrying formation. A decohesion layer may aid removal in these and other applications.

[0141] FIGS. 16A and 16B illustrate cross section and perspective views (respectively) of a removable contact mask, according to certain embodiments. In this example, substrate 1600 having a layer of voltage switchable dielectric material (VSDM) 1602 is shown, although a contact mask may be used with a voltage switchable dielectric material without a substrate.

[0142] In some embodiments, a contact mask 1610 includes an insulating foot 1620 and an electrode 1630. Electrode 1630 may connect to one or more

electrical leads 1632, which may provide for electrochemical reactions.

Contact mask 1610 typically includes one or more openings 1640, which may be openings in insulating foot 1620.

[0143] Insulating foot 1620 may sealingly attach contact mask 1610 to VSDM 1602 in such a manner as to form a seal. The sealed regions of VSDM 1602 are masked from deposition or other reaction. In some embodiments, contact mask 1610 may be pressed against VSDM 1602. Typically, insulating foot 1620 may be sufficiently compliant that contact mask 1610 masks a region of VSDM 1602 from formation of a current-carrying structure and defines a portion 1650 of VSDM 1602 upon which a current-carrying formation may be formed.

[0144] Insulating foot 1620 may separate electrode 1630 from VSDM 1602 by a distance 1660. Distance 1660 may be less than 1cm, 5mm, 1mm, or even less than 500 microns. Insulating foot 1620 may also support electrode 1630 substantially parallel to VSDM 1602, which may improve the uniformity of current-density (*e.g.*, during deposition) through portion 1650. Insulating foot 1620 may be fabricated from a variety of ceramic, polymer, or other insulating materials, such as polyimide, poly-tetrafluoroethylene, latex, photoresist materials, epoxy, polyethylene, and spin-on polymers. In some embodiments, an intermediate layer may be used to improve adherence and/or sealing of an insulating foot to an electrode. In some embodiments, an

intermediate layer may be used to improve sealing and/or adherence of an insulating foot to a VSDM.

[0145] Openings 1640 may be configured to expose one or more portions 1650 to a fluid (*e.g.*, a liquid, gas, plasma and the like) containing ions associated with formation of a current-carrying structure. For example, depositing a copper conductor may include exposing portion 1650 to a solution having copper ions. Typically, openings 1640 are sufficiently large and/or plentiful that a deposition fluid may be supplied “continuously” or fast enough that the supply of deposition fluid does not limit deposition.

[0146] Electrode 1630 may be fabricated from a suitably conductive material. In some embodiments, electrode 1630 may include a metal foil, such as a Ti, Pt, or Au foil. Contact mask 1610 may also include additional materials, such as layers that improve mechanical properties, layers that improve adherence, layers that improve deposition quality and the like. Electrode 1630 and insulating foot 1620 may each comprise a plurality of materials. In certain embodiments, a die (not shown) having a pattern (*e.g.*, that matches the shape of portions 1650) is used to apply uniform pressure to a “top” side of contact mask 1610.

[0147] Formation of one or more current-carrying formations may include electrochemical deposition, and in some cases, may include electrochemical pattern replication (ECPR) as described in U.S. patent application publication

number 2004/0154828 A1, the disclosure of which is incorporated herein by reference.

[0148] FIG. 17 illustrates deposition of a current-carrying material to form a current-carrying formation, according to certain embodiments. Exemplary steps in a deposition process are shown on the left side of FIG. 17, along with exemplary structures on the right side of FIG. 17.

[0149] In step 1700, contact mask 1610 may be applied to a voltage switchable dielectric material (VSDM) 1710 to form a “sandwich” 1720. Sandwich 1720 may optionally include a substrate 1712. Typically, VSDM 1710 and substrate 1712 may be planar and sufficiently stiff that contact mask 1610 may be sealingly attached to VSDM 1710. Typically, contact mask 1610 is removably attached to VSDM 1710, for example using a clamp or other means of applying pressure.

[0150] In step 1730, sandwich 1720 may be immersed in a fluid 1732 that provides a source of ions associated with a current-carrying material. In some embodiments, fluid 1732 may be a plating solution. For example, a solution having copper ions may be used to fabricate a copper current-carrying formation, with metallic copper forming the electrical conductor of the formation. Fluid 1732 may be circulated and/or agitated such that it passes through openings 1640, exposing portions 1650 to the fluid.

[0151] In step 1740, a voltage 1742 may be created between electrode 1630 and VSDM 1710. Typically, voltage 1742 is larger (in magnitude) than a

characteristic voltage associated with VSDM 1710, such that VSDM 1710 conducts current under voltage 1742. Voltage 1742 may cause a deposition of a current-carrying formation 1744 on portion 1650. Fluid 1732 may be replenished (*e.g.*, via openings 1640) sufficiently fast that current-carrying formation plates uniformly.

[0152] In step 1750, contact mask 1610 may be removed. In some embodiments, a contact mask may be re-used for multiple depositions. In some embodiments, a voltage may be applied prior to immersion of the VSDM/contact mask into the plating solution. In some embodiments, the applied voltage may be maintained until after the VSDM/contact mask has been removed from the plating solution.

[0153] FIG. 18 illustrates a current-carrying formation fabricated using an etching process, according to certain embodiments. Exemplary steps are shown on the left side of FIG. 18, along with exemplary structures on the right side of FIG. 18.

[0154] In step 1800, a contact mask 1610 may be applied to a conductor 1802 disposed on a voltage switchable dielectric material (VSDM) 1804, which may be disposed on top of a substrate 1806, forming a “sandwich” 1808. Contact mask 1610 defines one or more portions 1814 of conductor 1802 to be exposed to an etching solution, and prevents etching of regions of conductor 1802 in regions beneath the mask.

[0155] In step 1810, sandwich 1808 may be immersed in an etching solution 1812. Etching solution 1812 may be chosen to electrochemically etch conductor 1802, often using an applied voltage. Etching solution 1812 may pass through openings 1640, reaching exposed portions 1814. A deposition solution may also be operated as an etching solution by reversing the sign (or polarity) of the applied voltage.

[0156] In step 1820, a voltage 1822 may be applied between electrode 1630 and VSDM 1804. Voltage 1822 may be chosen to match a composition of etching solution 1812 and optionally the circulation of etching solution 1812 through openings 1640, such that conductor 1802 may be etched. Typically, voltage 1822 is greater than a characteristic voltage associated with VSDM 1804, which may be greater than a typical etching voltage (*e.g.*, 1 volt, 3 volts, or 5 volts). The regions of conductor 1802 remaining unetched may become one or more current-carrying formations 1824.

[0157] In step 1830, contact mask 1610 may be removed. In some embodiments, conductor 1802 may be deposited as a sufficiently thick layer (*e.g.*, several microns or more) that current-carrying formation 1824 may be used as-etched.

[0158] In optional step 1840, an additional current-carrying material 1842 may be incorporated into current-carrying formation 1824. For example, by exposing current-carrying material 1824 to a deposition solution and creating an appropriate voltage between VSDM 1804 and a counterelectrode in the

solution, an additional current-carrying material 1842 may be deposited on current-carrying formation 1824.

[0159] FIG. 19 illustrates a voltage switchable dielectric material (VSDM) 1910 having regions with different characteristic voltages, according to certain embodiments. Such a configuration may improve an ability to fabricate current-carrying formations in different regions. VSDM 1910 may have regions having different deposition and/or etching characteristics. For example, a first region 1940 may include one or more voltage switchable dielectric materials having a first characteristic voltage, and a second region 1950 may include one or more voltage switchable dielectric materials having a second characteristic voltage. A current-carrying formation may be formed on first region 1940, or second region 1950, or both regions, according to different deposition conditions. VSDM 1910 may be disposed on a conductive backplane 1920, which may optionally be disposed on a substrate 1930.

[0160] In an embodiment, first region 1940 may be characterized by a first thickness 1942 between conductive backplane 1920 and the surface of region 1940. A second region 1950 may be characterized by a second thickness 1952 between conductive backplane 1920 and the surface of region 1950.

[0161] In certain embodiments, regions 1940 and 1950 may also be characterized by depths 1946 and 1956, respectively. Under certain deposition conditions, deposition may include immersing VSDM 1910 in a deposition solution having ions associated with a material to be deposited. In

some cases, diffusion of ions from the bulk solution to the surfaces of regions 1940 and 1950 (*e.g.*, down depths 1946 and 1956) may be slow enough that a difference between depths 1946 and 1956 has an appreciable effect on the relative deposition and/or etching rates at the respective surfaces. In some embodiments, a cyclic voltage may be imposed, and in some cases, the frequency of the cyclic voltage is chosen pursuant to diffusion times associated with diffusion of ions within depths 1946 and 1956.

[0162] Deposition may include the use of an electrode 1960, which may be a planar electrode. In certain embodiments, deposition and/or etching in regions 1940 and 1950 may be modified by choosing an appropriate distance from the respective surface to electrode 1960. For example, first distance 1944 may characterize a length from the surface of region 1940 to electrode 1960, and second distance 1954 may characterize a length from the surface of region 1950 to electrode 1960.

[0163] In some embodiments, first region 1940 may have a different characteristic voltage than that of second region 1950. In some cases, this difference may be due to different thicknesses of the VSDM in each region, which may cause a difference in the field densities associated with the regions. In some embodiments, a different VSDM may be used in each region. In some embodiments, a VSDM layer may include a plurality of VSDM materials (*e.g.*, arranged in layers). For example, a first VSDM may

have a depth equal to second thickness 1952, and a combination of first VSDM and second VSDM may have a depth equal to first thickness 1942.

[0164] Regions having different characteristic voltages may be fabricated by stamping or other physical forming. Regions having different characteristic voltages may be fabricated by ablating, laser-ablating, etching, or otherwise removing material. A first region may be formed using a first mask (*e.g.*, a photoresist), and a second region may be formed using a second mask.

[0165] FIGS. 20A-C illustrate the deposition of one or more current-carrying formations, according to certain embodiments. In each figure, VSDM 1920 is used as an example for illustrative purposes only. VSDM 1920 includes a first region 1940 having a first characteristic voltage, and a second region 1950 having a second characteristic voltage. A current-carrying formation may be formed on first region 1940, or second region 1950, or both regions 1940 and 1950, according to different processing conditions.

[0166] FIG. 20A illustrates a structure comprising a first electrical conductor 2010, formed on second region 1950. Electrical conductor 2010 may be formed, for example, by exposing VSDM 1910 to a source of ions (associated with the conductor). A voltage difference may be created between VSDM 1910 and the source of ions that is greater than the characteristic voltage associated with second region 1950 and less than the characteristic voltage associated with first region 1940. First region 1940 may remain insulating,

while second region 1950 becomes conducting, and deposition may occur only on second region 1950.

[0167] FIG. 20B illustrates a structure comprising a first electrical conductor 2020 formed on first region 1940 and a second electrical conductor 2030 formed on second region 1950. Electrical conductors 2020 and 2030 may be formed, for example, by exposing VSDM 1910 to a source of ions (associated with the conductor). A voltage difference may be created between VSDM 1910 and the source of ions that is greater than the characteristic voltages associated with both first region 1940 and second region 1950. Deposition may occur on both first region 1940 and second region 1950.

[0168] FIG. 20C illustrates a structure having a first electrical conductor 2020 formed on first region 1940 having a characteristic voltage that is greater than the characteristic voltage associated with second region 1950. Such a structure may be formed, for example, by selectively etching a structure formed according to FIG. 20B. For example, electrical conductors 2020 and 2030 may be formed by exposing VSDM 1910 to a source of ions (associated with the conductor). A voltage difference may be created between VSDM 1910 and the source of ions that is greater than the characteristic voltages associated with both first region 1940 and second region 1950. Deposition may occur on both first region 1940 and second region 1950, forming two (or more) current-carrying formations. Subsequently, electrical conductor 2030 may be preferentially etched (*e.g.*, to the point of its complete removal),

leaving electrical conductor 2020 as shown. In some embodiments, a conductor may be etched by reversing the polarity of a deposition voltage. In such cases, etching may be associated with current flow through a region. By choosing an etching voltage that is greater than the characteristic voltage associated with second region 1950, but less than the characteristic voltage associated with first region 1940, preferential etching associated with second region 1950 may be achieved.

3. Micro-Circuit Board Applications

[0169] Embodiments of the invention also provide micro-circuit board applications. For example, smart cards are credit-card size substrate devices having one or more embedded computer chips. A smart card typically includes a mounted micro-memory module and conductors for interconnecting the micro-memory module with other components such as a sensor for detecting smart card readers. Due to the size of the smart card, as well as the size of the components embedded or mounted to the smart card, conductive elements on the substrate of the smart card also have to be very small.

[0170] In an embodiment, a voltage switchable dielectric material is used for the substrate of a smart card. An electrolytic plating process such as described above is used to produce a pattern of connectors on the smart card to connect the memory module to other components. A conductive layer comprising the pattern of connectors is plated onto the surface of the

substrate through a photoresist mask as described above. By using a voltage switchable dielectric material, the pattern of connectors can be plated onto the substrate without having to etch. This can reduce the thickness of the conductive layer on the substrate.

[0171] Another micro-circuit board application includes a circuit board that packages two or more processors together. The circuit board includes leads and circuits that enable high-level communications between the several processors mounted on the board so that the processors act substantially as one processing unit. Additional components such as a memory can also be mounted to the circuit board to communicate with the processors. Fine circuitry and lead patterns are therefore required to preserve processing speed for communications that pass between two or more processors.

[0172] As with previous embodiments, such as the embodiments directed to smart cards, the micro-circuit board also includes a substrate formed from a voltage switchable dielectric material. A fine resist layer is patterned onto the substrate to define a pattern for selected regions of conductive material to be subsequently deposited. An electrolytic process is used to plate conductive material in selected regions according to a pattern to interconnect processors subsequently mounted to the circuit board.

[0173] Again, one advantage provided by using voltage switchable dielectric materials is that conductive layers can be made with reduced thicknesses. Another advantage is that plating conductive material with fewer fabrication

steps reduces manufacturing costs for the micro-circuit board. Still another advantage is that a micro-circuit board can be developed to have conductive elements formed from more than one type of conductive material. This is particularly advantageous for interconnecting processors on one micro-circuit board because material requirements of the conductors may vary for each processor, depending on the quality, function, or position of each processor. For example, processors of the micro-circuit board that are exposed to the environment may require more durable conductive elements, for example made from nickel, to withstand temperature fluctuations and extremes. Whereas a processor for handling more computationally demanding functions, and located away from the environment, can have contacts and leads formed from a material with a higher electrical conductivity such as gold or silver.

4. Magnetic Memory Device

[0174] In another application, a substrate is integrated into a memory device that includes a plurality of memory cells. Each memory cell includes a layer of a magnetic material. The orientation of a magnetic field of the layer of the magnetic material stores a data bit. The memory cells are accessed by electrical leads. Voltages applied to the memory cells via the electrical leads are used to set and to read the orientations of magnetic fields. Transistors

mounted to, or formed in, the substrate are used to select the memory cells to be set and to be read.

[0175] In an embodiment of the invention, the substrate used in the memory device is formed from a voltage switchable dielectric material. A first non-conductive layer is deposited and patterned on the substrate to define regions where the layer of magnetic material is to be fabricated. A first electrolytic process, as described above, is used to plate the layer of magnetic material on the substrate. The electrolytic process, for example, can be used to plate a cobalt-chromium (CoCr) film as the layer of magnetic material. Similarly, a second non-conductive layer may be deposited and masked on the substrate to define regions where the electrical leads are to be located. A second electrolytic process is then used to plate the electrical leads.

5. Stacked Memory Devices

[0176] Under still another embodiment, a multi-substrate memory device includes a plurality of substrates each formed from a voltage switchable dielectric material. The substrates are stacked and are electrically interconnected using one or more vias. As shown by FIGS. 5 and 7, the vias are plated with a current-carrying layer by an electrolytic process. Several advantages are apparent under this embodiment of the invention. The vias can be plated during a fabrication step with one or more of the current-carrying formations formed on the surface of the respective substrates. The

plating on the surface of the vias is also less expensive to produce and more reliable than plated vias produced by previous methods, such as by seeding the surfaces of the vias or using adhesives.

6. Flex Circuit Board Devices

[0177] Yet another embodiment of the invention provides flex circuit board devices. Flex circuit boards generally include a high density of electrical leads and components. Unfortunately, increasing the density of electrical and conductive elements can diminish the speed and/or capacity of the flex circuit board. Embodiments of the invention provide a flex circuit board that advantageously uses a voltage switchable dielectric material to increase the density of electrical and conductive components on the flex circuit board.

[0178] Under an embodiment, a composition of a voltage switchable dielectric material is selected and molded into a flexible and thin circuit board. A resist layer is patterned onto the substrate to define finely spaced regions, as above. A voltage exceeding the characteristic voltage of the particular voltage switchable dielectric material is applied to the voltage switchable dielectric material and a current-carrying formation is plated to form leads and contacts in the finely spaced regions.

[0179] By using a voltage switchable dielectric material, current-carrying precursors are deposited directly on the surface of the substrate to form the current-carrying formation. This allows the current-carrying formation to

have a reduced thickness in comparison to previous flex circuit board devices. Accordingly, the respective electrical and conductive elements on the surface of the flex circuit board can be thinner and spaced more closely together. An application for a flex circuit board under an embodiment of the invention includes a print head for an ink jet style printer. Thus, the use of a voltage switchable dielectric material enables the flex circuit board to have more finely spaced electrical components and leads resulting in increased printing resolution from the print head.

7. Radio Frequency ID (RFID) Tags

[0180] Yet another embodiment of the invention provides RFID tags. In these embodiments the method of the invention can also be used to fabricate antennas and other circuitry on substrates for RFID and wireless chip applications. Additionally, a layer of a voltage switchable dielectric material can be used as an encapsulant.

Conclusion

[0181] In the foregoing specification, the invention is described with reference to specific embodiments thereof, but those skilled in the art will recognize that the invention is not limited thereto. Various features and aspects of the above-described invention may be used individually or jointly. Further, the invention can be utilized in any number of environments and applications

beyond those described herein without departing from the broader spirit and scope of the specification. The specification and drawings are, accordingly, to be regarded as illustrative rather than restrictive. It will be recognized that the terms "comprising," "including," and "having," as used herein, are specifically intended to be read as open-ended terms of art.

CLAIMS

What is claimed is:

1. A method for fabricating a current-carrying formation, the method comprising:
 - providing a layer of a voltage switchable dielectric material, the layer including a first region having a first characteristic voltage and a second region having a second characteristic voltage greater than the first characteristic voltage;
 - exposing the voltage switchable dielectric material to a source of ions associated with an electrical conductor;
 - creating a first voltage between the layer and the source of ions, the first voltage greater than the first characteristic voltage and less than the second characteristic voltage; and
 - depositing the electrical conductor on the first region.
2. The method of claim 1, wherein the layer is provided on a conductive backplane.
3. The method of claim 1 wherein the voltage switchable dielectric material in the first region has a first thickness and the voltage switchable dielectric material in the second region has a second thickness.

4. The method of claim 1, wherein the electrical conductor is not deposited on the second region under the first voltage.
5. The method of claim 1, wherein any of the first and second regions includes two or more voltage switchable dielectric materials.
6. The method of claim 1, wherein the electrical conductor includes any of Cu, Al, Ti, Ag, Au, and Pt.
7. The method of claim 1, wherein depositing includes electroplating.
8. The method of claim 1, wherein the first voltage includes a cyclic voltage.
9. The method of claim 1, wherein the first voltage is between 2 and 50 volts.
10. The method of claim 9, wherein the first voltage is between 5 and 20 volts.
11. The method of claim 1, further comprising:
creating a second voltage between the layer and the source of ions, the second voltage greater than the first and second characteristic voltages; and
depositing the electrical conductor on the first and second regions.

12. A method for fabricating a current-carrying formation, the method comprising:

providing a layer of a voltage switchable dielectric material, the layer including a first region having a first characteristic voltage and a second region having a second characteristic voltage greater than the first characteristic voltage;

exposing the voltage switchable dielectric material to a source of ions associated with an electrical conductor;

creating a first voltage between the layer and the source of ions, the first voltage greater than the first and second characteristic voltages;

and

depositing the electrical conductor on the first and second regions.

13. The method of claim 12, further comprising etching the electrical conductor from the first region.

14. The method of claim 13, wherein the second region retains at least a portion of the electrical conductor after etching.

15. The method of claim 12, further comprising:

creating a second voltage between the layer and the source of ions, the second voltage greater than the first characteristic voltage and less than the second characteristic voltage, the second voltage having a polarity that induces an etching of the deposited electrical conductor; and etching the electrical conductor from the first region.

16. The method of claim 15, wherein the second region retains at least a portion of the electrical conductor after etching.
17. The method of claim 12, wherein the layer is provided on a conductive backplane.
18. The method of claim 12 wherein the voltage switchable dielectric material in the first region has a first thickness and the voltage switchable dielectric material in the second region has a second thickness.
19. The method of claim 12, wherein any of the first and second regions includes two or more voltage switchable dielectric materials.
20. The method of claim 12, wherein the electrical conductor includes any of Cu, Al, Ti, Ag, Au, and Pt.

21. The method of claim 12, wherein depositing includes electroplating.
22. The method of claim 12, wherein the first voltage includes a cyclic voltage.
23. The method of claim 15, wherein the second voltage includes a cyclic voltage.
24. A structure comprising:
- a conductive backplane;
 - a voltage switchable dielectric material disposed on the conductive backplane, the voltage switchable dielectric material having a first region with a first characteristic voltage and a second region with a second characteristic voltage; and
 - one or more conductors deposited on any of the first and second regions.