CLAIMS

What is claimed is:

1. A microelectronic package comprising:

a microelectronic die having an active surface, an opposing back surface, and at least two opposing sides extending between the microelectronic die active surface and the microelectronic die back surface;

an interposer proximate the at least one microelectronic die side;

an encapsulation material adjacent the at least one microelectronic die side; and

a stacked microelectronic die attached to the interposer.

2. The microelectronic package of claim 1, wherein the interposer is proximate the at least two opposing microelectronic die sides;

3. The microelectronic package of claim 2, wherein the stacked microelectronic die substantially spans the microelectronic die.

4. The microelectronic package of claim 2, wherein the interposer substantially surrounds the microelectronic die.

5. The microelectronic package of claim 1, wherein the interposer is integral with the microelectronic die.

6. The microelectronic package of claim 5, wherein the interposer substantially surrounds an active area of the microelectronic die.

7. The microelectronic package of claim 1, further including a build-up layer formed proximate the microelectronic die active surface.

8. The microelectronic package of claim 1, wherein the encapsulation material includes a back surface that is substantially planar to the microelectronic die back surface.

9. The microelectronic package of claim 8, wherein the interposer includes a front surface and a back surface and wherein the encapsulation material back surface is substantially planar to the interposer back surface.

10. The microelectronic die of claim 1, wherein the microelectronic die comprises a microprocessor, and wherein the stacked microelectronic die comprises a memory device.

11. A method of forming a microelectronic package, comprising:

providing a microelectronic die having an active surface, an opposing back surface, and at least two opposing sides extending between the microelectronic die active surface and the microelectronic die back surface;

providing an interposer proximate at least one microelectronic die side;

disposing an encapsulation material adjacent the at least one side of the microelectronic die; and

attaching a stacked microelectronic die to the interposer.

12. The method of claim 11, wherein providing the interposer comprises providing an interposer proximate the at least two opposing microelectronic die sides.

13. The microelectronic package of claim 12, wherein attaching the stacked microelectronic die comprises attaching a stacked microelectronic die to the interposer to span the microelectronic die.

14. The method of claim 12, wherein providing the interposer comprises providing an interposer which substantially surrounds the microelectronic die.

15. The method of claim 11, wherein the providing the interposer comprises providing an interposer that is integral with the microelectronic die.

16. The method of claim 15, wherein the providing the interposer that is integral with the microelectronic die comprises providing an interposer that substantially surrounds an active area of the microelectronic die.

17. The method of claim 11, further comprising forming a build-up layer proximate the microelectronic die front surface.

18. The method of claim 11, wherein disposing the encapsulation material includes disposing an encapsulation material to form a back surface that is substantially planar to the microelectronic die back surface.

19. The method of claim 18, wherein providing the interposer comprises providing an interposer including a front surface and a back surface, and wherein disposing the encapsulation material comprises disposing the encapsulation material to form a back surface that is substantially planar to the interposer back surface.

20. The method of claim 11, wherein the microelectronic die comprises a microprocessor and the stacked microelectronic die comprises a memory device.

CLAIMS

What is claimed is:

1. A microelectronic package comprising:

a microelectronic die having an active surface, an opposing back surface, and at least two opposing sides extending between the microelectronic die active surface and the microelectronic die back surface;

an interposer integral with the microelectronic die;

an encapsulation material adjacent the at least one microelectronic die side; and

a stacked microelectronic die attached to the interposer.

2. The microelectronic package of claim 1, wherein the interposer is formed on the at least two opposing microelectronic die sides.

3. The microelectronic package of claim 2, wherein the stacked microelectronic die spans the microelectronic die.

4. The microelectronic package of claim 2, wherein the interposer surrounds an active area of the microelectronic die.

5. The microelectronic package of claim 1, wherein the encapsulation material includes a front surface, further including a build-up layer formed on a front surface of the encapsulation material.

6. The microelectronic package of claim 1, wherein the encapsulation material includes a back surface that is planar to the microelectronic die back surface.

7. The microelectronic package of claim 6, wherein the interposer includes a front surface and a back surface and wherein the encapsulation material back surface is planar to the interposer back surface.

8. The microelectronic die of claim 1, wherein the microelectronic die comprises a microprocessor, and wherein the stacked microelectronic die comprises a memory device.

9. A method of forming a microelectronic package, comprising:

providing a microelectronic die having an active surface, an opposing back surface, and at least two opposing sides extending between the microelectronic die active surface and the microelectronic die back surface;

providing an interposer that is integral with the microelectronic die;

disposing an encapsulation material adjacent the at least one side of the microelectronic die; and

attaching a stacked microelectronic die to the interposer.

10. The method of claim 9, wherein providing the interposer comprises providing an interposer formed on the at least two opposing microelectronic die sides.

11. The microelectronic package of claim 10, wherein attaching the stacked microelectronic die comprises attaching a stacked microelectronic die to the interposer to span an active area of the microelectronic die.

12. The method of claim 10, wherein providing the interposer comprises providing an interposer which surrounds an active area of the microelectronic die.

13. The method of claim 9, wherein disposing the encapsulation material includes disposing an encapsulation material to form a front surface, further comprising forming a build-up layer on the front surface of the encapsulation material.

14. The method of claim 9, wherein disposing the encapsulation material includes disposing an encapsulation material to form a back surface that is planar to the microelectronic die back surface.

15. The method of claim 14, wherein providing the interposer comprises providing an interposer including a front surface and a back surface, and wherein disposing the encapsulation material comprises disposing the encapsulation material to form a back surface that is planar to the interposer back surface.

16. The method of claim 9, wherein the microelectronic die comprises a microprocessor and the stacked microelectronic die comprises a memory device.