

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN FM STEREO DEMODULATORS

(71) We, HITACHI, LTD., of 1-5-1, Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to an FM stereo demodulator, and more particularly to an abnormal sound-preventing circuit in an FM stereo demodulator.

In an FM stereo demodulator circuit employing a PLL (phase locked loop), a voltage-controlled oscillator circuit (hereinafter abbreviated to "VCO") constituting the PLL circuit receives an output signal of a phase detector in the PLL as a control signal and delivers an oscillation signal whose frequency and phase are controlled with regard to a pilot signal included in an FM detection signal. A reproduced subcarrier signal of 38 KHz for FM stereo demodulation is obtained on the basis of the oscillation signal.

The self oscillation frequency of the VCO, however, is affected by the supply voltage and fluctuates according to variations in the supply voltage even when the level of the control signal is constant.

Essentially, such fluctuation of the oscillation frequency is corrected by the output of the phase detector in the PLL. The correction, however, becomes impossible when the supply voltage drops drastically, causing the oscillation frequency to approach or exceed the boundary value between the lock range and the capture range of the PLL. When the frequency of the VCO has fluctuated in this manner, the frequency and phase of the reproduced subcarrier signal fluctuate accordingly, and a beat signal develops between the reproduced subcarrier signal and a subcarrier signal component in a composite signal of broadcast reception. As a result, an abnormal sound (noise) due to

the beat signal is included in each reproduced stereo output signal, i.e., right and left signals which are obtained by, for example, switching, the composite signal with the reproduced subcarrier signal.

Such an abnormal sound results in the case where the supply voltage has conspicuously dropped on account of, for example, a high voice output, or in the case where a battery whose electromotive force has dropped is used in a receiver such as a portable radio set which operates at a low voltage. Even in a receiver which operates at a comparatively high voltage, in the case where the supply voltage varies slowly when turning a power switch "on" or "off", the noise results in the course of the rise or fall of the supply voltage.

It is an object of the present invention to obviate the above mentioned difficulties by providing a circuit which prevents the abnormal sound from developing during low voltage operation as described above in an FM stereo receiving set.

According to the present invention there is provided an FM stereo demodulator including:

a phase locked loop circuit having a phase detector, a voltage-controlled oscillator and a frequency divider, said phase detector receiving a signal from the frequency divider and a pilot signal in a composite stereo signal, the voltage-controlled oscillator delivering an oscillation signal on the basis of an output signal of the phase detector, and the frequency divider receiving the oscillation signal and delivering the said signal;

a decoder circuit which receives the composite stereo signal and a reproduced subcarrier signal obtained on the basis of the oscillation signal of the voltage controlled oscillator;

a detection unit for detecting when the supply voltage falls below a predetermined value sufficient to cause the voltage-controlled oscillator to fluctuate beyond tolerable limits, and

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a control circuit operable from the output of the detection unit for switching the decoder circuit from stereo reproduction to monaural reproduction, when the supply voltage falls to the predetermined value.

5 The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:—

10 Fig. 1 is a block diagram showing one preferred form of FM stereo demodulator;

Fig. 2 is a circuit diagram of some of the blocks of the FM stereo demodulator shown in Fig. 1; and

15 Fig. 3 is a circuit diagram of circuit blocks 13 and 14 in Fig. 1.

Referring first to Fig. 1, the FM stereo demodulator includes a pre-amplifier 5. The pre-amplifier 5 receives at an input terminal 20 IN an FM detection signal, that is, a stereo composite signal which includes a sum signal of right and left signals, a difference signal modulated by a 38 KHz-subcarrier, and a 19 KHz-pilot signal. It delivers the amplified composite signal to lines L2 and L3.

25 The FM stereo demodulator also includes a phase detector 6, which receives the composite signal from the pre-amplifier 5 and 19 KHz-signal from a frequency divider circuit 10 to be described later and which provides a D.C. output corresponding to the phase difference between the pilot signal in the composite signal and the divided frequency output from the frequency divider circuit 10.

30 A D.C. amplifier 7 amplifies the output signal of the phase detector 6, and a voltage-controlled oscillator 8, receives the output signal of the D.C. amplifier 7 as a control signal. The VCO 8 delivers an oscillation signal of 76 KHz.

35 The FM stereo demodulator also includes frequency divider circuits 9 to 11. The frequency divider circuit 9 receives the output of the VCO 8, and delivers signals of a frequency divided by two. The frequency divider circuits 10 and 11 receive the divided frequency outputs of the frequency divider circuit 9 opposite in phase to each other, and each deliver signals of a frequency divided by two.

40 A phase detector 14 receives the composite signal from the pre-amplifier 5 and the 19 KHz-signal from the frequency divider circuit 11 and provides a D.C. output corresponding to the level of the pilot signal in the composite signal.

45 A trigger circuit 13 receives the output of the phase detector 14 and an output of a detection unit 1 to be described later and controls a stereo switching circuit 12 and a stereo indicating lamp PL.

50 The stereo switching circuit 12 transmits the reproduced subcarrier signal from the

frequency divider circuit 9 to a decoder circuit 15 on the basis of an output of the trigger circuit 13.

The stereo indicating lamp PL ignites during stereo reproduction.

70 The decoder circuit 15 receives the composite signal from the pre-amplifier 5 and the reproduced subcarrier signal transferred from the stereo switching circuit 12, and delivers reproduced stereo signals.

75 A low-pass filter 16 which is connected to the output of the phase detector 6, transmits the low frequency components of the output of the phase detector 6 to the succeeding stage.

80 The circuits 6 to 10 and 16 constitute a PLL (phase locked loop).

The circuit arrangements of each of the circuits 5 to 12, 14 and 15 are of known construction.

85 In the circuit illustrated by the block diagram, the output frequency of the frequency divider circuit 11 fluctuates in response to the fluctuation of the oscillation frequency of the VCO 8.

90 In the case where such a fluctuation arises in the output of the frequency divider circuit 11, the phase detector circuit 14 fails to detect the pilot signal in the composite signal, and hence, it may provide at its output terminal an output level which corresponds to the monaural reception state. In such a case, the stereo switching circuit 12 is opened through the trigger circuit 13. That is, the decoder circuit 15 attains the monaural reproduction state. With only the phase detector 14, however, the stereo switching circuit 12 is opened after the reproduced subcarrier signal from the frequency divider circuit 9 has fluctuated, so that the undesirable reproduced subcarrier signal is supplied to the decoder circuit 15 within the delay time of the operation.

95 In this embodiment, the detection unit 1 is arranged to prevent an abnormal sound from arising in the reproduced stereo output at the time of a low supply voltage. The trigger circuit 13 is controlled by the output of this detection unit.

100 The detection unit 1 is constituted by a circuit 2 for generating a reference voltage, a circuit 3 for generating a voltage which follows the fluctuations in the supply voltage of the VCO 8, and a voltage comparator circuit 4 for comparing both the voltages.

105 The abnormal sound as stated above is not audible in the state in which the amount of fluctuation of the oscillation frequency of the VCO 8 is comparatively small. It is desirable that the decoder circuit 15 carry out the stereo reproduction as far as possible during the stereo broadcast reception. The detecting level of the

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detection unit 1 is accordingly determined within a reasonable range with reference to that supply voltage of the VCO 8 which induces the fluctuation in the VCO oscillation output.

The output reference voltage of the reference voltage generator 2 is set so as to be substantially equal to the output voltage of the voltage generator circuit 3 at the time when the fluctuation is induced in the VCO oscillation output.

The voltage comparator circuit compares the output voltage of the circuits 2 and 3, and supplies a low level signal at its output terminal when the output voltage of the circuit 3 has become lower than the reference output voltage of the circuit 2.

When the output signal of the detection unit 1, i.e., that of the voltage comparator circuit 4 is at the low level, the trigger circuit 13 opens the stereo switching circuit 12 irrespective of the level of the output signal of the phase detector 14.

According to the above construction, when the supply voltage drops to a value sufficient to cause the frequency of the VCO 8 to fluctuate beyond tolerable limits, or during the period in which the supply voltage is still low after a power switch is closed, the stereo switching circuit 12 is opened and stereo reproduction is compulsorily turned into monaural reproduction.

In this manner, the undesirable reproduced subcarrier signal whose frequency and phase fluctuate due to the low supply voltage is not fed to the decoder circuit 15, and only the normal reproduced subcarrier signal is fed thereto. As a result, generation of the abnormal sound is prevented.

Fig. 2 is a detailed circuit diagram of the detection unit 1 in the state in which it is combined with a constant-voltage circuit.

Referring to the figure, the constant-voltage circuit is made up of differential transistors Q_1 and Q_2 , as well as an emitter resistor R_1 , a diode D_1 which is arranged on the collector side of the transistor Q_1 , a p-n-p transistor Q_3 which is arranged in collector side of the transistor Q_2 , a transistor Q_4 which is controlled by the transistor Q_3 , series resistors R_2 and R_3 which divide a constant voltage of the emitter output of the transistor Q_4 , and diodes D_1 and D_2 and a resistor R_4 which constitute a reference voltage circuit arranged in correspondence with the divided voltage output.

The differential transistors Q_1 and Q_2 control the base potential of the transistor Q_4 so that the difference between the reference voltage composed of forward voltages developing in the diodes D_1 and D_2 and the divided voltage owing to the resistors R_2 and R_3 may become zero. In

consequence, the constant voltage V_R which depends on the forward voltages of the diodes D_1 and D_2 and the voltage dividing ratio of the resistors R_2 and R_3 is obtained at the emitter of the transistor Q_4 .

The voltage V_R is used as the supply voltage for the VCO 8 constructed of an RC oscillator circuit.

In this embodiment, the divided voltage output circuit which consists of the resistors R_2 and R_3 is also used as the voltage generator circuit 3, whilst the constant-voltage circuit which consists of the diodes D_1 and D_2 and the resistor R_4 is also used as the reference voltage circuit 2. The voltage comparator circuit 4 is made up of p-n-p transistors Q_5 and Q_6 , an emitter resistor R_5 which is connected to the common emitter of the transistors Q_5 and Q_6 , transistors Q_7 to Q_9 , resistors R_6 and R_7 , and a capacitor C_1 .

The base potential of the transistor Q_5 is substantially equal to that of the transistor Q_6 when the supply voltage V_{CC} is sufficiently high and the constant-voltage circuit is therefore operating normally. Accordingly, substantially equal collector currents flow through the transistors Q_5 and Q_6 . Owing to the collector current of the transistor Q_5 , the transistor Q_7 is conductive, and the transistors Q_8 and Q_9 are non-conductive.

On account of the non-conductive state of the transistor Q_9 , the trigger circuit 13 is controlled solely by the output of the phase detector 14.

When the supply voltage V_{CC} becomes low and it becomes impossible to apply sufficient bias voltages to the transistors Q_5 and Q_6 , the output voltage V_R of the voltage regulator circuit fails to remain at the constant voltage. In this case, the output voltage V_R fluctuates according to the fluctuation of the supply voltage V_{CC} .

Due to the lowering of the output voltage V_R , the voltage divided by the resistors R_2 and R_3 becomes lower than the forward voltages in the diodes D_1 and D_2 . As a result, the transistor Q_6 becomes conductive and the transistor Q_5 becomes non-conductive.

Since the transistor Q_5 is non-conductive the transistor Q_9 is rendered conductive. When the transistor Q_9 becomes conductive, the trigger circuit 13 opens the stereo switching circuit 12 and extinguishes the stereo indicating lamp PL irrespective of the output of the phase detector 14.

Fig. 3 is a circuit diagram of the phase detector 14 and the trigger circuit 13.

The phase detector 14 consists of transistors Q_{10} and Q_{11} , resistors R_8 to R_{11} , and a capacitor C_{11} . The composite signal from the pre-amplifier 5 is applied to the input line L2 of the phase detector 14, and

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the output signals from the frequency divider circuit 11 which have phases opposite to each other are applied to input lines L13 and L13' thereof. The transistors Q_{10} and Q_{11} execute switching operations in phases opposite to each other by the input signals applied to their respective bases. Under the state in which the PLL is locked, the signal on the line L13 has the same phase as that of the pilot signal in the composite signal on the line L2. During the stereo broadcast reception, a line L21 is at a positive potential with respect to a line L22. During the monaural reception, the potentials of the lines L21 and L22 become equal. A power source E_1 is a bias voltage source.

The trigger circuit 13 consists of transistors Q_{12} to Q_{21} , and resistors R_{12} to R_{17} . During the stereo broadcast reception, the collector current of the differential transistor Q_{14} is greater than that of the differential transistor Q_{13} owing to the potential difference between the lines L21 and L22, so that the transistor Q_{16} is conductive. If, at this time, the transistor Q_9 in Fig. 2 is non-conductive the potential of a line L14 is at the high level owing to the fact that the transistor Q_{16} is conductive. The high potential level of the line L14 brings the transistors Q_{20} and Q_{21} into conduction and consequently lights the lamp PL. Simultaneously, the stereo switching circuit 12 is closed through the resistor R_{14} and a line L12. In contrast, if the transistor Q_9 is conductive, the potential of the line L14 is at the low level, with the result that the transistors Q_{20} and Q_{21} are non-conductive and the stereo switching circuit 12 opens.

The transistor Q_{13} is set so as to cause collector current to flow which is greater than that of the transistor Q_{14} during monaural broadcast reception, so that the transistor Q_{16} is non-conductive. Under this state, the potential of the line L14 is at the low level.

As will be apparent from the above description the circuit 3 for generating the voltage which varies following up the supply voltage need not vary following up the supply voltage at all times, but it may vary following up the supply voltage at least while the supply voltage is below the value immediately before the generation of the abnormal sound.

Since the circuit of the above described embodiment uses the constant-voltage circuit and the voltage divider circuit also as the reference voltage circuit and the voltage generator circuit which constitute the abnormal sound-preventing circuit, respectively, an increase in the number of circuit elements used is avoided.

In a modified form, in order to change-

over the stereo reproduction to the monaural reproduction, the invention can adopt all the available expedients capable of stereo/monaural switching, such as stopping the oscillation of the VCO on the basis of the voltage comparison output and inhibiting the entrance of the pilot signal of the PLL on the basis of the same.

The voltage comparison output which serves to changeover the stereo reproduction to the monaural reproduction as described above may be also used for controlling, e.g., an indicating lamp indicative of the replacement of battery means in a battery-operated receiving set.

The detection unit of this invention is also applicable to a receiving set equipped with a PLL, in order to control a switching circuit for ceasing the receiving operation when the reception frequency fluctuates due to the lowering of the supply voltage.

WHAT WE CLAIM IS:—

1. An FM stereo demodulator including:
 - a phase locked loop circuit having a phase detector, a voltage-controlled oscillator and a frequency divider, said phase detector receiving a signal from the frequency divider and a pilot signal in a composite stereo signal, the voltage-controlled oscillator delivering an oscillation signal on the basis of an output signal of the phase detector, and the frequency divider receiving the oscillation signal and delivering the said signal;
 - a decoder circuit which receives the composite stereo signal and a reproduced subcarrier signal obtained on the basis of the oscillation signal of the voltage controlled oscillator;
 - a detection unit for detecting when the supply voltage falls below a predetermined value sufficient to cause the voltage-controlled oscillator to fluctuate beyond tolerable limits; and
 - a control circuit operable from the output of the detection unit for switching the decoder circuit from stereo reproduction to monaural reproduction, when the supply voltage falls to the predetermined value.
2. An FM stereo demodulator according to claim 1, wherein said detection unit consists of a voltage generator circuit which generates a voltage dependent on the supply voltage, a reference voltage generator circuit which delivers a reference voltage previously set, and a voltage comparator circuit connected at its inputs to the voltage generator circuit and the reference voltage generator circuit and at its output to said control circuit.
3. An FM stereo demodulator according to claim 2, wherein said voltage generator circuit is constituted by a constant-voltage

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the output signals from the frequency divider circuit 11 which have phases opposite to each other are applied to input lines L13 and L13' thereof. The transistors Q₁₀ and Q₁₁ execute switching operations in phases opposite to each other by the input signals applied to their respective bases. Under the state in which the PLL is locked, the signal on the line L13 has the same phase as that of the pilot signal in the composite signal on the line L2. During the stereo broadcast reception, a line L21 is at a positive potential with respect to a line L22. During the monaural reception, the potentials of the lines L21 and L22 become equal. A power source E₁ is a bias voltage source.

The trigger circuit 13 consists of transistors Q₁₂ to Q₂₁, and resistors R₁₂ to R₁₇. During the stereo broadcast reception, the collector current of the differential transistor Q₁₄ is greater than that of the differential transistor Q₁₃ owing to the potential difference between the lines L21 and L22, so that the transistor Q₁₆ is conductive. If, at this time, the transistor Q₉ in Fig. 2 is non-conductive the potential of a line L14 is at the high level owing to the fact that the transistor Q₁₆ is conductive. The high potential level of the line L14 brings the transistors Q₂₀ and Q₂₁ into conduction and consequently lights the lamp PL. Simultaneously, the stereo switching circuit 12 is closed through the resistor R₁₄ and a line L12. In contrast, if the transistor Q₉ is conductive, the potential of the line L14 is at the low level, with the result that the transistors Q₂₀ and Q₂₁ are non-conductive and the stereo switching circuit 12 opens.

The transistor Q₁₃ is set so as to cause collector current to flow which is greater than that of the transistor Q₁₄ during monaural broadcast reception, so that the transistor Q₁₆ is non-conductive. Under this state, the potential of the line L14 is at the low level.

As will be apparent from the above description the circuit 3 for generating the voltage which varies following up the supply voltage need not vary following up the supply voltage at all times, but it may vary following up the supply voltage at least while the supply voltage is below the value immediately before the generation of the abnormal sound.

Since the circuit of the above described embodiment uses the constant-voltage circuit and the voltage divider circuit also as the reference voltage circuit and the voltage generator circuit which constitute the abnormal sound-preventing circuit, respectively, an increase in the number of circuit elements used is avoided.

In a modified form, in order to change-

over the stereo reproduction to the monaural reproduction, the invention can adopt all the available expedients capable of stereo/monaural switching, such as stopping the oscillation of the VCO on the basis of the voltage comparison output and inhibiting the entrance of the pilot signal of the PLL on the basis of the same.

The voltage comparison output which serves to changeover the stereo reproduction to the monaural reproduction as described above may be also used for controlling, e.g., an indicating lamp indicative of the replacement of battery means in a battery-operated receiving set.

The detection unit of this invention is also applicable to a receiving set equipped with a PLL, in order to control a switching circuit for ceasing the receiving operation when the reception frequency fluctuates due to the lowering of the supply voltage.

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1. An FM stereo demodulator including: a phase locked loop circuit having a phase detector, a voltage-controlled oscillator and a frequency divider, said phase detector receiving a signal from the frequency divider and a pilot signal in a composite stereo signal, the voltage-controlled oscillator delivering an oscillation signal on the basis of an output signal of the phase detector, and the frequency divider receiving the oscillation signal and delivering the said signal;

a decoder circuit which receives the composite stereo signal and a reproduced subcarrier signal obtained on the basis of the oscillation signal of the voltage controlled oscillator;

a detection unit for detecting when the supply voltage falls below a predetermined value sufficient to cause the voltage-controlled oscillator to fluctuate beyond tolerable limits; and

a control circuit operable from the output of the detection unit for switching the decoder circuit from stereo reproduction to monaural reproduction, when the supply voltage falls to the predetermined value.

2. An FM stereo demodulator according to claim 1, wherein said detection unit consists of a voltage generator circuit which generates a voltage dependent on the supply voltage, a reference voltage generator circuit which delivers a reference voltage previously set, and a voltage comparator circuit connected at its inputs to the voltage generator circuit and the reference voltage generator circuit and at its output to said control circuit.

3. An FM stereo demodulator according to claim 2, wherein said voltage generator circuit is constituted by a constant-voltage



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circuit which feeds said voltage-controlled oscillator with a normally constant supply voltage.

5 4. An FM stereo demodulator according to claim 3, wherein said voltage generator circuit comprises a chain of voltage divider resistors.

10 5. An FM stereo demodulator according to claim 4, wherein said constant-voltage circuit comprises differential transistors, an emitter-follower transistor controlled by the differential transistors, its emitter electrode being connected to the voltage divider resistors.

15 6. An FM stereo demodulator according to claim 5, wherein the base electrodes of the differential transistors are respectively supplied with said reference voltage and the voltage generated at a common junction point in the chain of voltage divider resistors.

7 An FM stereo demodulator according to any one of the preceding claims, wherein said control circuit comprises a gate circuit which inhibits said reproduced subcarrier signal from being applied to said decoder circuit.

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8. An FM stereo demodulator according to any one of the preceding claims, wherein said signal from the frequency divider has a frequency of 19 KHz.

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9. An FM stereo demodulator constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying drawings.

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