

A unified memory architecture system using multiple physical memory channels. While modern memory systems offer compact bus interfaces, thus reducing the amount of required I/O ports for each memory bus, a unified memory architecture system is provided which allows a physical system-on-chip to be built using more than one physical memory channel. The unified memory architecture system is supported while also providing a multi-channel memory system that can take advantage of the multi-channel memory bandwidth to provide increased speed for an application. A performance/coast tradeoff can be adjusted dynamically by an end user application. 3-D renderings can be accomplished with the invention where performance may be optimized, while taking advantage of the multi-channel memory bandwidth for traditional graphics buffers.