Method and Apparatus for Reducing Disturbances on an Integrated Circuit

FIELD

This invention relates generally to noise on integrated circuitry and more specifically may apply to reducing noise induced into integrated circuitry power supplies.

CROSS REFERENCE TO RELATED PATENT APPLICATIONS

This patent application is related to United States patent application Serial No. 08/518,083, Attorney Docket No. AA9-95-014. entitled CONTROLLABLE DECOUPLING CAPACITOR, by Walls et al; filed August 22, 1995.

BACKGROUND

Capacitors may be used to reduce variation in voltage supplied to integrated circuitry, by coupling one or more capacitors from the supply to ground. Such capacitors tend to decouple the voltage supply from disturbances induced by activity of the supplied circuitry, and thus also to decouple portions of the circuitry itself.

It is common to include these decoupling capacitors on the die with the circuitry and to include means for limiting excessive capacitor leakage current that might develop, such as due to oxide failure. For example, a fuse may be included in series with such a capacitor, so that the fuse blows when the leakage current exceeds an allowable limit, thereby isolating the capacitor from ground so that the leakage current is substantially stopped.

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However, this is not ideal, because of heating required to blow the fuse.

Control circuitry has also been used to limit excessive leakage current. Krauter et al., U.S. patent 5,506,457, discloses control circuitry including a transistor in series with the capacitor, and feedback circuitry which turns off the series transistor if the capacitor develops excess leakage current. The feedback circuitry is responsive to voltage on a feedback node coupling one of the capacitor electrodes and one of the series transistor conducting electrodes.

One problem with such prior art control circuitry concerns sensitivity to transient currents. That is, the control circuitry may tend to respond to mere transient currents through the capacitor that arise from activity on circuitry supplied by the power supply. Even if the prior art feedback circuitry switches off the series transistor in response to a transient current, the series transistor tends to be held in the off state after the transient has subsided. Of course, this is a desirable response to excessive leakage current caused by oxide failure, but ideally there should be a different response for a transient current.

SUMMARY

An objective of the invention is to protect against excessive current through a decoupling capacitor.

Another objective is to distinguish between transient and more static conditions, in protecting against excessive current.

According to the present invention, the foregoing and other objects are attained by circuitry which includes a capacitor operatively coupled to a supply, and control circuitry for isolating the capacitor. The control circuitry isolates the capacitor in response to a current exceeding a certain threshold, but tends to restore the capacitor to operation if the current subsides.

In a further aspect, the control circuitry includes first second and third control devices. Such a control device may be a transistor, which has first and second conducting electrodes and a control (i.e., gate) electrode. The first control device may be switched to an off state to isolate the capacitor, by the second control device in response to a voltage produced by the excessive current. The third control device tends to discharge the voltage so that the second control device tends to turn on the first device if the current subsides.

In a still further aspect, the first control device is in series with the capacitor. One of the capacitor electrodes and one of the conducting electrodes of the first control device are operatively coupled at a node. Also coupled at the node, is the control electrode of the second control device. One of the conducting electrodes of the second control device is coupled to the control electrode of the first control device, so that the first control device is turned off, isolating the capacitor, by the second control device in response to the voltage on the node

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exceeding a voltage threshold (corresponding to the aforementioned current threshold). The third control device has a conducting electrode coupled to the node, and a conducting electrode coupled to ground, so that if the third control device is turned on, the node tends to discharge.

It is an advantage of the present invention that voltage supply variations and circuitry disturbances are reduced without undesirable consequences that may accompany the use of a fuse with the decoupling capacitor.

It is another advantage of the present invention that when the control circuitry isolates the capacitor in response to the condition of excessive current (and accompanying voltage), if the condition is transient the control circuitry responds further to de-isolate the capacitor, i.e., put the capacitor back into operation.

Additional objects, advantages, and novel features are set forth in the following description, or will be apparent to those skilled in the art or those practicing the invention. Other embodiments are within the spirit and scope of the invention. These objects and embodiments may be achieved by the combinations pointed out in the appended claims. The invention is intended to be limited only as defined in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates, for the present invention, circuitry for controlling a decoupling capacitor.

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DETAILED DESCRIPTION

To clearly point out novel features of the present invention, the following discussion omits or only briefly describes conventional features of decoupling capacitors which are apparent to those skilled in the art. For example, it is assumed that those skilled in the art are familiar with forming capacitors, transistors, interconnections and other aspects of integrated circuitry in semiconducting media, and with the electrical properties of such circuitry.

Referring now to FIG. 1, device 100, for reducing disturbances on an integrated circuit, is shown. Power supply 101, labelled "Vdd" in accordance with common terminology, is shown operatively coupled to capacitor 102. The capacitor 102 has two electrodes 104 and 106, electrode 104 being coupled to Vdd as an anode, and electrode 106 being coupled through control device 108 to ground 120 as a cathode. Control device 108 is an N type, field effect transistor ("NFET"), having first and second conducting electrodes 110 and 112, connected as source 112 and drain 110. Device 108 also has a control electrode, or gate, 114. Source 112 is connected to ground 120. Drain 110 is connected to the capacitor 102 cathode 106, forming node 126.

Also connected to node 126 is the "gate" of a second control device, inverter 124, and a conducting electrode of a third control device 122. The inverter 124 has an NFET and PFET connected with conducting electrodes in series and gates in parallel. These

parallel connected gates are referred to herein as the control electrode, or gate, of the second control device. The connected drains of the NFET and PFET are referred to as one of the conducting electrodes of the inverter, or second control device 124.

In the preferred embodiment, a PFET is included in the third control device 122, as shown by dashed lines in FIG. 1. The PFET and NFET 122 are connected as a second inverter.

One of the conducting electrodes of inverter 124 is connected to the gate 114 of NFET 108, forming node 115. The other conducting electrodes of inverter 124 and NFET 122 are connected to ground 120. The control electrode of NFET 122 is connected to an external signal 116.

The operation of circuitry 100 is as follows. In normal operation, NFET 122 is turned on (and, if present, PFET 122 is turned off) by the external signal 116 so that NFET 122 tends to discharge node 126. (It would be possible to substitute a resistor or other suitable device in place of the third control device, NFET 122, in order to discharge node 126.) In terms of current carrying capacity, NFET 122 is the smallest possible NFET, whereas NFET 108 is a substantially larger NFET, so that within short time intervals, such as a few RC time constants, when NFET's 108 and 122 are on, the voltage generated at node 126 by current flow through capacitor 102 is not greatly affected by the presence of NFET 122. For example, NFET 108 may have a channel width of one hundred to

two hundred microns, and NFET 122 may have a channel width of one to two microns, so that, when conducting, the resistance of NFET 122 is about 100 times that of NFET 108.

With NFET 122 on, this tends to turn on PFET 124 and turn off NFET 124, pulling node 115 and gate 114 high. This tends to turn on NFET 108 so that capacitor 102 is operative (i.e., not isolated from ground). However, if capacitor 102 allows sufficient current to flow, either due to transient conditions or a longer term condition, the current through NFETs 108 and 122 generate enough voltage at node 126 to exceed the switching thresholds of NFET 124 and PFET 124, so that inverter 124 automatically tends to pull node 115 and gate 114 down and switch off NFET 108. This substantially isolates capacitor 102, that is, isolates the capacitor 102 except for the relatively high resistance path to ground through NFET 122.

If the condition giving rise to the excessive current is a long term condition, and the current is large, as is ordinarily the case in the event of oxide failure, the small path to ground through NFET 122 will not be sufficient to discharge node 126 to below the switching threshold for FET's 124, and the capacitor 102 will remain substantially isolated from ground. On the other hand, if the current is transient, such as due to a transient switching condition, NFET 122 will be able to eventually discharge node 126, that is, perhaps after one or more RC time constants. When the voltage at node 126 falls to below the switching threshold for

FET's 124 this will tend to turn on FET 108 again, and de-isolate capacitor 102, that is, return the capacitor to full operation.

With the inclusion of PFET 122, the external control signal can be used to turn off FET 108, such as may be desirable for testing of the integrated circuitry (not shown) served by the decoupling capacitor. That is, if the external control signal is low, this turns on PFET 122 and turns off NFET 122. PFET 122 is sufficiently large to force NFET 124 on PFET 124 off, despite opposition by NFET 114. With PFET 124 on and NFET 124 off this turns off NFET 108.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made without departing from the spirit and scope of the invention as defined by the following claims.

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What is claimed is:

1. An apparatus for reducing disturbances on an integrated circuit, comprising:

a capacitor operatively coupled to a supply; and

control circuitry operatively coupled to the capacitor, wherein the control circuitry tends to isolate the capacitor in response to a current exceeding a certain threshold, and tends to restore the capacitor to operation if the current subsides.

2. The apparatus of claim 1, wherein the control circuitry comprises first, second and third devices, the first and second devices including control devices, and wherein the first device is switched off, to substantially isolate the capacitor, by the second device in response to a voltage produced by the excessive current, and the third device tends to discharge that voltage so the first control device is switched on again if the current subsides.

3. The apparatus of claim 2, wherein the capacitor, one of the conducting electrodes of the first control device, and the control electrode of the second control device are operatively coupled at a node, and one of the conducting electrodes of the second control device is coupled to the control electrode of the first control device, so the first control device is turned off, isolating the capacitor, by the second control device responsive to the voltage on the node; and wherein the third device includes a

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control device with a conducting electrode for discharging the node.

4. The apparatus of claim 3, wherein the second and third control devices include inverters.

5. The apparatus of claim 2, wherein the third control device includes a resistor.

6. A method for reducing disturbances on an integrated circuit, comprising the steps of:

operatively coupling a capacitor to a supply; and

substantially isolating the capacitor in response to a current exceeding a certain threshold;

restoring the capacitor to operation in response to the current subsiding.

7. The method of claim 6, in an apparatus having control circuitry with first, second and third devices, the first and second devices including control devices, the method comprising the steps of:

switching off the first device to substantially isolate the capacitor, by the second device responding to a voltage produced by the excessive current; and

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discharging the voltage by the third device so the first control device is switched on again if the current subsides.

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