

The invention relates to a circuit for decoding the vertical synchro signal in a composite video signal.

The image part of a television signal, or composite video signal, comprises, on the one hand, some information relating to the picture proper and, on the other hand, some information on synchronisation of the lines and frames. The part of the composite video signal which concerns synchronisation is termed "composite synchro". This composite synchro signal comprises some line synchronisation pulses or "signals" 10 (figures 1_a and 1_b) and, between two successive frames : some pre-equalisation pulses, the vertical synchro signal, and some post-equalisation pulses following the vertical synchro signal. The vertical synchro signal consists of a given number n of positive pulses ; the equalisation pulses, like the number of post-equalisation pulses, is equal to the same number n .

In the 625 line standard, each line synchronisation signal has a duration of 4.7 microseconds at the low level and in a single frame two line signals are separated by the duration H of one line, i.e. 64 microseconds. The number of pre-equalisation pulses is equal to five. The duration of each of these pulses 11 is half of that of a line synchronisation signal 10, i.e. 2.35 μ s, and the interval between two pre-equalisation pulses is 32 μ s. The post-equalisation pulses are also five in number having the same duration of 2.35 μ s at the low level and a separating interval of 32 μ s. The vertical synchro signal proper consists of five pulses 12 each of which has a duration of 4.7 μ s at the high level, and two successive pulses 12 are separated by a period of 32 μ s; thus the vertical synchro signal proper has a duration of 160 μ s.

The composite video signal being of the interlaced frames type, the composite synchro signal does not have the same characteristics depending on whether the frame is of even rank or of odd rank.

At the end of a frame of even rank (figure 1_a) the last line signal 10_d is separated by a half-line-period $\frac{H}{2}$, i.e. 32 μ s, from the first pre-equalisation pulse 11_p. At the start of a frame of odd rank (figure 1_a) the last post-equalisation pulse 11_d is separated by a half-line-period $\frac{H}{2}$ from the first line synchronisation signal 10_p.

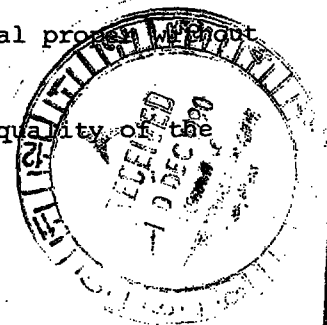
At the end of a frame of odd rank (figure 1_b) the last line synchronisation signal 10 is separated from the first pre-equalisation signal by a period H (64 μ s). At the start of a frame of even rank (figure 1_b) the last post-equalisation pulse is separated from the first line signal by a duration H, i.e. 64 μ s.

These various offsets enable it to be ensured that an odd-ranked frame starts at the beginning of a line and finishes in the middle of a line, and, conversely, that an even-ranked frame starts in the middle of a line and finishes at the end of a line; The 'salvoes of equalisation pulses are intended to put the integrator circuits, usually provided to detect the vertical synchro signals, into the same electrical state at the start of each frame whatever its rank, even or odd.

To detect the vertical synchro signal a condenser integrator is generally used the charge level of which depends on the level of the composite synchro signal. This condenser becomes charged when the composite synchro signal is at the high level and discharges when this signal is at the low level. The time constant of the condenser charging or discharging circuit is such that the latter discharges by only a very low value during the line synchronisation signals 10. In contrast it remains discharged during the vertical synchro signal. Thus the vertical synchro signal consists of a low level signal and the leading edge of this vertical synchro signal, i.e. the descending edge, is detected when the charge of the condenser descends below a given threshold. In these conditions the vertical synchro signal obtained at the output from the condenser decoding circuit is delayed in comparison with the start 15 (figure 1) of the vertical synchro signal of the composite synchro signal; this delay is the time which the condenser takes to change from its full charge to the charge which corresponds with the said threshold.

Means have been proposed (French Patent FR-A-2,443,777) the intention of which is to stabilise the delay between the decoded vertical synchro signal and the vertical synchro signal proper without however getting rid of this delay.

Such a delay is troublesome; it can affect the quality of the reproduced picture.



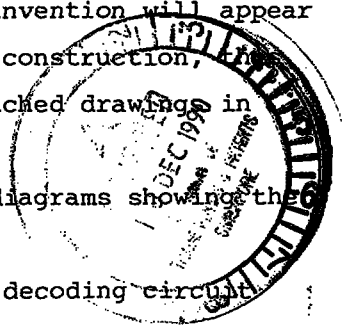
The invention remedies this disadvantage; that is to say that it provides a vertical synchro signal decoding circuit which causes practically no delay between the start of the vertical synchro signal and the start of the decoded vertical synchro signal. Furthermore, the circuit according to the invention does not call upon any signal (such as an external clock signal) other than the composite synchro signal.

To this end the circuit according to the invention is characterised in that it comprises: some digital means for producing, starting from the composite synchro signal, a first rectangular signal at half the line frequency throughout the frame, and a second rectangular signal at half the line frequency throughout the frame except during the equalisation and vertical synchro signal periods when this signal is at the line frequency, the relative phases of these two rectangular signals depending on the parity of the rank of the frame and a means for correlating these rectangular signals in order to generate a decoded vertical synchro signal the start of which coincides, practically without delay, with the start of the vertical synchro signal of the composite synchro signal.

In one embodiment the means of correlation comprises a means for generating a validation signal, or window, starting from the said rectangular signals, the start of which coincides with the trailing edge of the last pre-equalisation pulse and the end with an edge of the first postequalisation pulse, and also a digital circuit for combining the validation window with the composite synchro signal in order to generate the said decoded vertical synchro pulse.

Other characteristics and advantages of the invention will appear with the description of certain of its methods of construction, description being given with reference to the attached drawings in which:

- figures 1a and 1b, already described, are diagrams showing the composite synchro signals,
- figure 2 is a diagram, in block form, of a decoding circuit according to the invention,
- figure 3 shows a method of constructing the circuit of figure 2 and



- figures 4, 5 and 6 are diagrams illustrating the functioning of the circuit of figure 3.

The example which we shall describe in connection with figures 2 to 6 relates, like figure 1, to the 625 lines, 50 frames per second standard. However, as we shall see below, the invention is not limited to this standard.

The composite synchro signal is applied to the input of a circuit 20 for detecting signals at the frame frequency (figures 2 and 3). This circuit 20 generates the signals shown in the diagrams of figures 4b to 4i or 5b to 5i, in particular the signal T_p (figure 4i or 5i) formed by a train of pulses at the frame frequency, the number of pulses of which, at each frame, depends on the parity of the rank of this frame.

This signal T_p is used, on the one hand, by an initialisation circuit 21 enabling at each frame the other circuits of the decoder to be restored to the initial state and, on the other hand, by a circuit 22 determining the parity of the rank of the frame being analysed. In figure 2 this circuit 22 has been marked "even frame, odd frame decoding".

The signal H_c (figure 6a) generated by the circuit 22 is used by a generator 23 of a signal Q_{11} termed "validation window", and shown in figure 6i, surrounding the vertical synchro pulse (figure 1). This validation signal Q_{11} is applied to an input of a flip-flop circuit 24 enabling the vertical synchro signal to be extracted from the composite synchro signal, by means of the said window.

We refer now to figure 3. The circuit 20 for detection of signals at the frame frequency comprises two flip-flops 30 and 31 of the JK type of which the clock inputs H receive the composite synchro signal. The composite synchro signal is also applied to the input of a monostable flip-flop 32 delivering a signal Q_2 (figure 4b and 5b) consisting of a pulse of duration t_1 , 50 μ s in one example, after the appearance of a descending edge 33 (figure 4a) on its input. The output from the monostable 32 is applied to the input of a second monostable 34 of the same type as the above but imposing a delay of duration t_2 equal to 28 μ s in the example. The output signal O_4 from the monostable 34 is represented by the figure 4c or 5c.

As we shall see below with the functional description, it is sufficient for the duration t_1 to be between $\frac{H}{2}$ and H i.e. between 32 and 64 μs and for the duration $t_1 + t_2$ to be between H and $\frac{3H}{2}$ i.e. between 64 μs and 96 μs .

The output Q_4 from the monostable 34 is applied to the inputs J and K of the flip-flop 30.

Some signals of constant value, 5 volts, corresponding to a binary level 1 are applied to the inputs J and K of the flip-flop 31.

The output Q_1 from the flip-flop 30 is connected to the first input 35_1 of an exclusive OR gate 35 the second input 35_2 of which is connected to the output Q_3 of the flip-flop JK31. The output signals Q_1 and Q_3 are shown in figures 4d and 4e or 5d and 5e.

The output from the exclusive OR gate 35 is connected to the input D_1 of a D type flip-flop 36 the clock input H of which receives the composite synchro signal. The output Q_5 - shown by figures 4g or 5g - from the D type flip-flop 36 is connected, on the one hand, to the first input 37_1 of an exclusive OR gate 37 and, on the other hand, to the input D_2 of a D type flip-flop 38 the clock input H of which receives the composite synchro signal. The output Q_6 from this flip-flop 38 is connected to the second input 37_2 of the exclusive OR gate 37.

The D type flip-flop 36 is triggered by the rising edges of the pulses on its clock input while the flip-flop 38, also D type is triggered by the descending edges of the pulses on its clock input H.

The signal T_p at the output from the exclusive OR gate 37 is shown by figures 4i and 5i.

This output from the gate 37 is connected to the input of the initialisation circuit 21 which consists of two monostable flip-flops in series 39 and 40. The input of the monostable flip-flop 39 is connected to the output from the exclusive OR gate 37; it is triggered by rising edges and it imposes a delay $t_3 = 1$ millisecond. This output signal Q_7 from this flip-flop is shown by figure 6b. As we shall see below the delay t_3 may be chosen at any value between 480 microseconds and 20 milliseconds.

The output from the monostable 39 is connected to the input of the monostable 40 which is triggered by descending edges of pulses and imposes a delay t_4 of 20 microseconds. The output $\bar{Q}_8$ from the monostable 40 is shown by figure 6c. It is the $\bar{Q}_8$ output pulse which constitutes the initialisation signal for the circuit 22 for decoding the rank of the frame and the validation window generator 23.

The circuit 22 for decoding the rank of the frame comprises a D type flip-flop 41 triggered by the rising edges of pulses on its clock input H, the input D_3 of which receives the output signal Q_4 from the monostable 34. The output $\bar{Q}_9$ from this flip-flop 41 is connected to the input D_4 of another D type flip-flop 42 also triggered by the rising edges of pulses on its clock input H. The signal on the output $\bar{Q}_9$ from the flip-flop 41 is shown by figure 6g. The signal Q_{10} on the output from the flip-flop 42 is shown by figure 6h. The clock input of the flip-flop 42 receives the signal of output $\bar{Q}_8$ of the monostable 40.

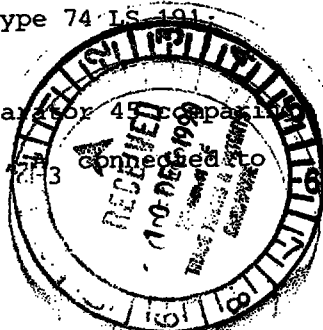
The clock input H of the flip-flop 41 receives a signal from an M/m output 43_2 of a counter 43 forming part of the validation window generator 23.

The output Q_{10} from the flip-flop 42 is connected to the first input 44_1 of an exclusive OR gate 44 the second input 44_2 of which receives the output signal T_p from the exclusive OR gate 37.

The output signal H_C from the exclusive OR gate 44 is shown by figure 6a. It is applied to the clock input H of the counter 43 forming part of the generator 23. This counter is triggered by the rising edges of pulses. Its charging input 43_1 receives the signal $\bar{Q}_8$ from the monostable 40. This counter is of the asynchronous charging type, i.e. it becomes charged so long as the pulse $\bar{Q}_8$ applied on its input 43 is at the level zero.

The counter 43 becomes charged to the value 8 dictated by the signals applied on its inputs A B C D : A = B = C = 0 and D = 1 (5 volts). The counter 43 is, in one example, of type 74 LS 191. It functions here as a count-down unit.

The generator 23 additionally comprises a comparator 45 comprising two 4-bit words having some first inputs A_0, A_1, A_2, A_3 connected to



the respective outputs Q_a , Q_b , Q_c , Q_d of the counter 43 and some second inputs B_0 , B_1 , B_2 , B_3 and also an output 45₁ emitting a 1 signal when the words on its inputs are equal, which is connected to the clock input H of a D-type flip-flop 46 also forming a part of the generator 23. The D-type flip-flop 46 is triggered by the rising edges of pulses on its clock input. It is mounted as a halver with its output $\bar{Q}_{11}$ connected to its input D_5 . The output Q_{11} is connected to the input B_1 of the comparator 45. The inputs B_0 and B_2 receive the output signal $\bar{Q}_{11}$ from the flip-flop 46. The last input B_3 of the comparator 45 is at the level zero.

The M/m output 43₂ of the counter 43 is at "0" when the content of the counter is not zero and is "1" when the content of the counter is zero. The M/m signal is shown by figure 6e.

The output signal O_{11} from the flip-flop 46 constitutes the validation window which is shown by figure 6i.

The vertical synchro signal extraction circuit 24 comprises a J-K flip-flop 47 triggered by the descending edges of pulses applied to its clock input H. This input receives the composite synchro signal while the J input is at "1" (5 volts) and the K input at "0". The zero setting input ZS receives the output signal O_{11} from the flip-flop 46 of the generator 23. The output Q_{12} from the flip-flop 47 represents the decoded vertical synchro signal. It is shown by figure 6j.

We shall now describe with reference to the diagrams of figures 4, 5 and 6 the functioning of the vertical synchro signal decoder.

Figure 4 relates to the situation represented in figure 1a, i.e. the end of an even-ranked frame and the start of an odd-ranked frame. Figure 4a is moreover identical to figure 1a. Figure 5 corresponds to the situation of figure 1b, i.e. the end of an odd-ranked frame and the start of an even-ranked frame. Figure 5a is identical with figure 1b.

Figure 6 corresponds with the situations of figures 1a and 4, i.e. the end of an even frame and the start of an odd frame.

Firstly, it will be recalled that the functioning of a J-K flip-flop is as follows: if $J = K = 0$ the Q output remains in its existing

state, even if pulses are applied to the H input. If $J = K = 1$ the output Q changes state (i.e. changes from zero to one, or from one to zero) with each descending edge of pulses applied on the input H. If $J = 0$ and $K = 1$, then $Q = 0$ after a descending edge on the H input, and if $J = 1$ and $K = 0$, $Q = 1$ is obtained after the descending edge on the H input.

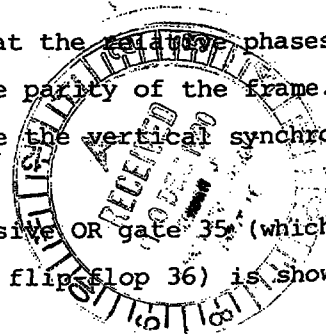
A gate of the exclusive OR type delivers a zero signal if its inputs receive identical signals. Conversely, the output from the exclusive OR gate is one if the signals on its two inputs have different values.

Taking into account the functioning of a J-K flip-flop explained above, it will be seen that the monostables 32 and 34 allow, by the choice of the delays t_1 and t_2 , some signals $J = K = 0$ to be applied which render the flip-flop 30 blind to one pulse in two when these pulses are separated by a period $H/2$, i.e. during the post and pre-equalisation periods and the period of emission of the vertical synchro signal. Thus the signal Q_1 at the output from the flip-flop 30 (figure 4d) is a rectangular signal at half-line-frequency: 7812.5 hertz and its cyclic ratio is one.

In contrast the flip-flop 31 functions permanently as a divider by two since its inputs J and K do not receive the signal Q_4 but are such that: $J = K = 1$. Thus outside the periods of equalisation and of vertical synchro signal the signal Q_3 (figures 4e and 5e) is at half-line-frequency 7812.5 hertz whereas during the periods of equalisation and of vertical synchro signal this rectangular signal has twice the frequency, i.e. the line frequency of 15625 hertz. In other words the signal Q_1 is a half-line-frequency pure spectrum signal whereas the signal Q_3 is also half-line-frequency but contains some information at frame frequency.

Comparison of the figures 4 and 5 shows that the relative phases of the signals Q_1 and Q_3 differ depending on the parity of the frame. These signals Q_1 and Q_3 are correlated to decode the vertical synchro signal.

The signal D_1 at the output from the exclusive OR gate 35 (which also constitutes the signal at the input of the flip-flop 36) is shown



by figures 4f and 5f. This signal D_1 always has the same value, "zero" or "one", throughout the frame duration except during the equalisation and vertical synchro signal periods in which it varies at half-line frequency. A comparison of figures 4f and 5f shows that at the end of an even-ranked frame and at the start of an odd-ranked frame (figure 4f) the number of half-periods at the half-line frequency of the signal D_1 is greater by one than the corresponding number of the same signal D_1 at the end of an odd-ranked frame and at the start of an even-ranked frame (figure 5f). The D-type flip-flop 38 and the exclusive OR gate 37 make use of this difference to generate a signal T_p at the output from the gate 37 which comprises eight pulses in the first case (end of an even frame, start of an odd frame) and seven pulses in the second case (end of an odd frame, start of an even frame). Furthermore, the D-type flip-flop 36 enables disturbances to be eliminated from the signal D_1 which are due to the simultaneity of the switching of the signals on the inputs 35_1 and 35_2 of the exclusive OR gate 35.

In order clearly to understand the functioning of this part of the circuit 20 it will be recalled that a D-type flip-flop is such that the input D is transferred to the output Q when a rising edge (flip-flop 36) is applied on its clock input H or, for other types of flip-flops (38), when it is a descending edge which is applied to the clock input.

Thus, by the "exclusive OR" combination of the signals Q_5 and Q_6 , eight T_p pulses are obtained in the case of figure 4i and seven T_p pulses in the case of figure 5i. These pulses are always positive. They appear as soon as the composite synchro signal appears.

We see in figure 4i that: the first pulse of the train T_p appears between the start of the first pre-equalisation signal and the start of the second pre-equalisation signal; the second pulse of the train T_p is situated between the end of the third pre-equalisation signal and the start of the fourth pre-equalisation signal; the third pulse of the train T_p appears between the end of the fifth pre-equalisation signal and the start of the vertical synchro signal; the fourth and fifth pulses of train T_p correspond respectively to the second and

fourth pulses of the vertical synchro signal; the sixth pulse of the train T_p corresponds to the space between the end of the first post-equalisation signal and the second post-equalisation signal; the seventh pulse of train T_p is situated between the end of the third post-equalisation pulse and the start of the fourth post equalisation pulse; and, lastly, the eighth pulse of the train T_p coincides with the space between the end of the fifth post-equalisation signal and the start of the following line signal.

We see in figure 5i that: the first pulse of the train T_p is situated between the end of the second pre-equalisation signal and the start of the third signal of the same period; the second pulse of this train appears between the end of the fourth pre-equalisation signal and the start of the fifth signal; the third, fourth and fifth pulses coincide with respectively the first, third and fifth pulses of the vertical synchro signal; the sixth pulse of the train T_p appears between the end of the second post-equalisation signal and the start of the third post-equalisation signal; and, lastly the seventh pulse of train T_p of figure 5i is situated between the end of the fourth post-equalisation signal and the start of the fifth signal of the same period.

The monostable 39 of the initialisation stage 21 produces a positive pulse Q_7 (figure 6b) of duration $t_3 = 1$ millisecond at the time of the first rising edge of the T_p signal.

The duration t_3 must meet the following conditions: it must be greater than the duration of the T_p pulses, i.e. greater than 480 microseconds, and less than one frame period, i.e. 20 milliseconds.

The descent edge of the pulse Q_7 triggers the monostable 40 which generates a negative pulse of duration t_4 equal to 20 microseconds on the output $\overline{Q}_8$. This pulse $\overline{Q}_8$ constitutes the initialisation pulse used to trigger (through the input 43₁) the charging of the counter and to determine, through the flip-flop 42 of the stage 22, the charging level - 7 or 8 - of this counter 43.

The stage 22 makes use of the signals T_p , $\overline{Q}_8$, Q_4 and M/m (figure 6e) to generate a signal H_C (figure 6a), applied to the clock input H of the counter 43 of the stage 23, which will determine whether the

said counter 43 will perform a count-down from 8 to 0 or from 7 to 0, i.e. will determine the rank of the frame.

When the rising edge of the M/m pulse arrives while there is no positive pulse Q_4 (figure 6f) on the input D_3 , the output Q_9 adopts the value 0 and therefore $\overline{Q}_9$ the value 1 (figure 6g).

At the output Q_{10} of the D-type flip-flop 42 a signal is obtained (figure 6h) of frequency 25 hertz and of cyclic ratio 1. The combination of this signal Q_{10} with the signal T_p by the exclusive OR 44 supplies the signal H_C (figure 6a). If the first input 44_1 of the exclusive OR gate 44 is at zero the signal H_C is, as in the example of figure 6, formed of positive pulses identical to the pulses T_p ; conversely if the input 44_1 of the gate 44 (i.e. the signal Q_{10}) has the value "one", the signal H_C corresponds to the signal T_p but is formed of negative pulses.

When a negative pulse $\overline{Q}_8$ (figure 6c) is applied to the input 43_1 of the counter 43 of the validation window generator stage 23, the counter 43 becomes charged to the value 8. This charging lasts so long as the pulse $\overline{Q}_8$ is at the level 0. When the signal $\overline{Q}_8$ returns to the value "1", the signal Q_{10} applied on the input 44_1 of the exclusive OR gate 44 of the stage 22 takes the value "1" in the example shown in figure 6 or "0" for another frame. If the signal Q_{10} is at the level "0" the output signal H_C of the gate 44, applied to the clock input of the counter 43, remains at zero and this counter remains charged to the value 8. But if the signal Q_{10} on the input 44_1 of the gate 44 is at "one" the output from this gate changes to "1"; this results in a rising transition on the clock input H of the counter 43 which causes it to change over from the state 8 to the state 7; it remains in this state so long as no pulses are applied to its clock input.

The pulse $\overline{Q}_8$, simultaneously with the charging of the counter 43, resets the D-type flip-flop 46 of the stage 23 which is mounted as a halver. When this zero setting is performed the output Q_{11} (figure 6i) is at "zero" and the output $\overline{Q}_{11}$ at "one". In these conditions the inputs B_0 , B_1 , B_2 and B_3 of the comparator 45 receive the following signals :

$$B_0 = B_2 = \overline{Q}_{11} = 1,$$

$$B_1 = Q_{11} = 0,$$

$$B_3 = 0;$$

in other words, on the inputs B_0, B_1, B_2, B_3 of the comparator 45 is applied the binary number 0101, i.e. 5 in decimal (B_3 is the heaviest bit).

Thus when the counter 43, starting from the value 8 or 7, starts to count down it passes through the value 5; at this moment the output 45_1 of the comparator 45 supplies a positive pulse which causes the output Q_{11} of the flip-flop 46 to change over from the 0 state to the 1 state and the $\overline{Q}_{11}$ output from the 1 state to the 0 state, as shown in figures 6d and 6i. Thus the binary number 0010, i.e. 2 in decimal, is then applied to the B inputs of the comparator 45.

When the content of the counter then reaches the value 2 the output 45_1 of the comparator 45 applies a positive pulse to the clock input of the flip-flop 46 and the output Q_{11} reverts to zero and the output $\overline{Q}_{11}$ changes back to "1" (figure 6d and 6i).

The output Q_{11} , which remains in the "1" state when the content of the counter is between 5 and 2, constitutes a validation window.

When the content of the counter 43 reaches the value zero the M/m signal (figure 6e) at output 43_2 changes from zero to one, which causes the output $\overline{Q}_9$ (figure 6g) of the flip-flop 41 of the stage 22 to change to the value one; thus the phase of the counter clock signal is changed depending on the rank of the frame and this counter 43 is prepared to count down.

It is the output Q_{12} of the flip-flop 47 which delivers the decoded vertical synchro signal (figure 6i). To understand the functioning of this final stage 24 it will be recalled that when a J-K flip-flop receives a 0 signal on its zero setting ZS input, its output Q remains on zero whatever the values of the signals on its other inputs J, K and H. Conversely when the ZS input of a flip-flop receives a level one signal and when $J = 1$ and $K = 0$ the output Q takes the value 1 as soon as a descending edge appears on the clock input H.

Thus the output Q_{12} changes to 1 as soon as the first descending edge of the composite synchro signal appears. There is therefore a negligible delay between the start of the decoded vertical synchro signal Q_{12} and the start of the vertical synchro signal of the composite synchro signal. This negligible delay is of a few nanoseconds; it is the propagation time in the flip-flop 47.

The invention applies not only to the 625 line standard but also to the 525 line standard in which six pre-equalisation pulses are provided, six pulses in the vertical synchro signal, and six pulses in the post-equalisation period whereas in the 625 line standard this number is five. One may, for this 525 line standard, use the arrangement of figure 3 with some minor changes: the counter 43 is charged to the value 9; the validation window appears between the contents 6 and 3 (instead of 5 and 2) and the clock of the counter is reversed before the charging.

C L A I M S

1. Circuit for decoding the vertical synchro signal of a composite synchronisation signal using interlaced frames, the vertical synchro signal comprising n positive pulses preceded by n negative pre-equalisation pulses and followed by n negative post-equalisation pulses, these pulses of the vertical synchro and equalisation signal appearing at a frequency which is twice the scanning frequency of the lines, characterised in that it comprises some digital means for producing, starting from the composite synchronisation signal, a rectangular signal (Q_1) at the half-line-frequency, and a rectangular signal (Q_3) at half-line-frequency during the frame except during the equalisation periods and the vertical synchro signal period when this signal (Q_3) is at the line frequency, the relative phases of these two rectangular signals depending on the parity of the rank of the frame, and a means (20, 22, 23, 24) for correlating these rectangular signals (Q_1 , Q_3) in order to generate a decoded vertical synchro signal the start of which coincides, practically without delay, with the start of the vertical synchro signal of the composite synchronisation signal.

2. Circuit according to claim 1, characterised in that the means (23, 24) for correlating the rectangular signals (Q_1 , Q_3) comprise a means (23) for generating a validation signal, or window, (Q_{11}) starting from the said rectangular signals (Q_1 , Q_3), the start of which coincides with the trailing edge of the last pre-equalisation pulse and the end with an edge of the first post-equalisation pulse, and a digital circuit (24) for combining the validation window with the composite synchronisation signal in order to generate the said decoded vertical synchro signal.

3. Circuit according to claim 2, characterised in that the circuit (24) for combining the validation signal with the composite synchronisation signal comprises a J-K type flip-flop (47) on the zero setting input of which is applied the validation signal (Q_{11}) and to the inputs J and K of which are applied signals having the respective values 1 and 0, the clock input (H) receiving the composite synchronisation signal.



4. Circuit according to claim 1, 2 or 3, characterised in that it comprises a means (20) making use of the different relative phase shifts between the rectangular signals (Q_1 and Q_3) depending on the parity of the rank of the frame to produce a train of pulses (T_p) appearing only during the pre- and post-equalisation periods and the frame period, such that the number of pulses and the moments of their appearance depend on the parity of the rank of the frame.

5. Circuit according to claims 2 and 4, characterised in that it comprises, to generate the validation window (Q_{11}), a counter (43) charged at each frame with a number (N) which corresponds to the largest number of the pulses of the said train (T_p), the pulses of this train (T_p) controlling the count-down of the content of this counter (43), some means (45 and 46) being provided for generating the validation signal when the content of the counter is between a first value (5) less than N , and a second value (2) less than the first but greater than zero.

6. Circuit according to claim 5, characterised in that it comprises a comparator (45) on the first input (A_0, A_1, A_2, A_3) of which is applied the output signal (Q_a, Q_b, Q_c, Q_d) of the counter (43) and the second input (B_0, B_1, B_2, B_3) of which depends on the state of a flip-flop (46) receiving the output signal (45_1) from the comparator (45) in order for this signal on the second input to be equal in turn to the said first and second values.

7. Circuit according to claim 5 or 6, characterised in that, to allow charging of the counter (43) to a value which depends on the parity of the rank of the frame, it comprises some means (41, 42, 44) for generating a signal (H_c) to control the counting down of the content of the counter (43) which, for a frame having a rank of given parity, is identical with the pulse train signal (T_p) and for a frame the rank of which is of the other parity, consists of pulses of opposite sign from that of the said train (T_p).

8. Circuit according to any of the above claims, characterised in that to generate the first rectangular signal (Q_1) at half-line-frequency it comprises a flip-flop (30) mounted as a frequency halver and a means (such as some monostables (32, 34), of delaying the



composite synchronisation signal which generates a signal (Q_4) inhibiting this flip-flop for one pulse in two during the equalisation periods and the vertical synchro signal period.

9. Circuit according to claim 8, characterised in that the said flip-flop generating the first rectangular signal (Q_1) is a J-K type flip-flop the clock input (H) of which receives the composite synchronisation signal and the J and K inputs of which are connected to the output from the means of delay (32, 34).

10. Circuit according to any of the above claims, characterised in that the means for generating the second rectangular signal (Q_3) comprises a flip-flop (31) such as a J-K flip-flop mounted as a frequency halver.

11. Circuit according to claim 4, characterised in that, to combine the two rectangular signals (Q_1 and Q_3) so as to produce the said train of pulses (T_p) containing a number of pulses which depends on the parity of the rank of the frame, it comprises a first gate (35) of the exclusive OR type the inputs (35_1 , 35_2) of which receive the said respective rectangular signals (Q_1 , Q_3), a D-type flip-flop (38) the clock input of which receives the composite synchronisation signal and the data input (D_2) of which receives the signal coming from the first exclusive OR gate (35), and a second exclusive OR gate (37) the first input (37_2) of which receives the output signal (Q_6) from the D-type flip-flop (38) and the second input (37_1) of which receives a signal representing the output from the first exclusive OR gate (35).

12. Circuit according to claim 11, characterised in that the signal applied to the second input (37_1) of the second exclusive OR gate (37) and to the data input (D_2) of the D-type flip-flop (38) is supplied by the output (Q_5) of another D-type flip-flop (36) the data input (D_1) of which is connected to the output from the first exclusive OR gate (35) and the clock input (H) of which receives the composite synchronisation signal.

