

semiconductor memory or the like, does not damage the chip electrodes, has a wide range of bonding energy conditions, has a low specific resistance, and has a low material cost. Further, the issue is solved by providing a manufacturing method of the bonding wire and a semiconductor wire bonding structure and a semiconductor device using the bonding wire.

[0021] In order to solve the above-described wedge bonding problems, the present inventors found out that controlling a compressive stress of the wire is effective as a result of the conclusion reached through diligent research and trials and errors with the bonding wire. The compressive stress is the value of strength (force) per unit area when the wire is deformed by receiving force in a compressing direction, and they found out in the present invention that the issue can be solved as long as the compressive stress when the wire is compressed (deformed) by 60% with respect to the wire diameter is in a range of 290 MPa or more and 590 MPa or less.

[0022] Details of the method of measuring the compressive stress of the present invention will be described in paragraphs [0050] to [0053] to be described later, but the compressive stress is calculated from the following equation.

[0023] Wire compressive stress (MPa) = Force applied at 60% deformation with respect to a wire diameter (N) / (Circumference ratio $\times$ Wire diameter (mm) / 2) $\times$ Indenter diameter (mm)

Incidentally, as the compressive stress, a value automatically calculated by a compression testing machine may be used. The indenter diameter is the diameter of the indenter attached to the compression testing machine. As the circumference ratio, 3.14 is used.

[0024] As a basic idea of the present invention, the present inventors have focused on a wire structure in which Ag or Cu wires are used mainly and surfaces of these wires are coated with soft Au under the condition that the above-described compressive stress falls within the range, the specific resistance is low, and the cost is low.

[0025] According to a first aspect of the present invention, there is provided a gold-coated bonding wire including: a core material containing silver or copper as a main component; and a coating layer that is provided on a surface of the core material and

contains gold as a main component, in which a compressive stress when the gold-coated bonding wire is deformed by 60% with respect to a wire diameter is 290 MPa or more and 590 MPa or less.

[0026] According to a second aspect of the present invention, there is provided a method of manufacturing a gold-coated bonding wire, the gold-coated bonding wire including: a core material containing silver or copper as a main component; and a coating layer that is provided on a surface of the core material and contains gold as a main component, the manufacturing method including: setting a compressive stress when the gold-coated bonding wire is deformed by 60% with respect to a wire diameter to 290 MPa or more and 590 MPa or less when deformed by 60% with respect to a wire diameter.

[0027] According to a third aspect of the present invention, there is provided a semiconductor wire bonding structure including: a gold-coated bonding wire including: a core material containing silver or copper as a main component; and a coating layer containing gold as a main component; an electrode of a semiconductor chip; and a wedge bonding portion where the wire and the electrode are bonded, in which a film thickness of the coating layer is 5 nm or more and 200 nm or less, and the gold-coated bonding wire has a compressive stress of 290 MPa or more and 590 MPa or less when deformed by 60% with respect to a wire diameter.

[0028] According to a fourth aspect of the present invention, there is provided a semiconductor device including: one or a plurality of semiconductor chips, the semiconductor chip including at least one first electrode; a circuit substrate that is selected from a lead frame and a circuit board including at least one second electrode; and a gold-coated bonding wire that electrically connects at least one selected from between the first electrode of the semiconductor chip and the second electrode of the circuit substrate and between the first electrodes of a plurality of the semiconductor chips and is wedge-bonded to at least one of the first electrode and the second electrode or one of a plurality of the first electrodes, in which the gold-coated bonding wire includes: a core material containing silver or copper as a main component; and a coating layer that is provided on a surface of the core material and contains gold as a main component, and a compressive stress of the

gold-coated bonding wire is 290 MPa or more and 590 MPa or less.

EFFECT OF THE INVENTION

[0029] According to embodiments of the gold-coated bonding wire and the manufacturing method thereof of the present invention, by setting the compressive stress to 290 MPa or more and 590 MPa or less, a stable wedge bonding strength can be obtained without damaging semiconductor chip electrodes and the like, even in the case of continuous wedge bonding where the bonding energy condition varies depending on individual bonding points such multistage stacked chip electrodes. Further, according to embodiments of the semiconductor device of the present invention, the use of such a gold-coated bonding wire makes it possible to provide an inexpensive, thin, and large storage capacity semiconductor memory, and the like with a reduced total cost.

[0030] In addition to the above effects, embodiments of the present invention are naturally effective in bonding stability, bonding reliability, and the like in ball bonding to ordinary semiconductor chip electrodes and wedge bonding to substrate circuits, lead frames, and the like.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] [FIG. 1] FIG. 1 is a vertical cross-sectional view illustrating a gold-coated bonding wire in an embodiment.

[FIG. 2] FIG. 2 is a cross-sectional view illustrating the gold-coated bonding wire in the embodiment.

[FIG. 3] FIG. 3 is a vertical cross-sectional view illustrating a modified example of the gold-coated bonding wire in the embodiment.

[FIG. 4] FIG. 4 is a cross-sectional view illustrating the modified example of the gold-coated bonding wire in the embodiment.

[FIG. 5] FIG. 5 is a view illustrating an indentation shape in a compressive stress test of the bonding wire in the embodiment.

[FIG. 6] FIG. 6 is a cross-sectional view illustrating a stage of a semiconductor

CLAIMS

1. A gold-coated bonding wire, comprising:
a core material containing silver or copper as a main component; and
a coating layer provided on a surface of the core material, the coating layer containing gold as a main component, wherein
the gold-coated bonding wire has a film thickness of the coating layer of 5 nm or more and 200 nm or less, and
the gold-coated bonding wire has a compressive stress of 290 MPa or more and 590 MPa or less when deformed by 60% with respect to a wire diameter.
2. The gold-coated bonding wire according to claim 1, wherein
the core material has a Vickers hardness (Hv) of 40 or more and 80 or less in a cross section thereof.
3. The gold-coated bonding wire according to claim 1 or claim 2, wherein
the core material is made of a silver alloy containing 97 mass% or more of silver and contains at least one metal selected from the group consisting of copper, calcium, phosphorus, gold, palladium, platinum, nickel, rhodium, indium, and iron in the range of 1 mass ppm or more and 3 mass% or less with respect to the total amount of the wire.
4. The gold-coated bonding wire according to claim 1 or claim 2, wherein
the core material is made of a copper alloy containing 98 mass% or more of copper and contains at least one metal selected from the group consisting of phosphorus, gold, palladium, platinum, nickel, silver, rhodium, indium, gallium, and iron in the range of 1 mass ppm or more and 2 mass% or less with respect to the total amount of the wire.

5. The gold-coated bonding wire according to any one of claims 1 to 4, wherein
the gold-coated bonding wire has a diameter of 13 μm or more and 35 μm or less.
6. The gold-coated bonding wire according to any one of claims 1 to 5, further comprising:
an intermediate metal layer provided between the core material and the coating layer, the intermediate metal layer containing one metal selected from the group consisting of palladium, platinum, and nickel as a main component.
7. The gold-coated bonding wire according to claim 6, wherein
the intermediate metal layer has a thickness of 60 nm or less.
8. The gold-coated bonding wire according to any one of claims 1 to 7, being
for semiconductor memory.
9. A method of manufacturing a gold-coated bonding wire, the gold-coated bonding wire including:
a core material containing silver or copper as a main component; and
a coating layer provided on a surface of the core material, the coating layer containing gold as a main component, the method comprising:
setting a film thickness of the gold-coated bonding wire to 5 nm or more and 200 nm or less; and
setting a compressive stress to 290 MPa or more and 590 MPa or less when deformed by 60% with respect to a wire diameter.
10. A semiconductor wire bonding structure, comprising:
a gold-coated bonding wire including:

a core material containing silver or copper as a main component; and
a coating layer containing gold as a main component;
an electrode of a semiconductor chip; and
a wedge bonding portion where the wire and the electrode are bonded, wherein
the coating layer has a film thickness of 5 nm or more and 200 nm or less, and
the gold-coated bonding wire has a compressive stress of 290 MPa or more and
590 MPa or less when deformed by 60% with respect to a wire diameter.

11. The semiconductor wire bonding structure according to claim 10, further comprising:

two or more of the semiconductor chips; and
two or more of the wedge bonding portions where the electrodes of the two
semiconductor chips and the wire are connected in sequence.

12. The semiconductor wire bonding structure according to claim 10 or claim
11, being for semiconductor memory.

13. A semiconductor device, comprising:

one or a plurality of semiconductor chips, the semiconductor chip including at
least one first electrode;

a circuit substrate that is selected from a lead frame and a circuit board including
at least one second electrode;

a gold-coated bonding wire configured to electrically connect at least one selected
from between the first electrode of the semiconductor chip and the second electrode of the
circuit substrate and between the first electrodes of a plurality of the semiconductor chips;
and

a wedge bonding portion where the first electrode or the second electrode and the
gold-coated bonding wire are bonded, wherein

the gold-coated bonding wire includes:

a core material containing silver or copper as a main component; and

a coating layer provided on a surface of the core material, the coating layer having a film thickness of 5 nm or more and 200 nm or less, the coating layer containing gold as a main component, and

the gold-coated bonding wire has a compressive stress of 290 MPa or more and 590 MPa or less when the gold-coated bonding wire is deformed by 60% with respect to a wire diameter.

14. The semiconductor device according to claim 13, further comprising:

a plurality of the semiconductor chips each including at least the single first electrode, wherein

the plurality of the semiconductor chips are stacked to make each of the first electrodes exposed, the semiconductor device further comprising:

two or more of the wedge bonding portions where the first electrodes of a plurality of the semiconductor chips are connected by the gold-coated bonding wire in sequence.

15. The semiconductor device according to claim 13 or claim 14, being for

semiconductor memory.