

# **SEMICONDUCTOR PACKAGE ASSEMBLY AND MANUFACTURING METHOD**

## **ABSTRACT**

Disclosed in the embodiments of the disclosure are a semiconductor package assembly and a manufacturing method. The semiconductor package assembly includes: a base plate, having a first surface; a chip stacking structure, located on the base plate, where the chip stacking structure includes a plurality of chips sequentially stacked in a direction perpendicular to the base plate, and is electrically connected to the first surface of the base plate; an interposer, located on the chip stacking structure and having a first interconnection surface, where the first interconnection surface has a first interconnection region and a second interconnection region, and the first interconnection region is electrically connected to the base plate; and a molding compound, sealing the chip stacking structure, the interposer and the first surface of the base plate. The first interconnection region is not sealed by the molding compound, and the second interconnection region is sealed by the molding compound. There is a preset height between a top surface of the molding compound on the second interconnection region and the first interconnection region.

[Fig. 1]