Circuit Board

FIELD OF THE INVENTION

The present invention relates broadly to a method of forming a circuit board, and to a circuit board.

BACKGROUND

The demand for advanced electronic systems in e.g. front-end wireless communication and the increased use of the Internet has resulted in miniaturization of electronic products having more functional features. These products use a large number of passive components (e.g. resistors, capacitors and inductors). In conventional printed circuit boards, these passive components are surface mounted devices, which consume a large area thereby increasing costs. Passive components generally may take up to 60% of the printed circuit board (PCB) area thereby limiting the space available for active components (e.g. integrated circuits (IC))

On the other hand, passive components, such as bypass capacitors are generally placed as close as possible to a die or IC to increase the effectiveness of the capacitors. These capacitors and other passive components are thus often surface mounted to the die side or on the opposite side of an IC during printed circuit board assembly. Fig. 1 illustrates a cross-section of a conventional multi-layer printed circuit board assembly 10 having an IC 11, capacitors 12 located on the die side and capacitors 13 located on the opposite side of the die. The terminals of the capacitors 12, 13 are internally connected to the integrated circuit through pads 9, vias 14, and power or ground lines 15, 16.

Reducing the dimensions of the passive components may help in mounting a large number of such passive components. However, reducing the dimensions of the surface mounted passive components has an adverse effect on the electrical performance.

An alternative that is currently practiced for selected applications is embedded passive components using screen printed inks. Commonly used materials include capacitor paste and resistor inks. The density of capacitance that can be achieved using commercially available printed paste is insufficient to meet a wide range of

capacitance requirements that is readily available using discrete capacitors. Printed resistor inks have poor resistance tolerance of up to 30%. In such instances, laser trimming may be used for precise resistance tolerance control for selected applications which increases costs.

Japanese Publication No. 2002261449 published on 13 September 2002 in the names of SEIICHI *et al.* describes a method of embedding IC chips and discrete passive components by using a proprietary epoxy resin material. Interconnections between the ICs and passive components are formed by vias, which are composed of a conductive resin. The use of proprietary material and via forming process in commercial applications increases costs.

United States Patent No. 6,407,929 B1 issued on 18 June 2002 to AARON *et al.* relates to embedding discrete passive components by a lamination process. Interconnections are formed after the lamination process by drilling holes right above the component terminals and filling the holes with a conductive material.

United States Patent Publication No. 2004/0001324 A1 published on 1 Jan 2004 in the names KWUN *et al.* describes a method of embedding IC chips in a through-hole cavity and discrete passive components in a PCB recess (partially formed cavity). A dielectric epoxy material is filled in the cavities, and once the epoxy is cured interconnections are formed by vias formed in the cured epoxy over the component terminals.

International (PCT) Publication No. 2004/001848 A1 pertains to a lamination process for embedding IC or discrete passive components in a PCB with cavity formed on prepreg sheets to fit the components. Interconnection are formed by drilling holes right above the component terminals and electroplating.

There are a number of concerns relating to the processes of embedding discrete passive components in the above documents. For instance, drilling holes for vias above the component terminals may introduce thermal/mechanical damage or removal of termination material. Electroplating the drilled vias over component's solder terminal may not be feasible due to concern of plating adhesion to solder surface.

It is with the knowledge the above concerns that the present invention has been conceived and is now reduced to practice.

SUMMARY

In accordance with a first aspect of the present invention there is provided a method of forming a circuit board, the method comprising mounting at least one passive component on a first surface of a first laminate material; interconnecting the passive component to contact traces and vias of the first laminate material; and attaching a second laminate material to the first surface of the first laminate material utilising a lamination process, the second laminate material sheet having at least one of a recess, a through-hole or both formed therein for accommodating the passive component in the second laminate.

The passive component may be directly interconnected to the contact traces and vias.

The passive component may be substantially vertically interconnected to the contact traces and vias with respect to a surface plane of the first laminate material.

The attaching of the second laminate material may utilise the lamination process comprises providing a dielectric material between the first and second laminate materials.

The dielectric material may comprise one or more prepreg sheets.

The mounting of the passive component may comprise forming mounting pads on the first laminate material.

The interconnecting of the passive component may comprise providing vias in the mounting pads.

The method may further comprise mounting one or more integrated circuits (ICs) on a second surface of the first laminate material in an area substantially above individual or a cluster of the passive components.

The second laminate material may comprise contact traces for forming a multi-layered circuit board.

The method may further comprise attaching one or more further laminate materials having contact traces formed thereon to the first and second laminate materials for forming a multi-layered circuit board.

The method may comprise attaching a resin coated metal material to the first and second laminate materials for forming a multi-layered circuit board.

The laminate materials may comprise organic laminate materials.

In accordance with a second aspect of the present invention there is provided a circuit board comprising a first laminate material comprising contact traces and vias; at least one passive component mounted on a first surface of the first laminate material; interconnections formed from the passive components to the contact traces and vias of the first laminate material; and a second laminate material sheet laminated to the first surface of the first laminate material having at least one of a recess, a through-hole or both formed therein for accommodating the passive component.

The passive component may be directly interconnected to the contact traces and vias.

The passive component may be substantially vertically interconnected to the contact traces and vias with respect to a surface plane of the first laminate material.

The board may comprise a dielectric sheet between the first and second laminate materials.

The dielectric material may comprise one or more prepreg sheets.

The board may comprise mounting pads on the first laminate material for the passive component.

The board may comprise vias in the mounting pads for interconnecting the passive component to the traces.

The board may further comprise one or more integrated circuits (ICs) mounted on a second surface of the first laminate material in an area substantially above individual or a cluster of the passive components.

The second laminate material sheet may comprise contact traces.

The board may further comprise one or more further laminate materials having contact traces formed thereon and attached to the first and second laminate materials.

The board may further comprise a resin coated metal material attached to the first and second laminate materials for.

The laminate materials may comprise organic laminate materials.

BRIEF DESCRIPTION OF THE DRAWINGS

Non-limiting embodiments of the invention are described hereinafter with reference to the drawings, in which:

Fig. 1 shows a schematic cross-sectional view of a conventional printed circuit board assembly with integrated chip and passive components;

Figs. 2A-2H show schematic cross-sectional views illustrating the process flow for fabricating embedded passive components in a printed circuit board assembly according to an embodiment of the present invention; and

Fig. 3 is a schematic bottom view of Fig. 2B.

DETAILED DESCRIPTION

In an example embodiment, discrete components are embedded away from the surface area of a printed circuit board. An organic core material of small thickness is fabricated using an established fabrication process. The fabricated core material in the example embodiment is designed on a two-layer printed circuit laminate having signal and ground connections which are connected by passive components mounted on mounting pads. A direct vertical connection is provided by vias formed in the mounting pad. The passive components are surface mounted on the core material and are so located as to form a group or cluster.

A second laminate material has a cavity which is formed by punching or routing. The surface area of the cavity is larger than the cluster area formed on the core material. The thickness of the second laminate is chosen to be greater than that of the discrete component in the example embodiment, so as to embed the passive components in the final assembly. The core material and second laminate material are sandwiched together and the cluster of passive components is enclosed by the cavity with a desired clearance.

The core and second laminate materials may be sandwiched using established printed circuit lamination process employing heating and pressing. A prepreg sheet of multiple layers is provided between the core and second laminate materials in the example embodiment prior to laminating the PCB assembly. The above process can be repeated for fabricating a multi-layered printed circuit board.

The cavity of the laminated printed circuit board is filled and planarized with a resin of the prepreg sheet thereby forming embedded components within the printed circuit board. The external surface area of the laminated board is free from passive components. This surface area can be used for mounting other electronic components. An integrated circuit is subsequently mounted directly above the cavity

area in the example embodiment, to form electrical connections with embedded passive components (such as bypass capacitors).

Figs. 2A to 2H illustrate the detailed process flow of forming embedded passive components in a PCB according to the example embodiment of the present invention. The manufacturing steps are as follows:

Referring to Fig. 2A, a two-layer organic laminate 17 having conductive patterns (such as copper) 15 and 16 is provided with mounting pads 9 on a bottom side of the laminate 17 for assembling passive components. The material of the organic laminate 17 can be standard PCB materials, such as FR-4 epoxy glass, polyimide, benzocyclobutene, teflon, cyanate ester, bismeleimide triazine, other epoxy resins, or the like, or combinations of those materials. The thickness of the laminate 17 is so chosen to balance between mechanical stability and proximity of the passive components to an IC. The mounting pads 9 are directly and vertically (with respect to the plane of the laminate 17 taken as a horizontal plane) connected to power or ground connections 15, 16, by via-in-pads, e.g. 14, in the example embodiment.

Referring to Fig. 2B, discrete passive components e.g. 13, are surface mounted on the pads 9 and in the example embodiment soldered using a reflow process. Thin profile (height) discrete passive components may be used to produce a low profile PCB in the example embodiment. The passive components can be tested at this stage.

Referring to Fig. 2C, a second laminate material 19 having a thickness (e.g. 0.1~0.2 mm) slightly larger than the height of the passive components e.g. 13 is placed adjacent to the first laminate material 17. The laminate material 19 has conductive patterns, e.g. 28, 30, formed on both sides. By punching or routing, a cavity 8 is provided in the second laminate material 19, and disposed directly below the passive components 13 of the laminate material 17. The area of the cavity 8 is slightly larger than the cluster area of the components e.g. 13 formed on the first laminate material 17. A multi-layered prepreg sheet 18 is placed between the core laminate material 17 and the second laminate material 19 in the example embodiment, prior to the lamination process. The number of prepreg sheets is dependent on the thickness of the second laminate material 19 and the number of passive components e.g. 13.

Referring to Fig. 2D, a multi-layered printed circuit lamination is formed in the example embodiment by adding another pair of a prepreg sheet 20 and a laminate material 21. The laminate material 21 has conductive patterns formed on the upper side. The process can be repeated depending on the number of printed circuit board layers required. In another embodiment, resin coated copper (RCC) foil may be used instead of the pair of the prepreg sheet 20 and the laminate material 21.

Referring to Fig. 2E, a multi-layered PCB in the example embodiment with embedded discrete components e.g. 13 is formed by a lamination process by appropriate heating and pressing of the top and the bottom surfaces of the structure formed in the previous step.

Referring to Fig. 2F, laminated assembly 22 is completed with embedded passive components.

Referring to Fig. 2G, through via holes 23 are formed and plated to form connections between the top, bottom and internal layers. The via holes 23 may be formed by drilling (e.g. mechanical or laser drilling)The top and bottom surfaces of the laminated assembly 22 (Figure 2F) are further processed by known etching methods in the example embodiment to provide metal pads 24, 25 for component surface mounting, thereby forming the final PCB 26 having embedded discrete components e.g. 13.

Referring to Fig. 2H, an IC 27 is surface mounted on top of the PCB 26. The embedded passive components e.g. 13 are electrically connected to the IC 27. Other components may be mounted on the top or bottom layers of PCB 26.

Fig. 3 is the bottom view of the passive component assembly shown in Fig. 2B, illustrating a cluster area 28 of the passive components e.g. 13, in the example embodiment.

The example embodiment makes use of known component assembly processing and printed circuit fabrication steps. By embedding passive components such as bypass capacitors, more surface area on top and bottom layers may be available for mounting other electronic components. This results in increased functional features and reduced PCB size.

The example embodiment also provides a less inductive interconnection between the embedded passive components, e.g. capacitors, which, in turn, increases the self-resonant frequency and extends the decoupling frequency range in broadband applications. The example embodiment facilitates increased routing space on the signal layers by direct vertical interconnection, in conjunction with co-location of the passive components with associated, surface mounted components such as ICs.

It will be appreciated by a person skilled in the art that numerous variations and substitutions may be made to the embodiments described without departing from the spirit or scope of the present invention. The example embodiments are, therefore, to be regarded as illustrative only, and not restrictive on the scope of protection sought.

CLAIMS:

1. A method of forming a circuit board, the method comprising

mounting at least one passive component on a first surface of a first laminate material;

interconnecting the passive component to contact traces and vias of the first laminate material; and

attaching a second laminate material to the first surface of the first laminate material utilising a lamination process, the second laminate material sheet having at least one of a recess, a through-hole or both formed therein for accommodating the passive component in the second laminate.

2. The method as claimed in claim 1, wherein the passive component is directly interconnected to the contact traces and vias.

3. The method as claimed in claims 1 or 2, wherein the passive component is substantially vertically interconnected to the contact traces and vias with respect to a surface plane of the first laminate material.

4. The method as claimed in claims 1 or 2, wherein the attaching of the second laminate material utilising the lamination process comprises providing a dielectric material between the first and second laminate materials.

5. The method as claimed in claim 4, wherein the dielectric material comprises one or more prepreg sheets.

6. The method as claimed in claims 1 or 2, wherein the mounting of the passive component comprises forming mounting pads on the first laminate material.

7. The method as claimed in claim 6, wherein the interconnecting of the passive component comprises providing vias in the mounting pads.

8. The method as claimed in claims 1 or 2, wherein the method further comprises mounting one or more integrated circuits (ICs) on a second surface of the first laminate material in an area substantially above individual or a cluster of the passive components.

9. The method as claimed in claims 1 or 2, wherein the second laminate material comprises contact traces for forming a multi-layered circuit board.

10. The method as claimed in claims 1 or 2, further comprising attaching one or more further laminate materials having contact traces formed thereon to the first and second laminate materials for forming a multi-layered circuit board.

11. The method as claimed in claims 1 or 2, wherein the method comprises attaching a resin coated metal material to the first and second laminate materials for forming a multi-layered circuit board.

12. The method as claimed in claims 1 or 2, wherein the laminate materials comprise organic laminate materials.