

WHAT IS CLAIMED IS:

1. A method of fabricating a dual damascene crossbar array, the method comprising:
 - 5 forming a bottom electrode layer on a substrate;
 - forming a first memory device on the bottom electrode layer; and
 - forming a dual damascene structure on the first memory device, wherein the dual damascene structure comprises a top electrode layer and a first via, wherein the first via is formed between the first memory device and the top electrode layer.
- 10 2. The method of claim 1 further comprising:
 - forming a second memory device on the bottom electrode layer; and
 - forming a second via for the second memory device, wherein the second via is formed between the second memory device and the top electrode layer.
3. The method of claim 1, wherein the via is a tapered via, wherein the via
15 includes a top portion coupled to the top electrode having a first critical dimension (CD) and a bottom portion coupled to the first memory device having a second CD.
4. The method of claim 3, wherein the first CD is larger than the second CD.
5. The method of claim 4, wherein a CD of a line of the top electrode layer is larger than the second CD of the via.
- 20 6. A dual damascene crossbar array comprising:
 - one or more memory devices of the dual damascene crossbar array;
 - a bottom electrode coupled to the one or more memory devices;
 - one or more vias coupled to each memory device; and

a top electrode layer coupled to the one or more vias, the one or more vias are positioned between the memory device and the top electrode layer.

7. The crossbar array of claim 6, wherein each of the one or more vias are tapered, wherein each of the one or more vias include a top portion coupled to the top electrode layer having a first critical dimension (CD) and a bottom portion coupled to the memory device having a second CD.
8. The crossbar array of claim 7, wherein each of the one or more vias has a CD that is in a range of 12-14 nm.
9. The crossbar array of claim 7, wherein the first CD is larger than the second CD.
10. The crossbar array of claim 9, wherein a CD of a line portion of the top electrode layer is larger than the second CD of the via.
11. The crossbar array of claim 10, wherein the line portion of the top electrode layer has a CD of 18 nm.
12. The crossbar array of claim 10, wherein a height of each of the one or more vias is 1.25 to 2 times at least one of the first CD or the second CD of the via.
13. The crossbar array of claim 6, wherein the bottom electrode is comprised of at least one of tungsten (W), molybdenum (Mo), ruthenium (Ru), and cobalt (Co).
14. The crossbar array of claim 6, further comprising a logic area coupled to the crossbar array through an interconnect, wherein the interconnect is configured to pass an increased current through the one or more memory devices to induce a void in the one or more vias.
15. A method of disabling memory devices of a dual damascene crossbar array, the method comprising:
 - identifying a faulty memory device of the dual damascene crossbar array, the crossbar array comprises:

one or more memory devices of the dual damascene crossbar array;
a bottom electrode coupled to the one or more memory devices;
one or more vias coupled to each memory device; and
a top electrode layer coupled to the one or more vias, the one or more
5 vias are positioned between the memory device and the top electrode layer;
disabling the faulty memory device of the dual damascene crossbar array; and
operating remaining one or more memory devices of the dual damascene
crossbar array.

16. The method of claim 15, wherein each of the one or more vias are tapered,
10 wherein each of the one or more vias include a top portion coupled to the top
electrode layer having a first critical dimension (CD) and a bottom portion coupled to
the memory device having a second CD.

17. The method of claim 15, wherein disabling the faulty memory device of the
dual damascene crossbar array comprises passing a current through the faulty memory
15 device to disable the faulty device.

18. The method of claim 17, wherein the current creates a void in a via
corresponding to the faulty memory device, the via is located between the faulty
memory device and the top electrode.

19. The method of claim 17, wherein the current is greater than an operating
20 current threshold for the dual damascene crossbar array.

20. The method of claim 19, wherein a CD of a line portion of the top electrode
layer is larger than the second CD of the one or more vias.