CLAIMS

1. A method comprising:

performing an implantation process in the presence of a gate electrode structure so as to introduce drain and source dopant species through a first sidewall and a second sidewall of an active region of a p-channel transistor of a semiconductor device, said active region being laterally enclosed by an isolation region that is recessed with respect to said active region, said first and second sidewalls defining a width of said active region; and

forming a metal silicide in said active region.

2. The method of claim 1, wherein performing said implantation process comprises using tilt angles with an amount of 20° or less with respect to a normal of said active region.

3. The method of claim 2, wherein said tilt angle amount is selected to 15° or less.

4. The method of claim 3, wherein said amount of said tilt angles is selected to be in the range of 8.5° to 12.5°.

5. The method of claim 1, wherein performing said implantation process further comprises forming deep drain and source regions in said active regions.

6. The method of claim 1, wherein said implantation process is performed so as to be substantially non-tilted with respect to a plane that is normal to a top surface of said active region and parallel to a width direction.

7. The method of claim 1, further comprising covering a second active region with an implantation mask when performing said implantation process,

wherein said second active region has formed thereon a second gate electrode structure that is not parallel to said gate electrode structure.

8. The method of claim 7, further comprising removing said implantation mask from said second active region, forming a further implantation mask so as to mask said active region and performing a second implantation process so as to introduce said drain and source dopant species through a first sidewall and a second sidewall of said second active region of a second p-channel transistor, wherein said first and second sidewalls of said second active region define a width of said second active region.

9. The method of claim 1, further comprising forming a semiconductor alloy in at least a portion of said active region by an epitaxial growth process prior to performing said implantation process.

10. The method of claim 9, wherein forming said semiconductor alloy comprises forming a compressive strain inducing semiconductor alloy in said active region.

11. The method of claim 9, wherein forming said semiconductor alloy comprises forming a threshold voltage adjusting semiconductor alloy in said active region.

12. A method comprising:

forming a gate electrode structure on an active region of a semiconductor device, said active region having a length and a width and being laterally delineated by an isolation region that is recessed with respect to said active region;

introducing drain and source dopant species into said active region by performing an implantation process, said implantation process including at least two different tilt angles with respect to a normal of a top surface of said active region and defined in a first plane that is normal to said top

surface of said active region and parallel to a width direction, said implantation process further including a non-varying implantation angle defined in a second plane that is normal to said top surface and perpendicular to said width direction; and

forming a metal silicide in a portion of said active region.

13. The method of claim 12, wherein respective two of said at least two different tilt angles are of same amount and different orientation.

14. The method of claim 12, wherein an amount of each of said at least two different tilt angles is in a range of 8.5° to 20°.

15. The method of claim 14, wherein an amount of each of said at least two different tilt angles is 15° or less.

16. The method of claim 12, wherein forming said gate electrode structure comprises forming a spacer structure prior to performing said implantation process and using at least a portion of said spacer structure as mask.

17. The method of claim 12, further comprising forming a semiconductor alloy in at least a portion of said active region prior to performing said implantation process.

18. The method of claim 12, further comprising covering a second active region with an implantation mask when performing said implantation process, wherein said second active region has formed thereon a second gate electrode structure that is not parallel to said gate electrode structure.

19. The method of claim 18, further comprising removing said implantation mask from said second active region, forming a further implantation mask so as to mask said active region and performing a second implantation process.

20. A semiconductor device comprising:

an isolation region formed above a substrate;

a silicon containing active region of a p-channel transistor laterally enclosed by said isolation region, said isolation region being recessed with respect to said silicon containing active region, said silicon containing active region having a length delimited by a pair of first sidewalls and having a width delimited by a pair of second sidewalls;

a gate electrode structure formed on said silicon containing active region;

drain and source regions, said drain and source regions comprising a first averaged dopant concentration at said first sidewalls that is less than a second averaged dopant concentration at said second sidewalls; and

a metal silicide formed in a portion of said silicon containing semiconductor region, said metal silicide being positioned within said drain and source regions.

CLAIMS

1. A method, comprising:

performing an implantation process in the presence of a gate electrode structure so as to introduce drain and source dopant species through a first sidewall and a second sidewall of an active region of a P-channel transistor of a semiconductor device, said active region being laterally enclosed by an isolation region that is recessed with respect to said active region, said first and second sidewalls defining a width of said active region, wherein performing said implantation process comprises using tilt angles with an amount of 20 degrees or less with respect to a normal of said active region; and

forming a metal silicide in said active region.

2. The method of claim 1, wherein said tilt angle amount is selected to be 15 degrees or less.

3. The method of claim 2, wherein said tilt angle amount is selected to be in the range of 8.5-12.5 degrees.

4. The method of claim 1, wherein performing said implantation process further comprises forming deep drain and source regions in said active region.

5. The method of claim 1, wherein said implantation process is performed so as to be substantially non-tilted with respect to a plane that is normal to a top surface of said active region and parallel to a width direction.

6. The method of claim 1, further comprising covering a second active region with an implantation mask when performing said implantation process, wherein said second active region has formed thereon a second gate electrode structure that is not parallel to said gate electrode structure.

7. The method of claim 6, further comprising removing said implantation mask from said second active region, forming a further implantation mask so as to

mask said active region and performing a second implantation process so as to introduce said drain and source dopant species through a first sidewall and a second sidewall of said second active region of a second P-channel transistor, wherein said first and second sidewalls of said second active region define a width of said second active region.

8. The method of claim 1, further comprising forming a semiconductor alloy in at least a portion of said active region by an epitaxial growth process prior to performing said implantation process.

9. The method of claim 8, wherein forming said semiconductor alloy comprises forming a compressive strain-inducing semiconductor alloy in said active region.

10. The method of claim 8, wherein forming said semiconductor alloy comprises forming a threshold voltage adjusting semiconductor alloy in said active region.

11. A method, comprising:

forming a gate electrode structure on an active region of a semiconductor device, said active region having a length and a width and being laterally delineated by an isolation region that is recessed with respect to said active region;

introducing drain and source dopant species into said active region by performing an implantation process, said implantation process including at least two different tilt angles with respect to a normal of a top surface of said active region and defined in a first plane that is normal to said top surface of said active region and parallel to a width direction, wherein an amount of each of said at least two different tilt angles is in a range of 8.5-20 degrees, said implantation process further including a non-varying implantation angle defined in a second plane that is normal to said top surface and perpendicular to said width direction; and

forming a metal silicide in a portion of said active region.

12. The method of claim 11, wherein respective two of said at least two different tilt angles are of the same amount and different orientation.

13. The method of claim 11, wherein an amount of each of said at least two different tilt angles is 15 degrees or less.

14. The method of claim 11, wherein forming said gate electrode structure comprises forming a spacer structure prior to performing said implantation process and using at least a portion of said spacer structure as a mask.

15. The method of claim 11, further comprising forming a semiconductor alloy in at least a portion of said active region prior to performing said implantation process.

16. The method of claim 11, further comprising covering a second active region with an implantation mask when performing said implantation process, wherein said second active region has formed thereon a second gate electrode structure that is not parallel to said gate electrode structure.

17. The method of claim 16, further comprising removing said implantation mask from said second active region, forming a further implantation mask so as to mask said active region and performing a second implantation process.

18. A method, comprising:

performing an implantation process in the presence of a first gate electrode structure so as to introduce drain and source dopant species through a first sidewall and a second sidewall of a first active region of a first P-channel transistor of a semiconductor device, said first active region being laterally enclosed by an isolation region that is recessed with respect to said first active region, said first and second sidewalls defining a width of said first active region;

covering a second active region with an implantation mask when performing said implantation process, wherein said second active region has

formed thereon a second gate electrode structure that is not parallel to said first gate electrode structure; and

forming a metal silicide in said first active region.

19. A method, comprising:

forming a first gate electrode structure on a first active region of a semiconductor device, said first active region having a length and a width and being laterally delineated by an isolation region that is recessed with respect to said first active region;

covering a second active region with an implantation mask, wherein said second active region has formed thereon a second gate electrode structure that is not parallel to said first gate electrode structure

while covering said second active region with said implantation mask, introducing drain and source dopant species into said first active region by performing an implantation process, said implantation process including at least two different tilt angles with respect to a normal of a top surface of said first active region and defined in a first plane that is normal to said top surface of said first active region and parallel to a width direction, said implantation process further including a non-varying implantation angle defined in a second plane that is normal to said top surface and perpendicular to said width direction; and

forming a metal silicide in a portion of said first active region.

20. A semiconductor device fabricated by a method in accordance with any one of the preceding claims.