Description

Field of the Invention

The present invention relates, in general, to integrated circuit data processing devices. More particularly, the invention relates to a microcomputer with on-board chip selects and programmable bus stretching.

Background of the Invention

Microcomputers are data processing devices which include a central processing unit (CPU), memory and some input/output (I/O) or other functions on a single piece, or chip, of semiconductor material. In many cases, such a microcomputer will include an external bus interface to provide communication with memory, I/O and other peripheral devices which are not located on the chip.

The timing requirements of integrated circuit data processors with external buses have long conflicted with the varying abilities of memory and other peripheral devices to respond to bus signals. Designers of computing systems have been forced to include circuits external to the data processor to modify, usually by "stretching" or inserting "wait states" into, the normal timing of a processor's buses in order to accommodate the abilities of the slower peripheral devices in their systems.

Most systems which include microcomputers also require off-chip logic to decode some of the upper address signals in order to trigger the enable, or select, inputs of the various peripheral devices. Bus stretching, chip select and any other required external functions are generally referred to as "glue logic". A possible design goal of a new microcomputer is to reduce required glue logic to as great an extent as possible.

U.S. Patent 4,509,120, issued April 2, 1985 and assigned to Bell Telephone Laboratories, describes a microcomputer which includes certain of this glue logic. In this case, the glue logic permits cycle-by-cycle variations in the bus cycle timing of the microcomputer. A latch can be loaded with a parameter which determines the extent to which a particular bus cycle is to be stretched. The bus cycle is stretched by delaying the assertion of a READY signal until a number of clock cycles equal to the value in the parameter register is counted

However, integrating glue logic functions onto a microcomputer chip is not necessarily a trivial process. Retaining the flexibility which must be present in a microcomputer in order that it reach a sufficiently wide market requires that difficult trade-offs be made between competing customer needs. Integrating chip select and bus stretching logic onto a microcomputer requires careful consideration of trade-offs between, for example, reducing glue logic and reducing overall microcomputer performance.

Summary of the Invention

Accordingly, it is an object of the present invention to provide a microcomputer with on-board chip select logic and programmable bus stretching.

It is a further object of the present invention to provide a microcomputer having on-board chip select logic and programmable bus stretching in which stretching of the external bus does not alter critical timing signals to other on-board devices.

These and other objects and advantages of the present invention are provided by a microcomputer comprising:

a central processing unit;

clock logic means for providing a first timing signal to said central processing unit;

another device which receives a second timing signal from said clock logic means;

external bus interface means for providing communication between said central processing unit and devices external to the microcomputer, said external bus interface means provides a chip select signal when an address provided by said central processing unit is within a pre-selected range of address values; and

bus stretch means for selectably stretching a bus cycle;

the microcomputer being characterized in that:

the bus stretch means also freezes said first timing signal for a preselected period while said chip select signal is active while continuing said second timing signal unaffected.

In accordance with another aspect of the present invention there is provided in a microcomputer comprising a central processing unit; clock logic means for providing a first timing signal to said central processing unit; another device which receives a second timing signal from said clock logic means; and external bus interface means for providing communication between said central processing unit and devices external to the microcomputer, a method of selectably stretching a bus cycle for a predetermined period comprising the steps of:

selectably providing to said external devices a chip select signal if an address provided by said central processing unit is within a pre-selected range of address values; said method being characterised by the steps of:

freezing said first timing signal to said central processing unit; and

continuing said second timing signal unaffected. These and other objects and advantages of the present invention will be apparent from the detailed description below taken together with the drawings.

Brief Description of the Drawings

FIG. 1 is a block diagram illustrating a microcom-

puter according to the principles of the present invention;

FIG. 2 is a block diagram illustrating a portion of the chip select and bus stretch logic of the microcomputer of FIG. 1; and

FIG.s 3A-3B are timing diagrams illustrating the operation of the apparatus of FIG.s 1 and 2.

Detailed Description of the Invention

FIG. 1 illustrates a microcomputer 10. Microcomputer 10 comprises a CPU 11, a timer unit 12, a serial communication interface 13, a memory unit 14, an external bus interface 15 and a clock logic unit 16. CPU 11 executes instructions and operates on data stored either in memory 14 or in external memory and communicates with timer 12, serial interface 13, memory 14 and external bus interface 15 by means of a set of internal buses 18. Internal buses 18 include address lines, data lines and control lines, as is familiar in the art.

Clock logic 16 receives signals, for instance, from an externally provided crystal oscillator, and generates the clock signals from which each of the other components of microcomputer 10 derive their timing signals. Clock logic 16 is, therefore, coupled to each of CPU 11, timer 12, serial interface 13, memory 14 and external bus interface 15. In addition, clock logic 16 provides a clock signal E (referred to hereinafter as the E-clock) in order that external devices may operate in appropriate timing relationship with microcomputer 10.

As illustrated, CPU 11, timer 12 and serial interface 13 are coupled to pins of microcomputer 10 to provide electrical connections to external devices. However, these connections are not necessary to an understanding of the present invention.

External bus interface 15 is also coupled to pins of microcomputer 10. As is familiar in the art, external bus interface 15 may "share" some pins with another on-board device such as a general purpose I/O port. This feature is not illustrated here to preserve clarity. External bus interface 15 provides the means by which CPU 11 communicates with externally provided memory and other peripheral devices which reside in its memory map. To that end, external bus interface 15 is coupled to a first group of pins which provide a plurality of address output signals, a second group of pins which provide a plurality of bidirectional data signals, a third group of pins which provide a plurality of chip select output signals and a single pin which provides a read/write output signal. Taken together, these pins comprise the external bus of microcomputer 10. The E-clock signal provided by clock logic 16 may also be thought of as a part of the external bus, since it provides the basis from which the timing specifications of the bus are defined and the means by which external devices may synchronize to the bus.

One skilled in the art will appreciate that the above-described external bus follows the conventions of products available from Motorola Microprocessor Products Group of Austin, Texas. However, the described embodiment is merely exemplary and not intended to limit the scope of the present invention of the conventions of a particular manufacturer.

Referring now to FIG. 2, portions of microcomputer 10 of FIG. 1 are illustrated in greater detail. Address compare logic 20 receives inputs from at least some of the address lines of internal buses 18 (see FIG. 1) and from a start address register 21. In addition, address compare logic 20 receives inputs from three bits, labelled SIZ1-SIZ3, of a control register 22. An output of address compare logic 20 is coupled to an input of priority logic 23. An output of priority logic 23 is coupled to an enable input of a pin driver 24.

Pin driver 24 also has inputs coupled to two bits, labelled POL and TIM, of control register 22. An output of pin driver 24 is coupled to a chip select pin which comprises one of the chip select outputs of external bus interface 15 of microcomputer 10.

Clock logic 16 has inputs coupled to an output of priority logic 23 and to two bits, labelled WAIT1 and WAIT2 of control register 22. Clock logic 16 has outputs which supply clock signals to CPU 11, external bus interface 15, to the E-clock pin of microcomputer 10 and to all other on-board devices such as timer 12, serial interface 13 and memory 14.

In operation, user-supplied software may store appropriate data values in start address register 21 and control register 22 in order to operate the chip select and bus stretch logic in the desired fashion. The start address register contains the lower bound of the address range for which the user wishes the chip select signal to be active. The SIZ1-SIZ3 bits of control register 22 contain information from which the desired size of the address range can be derived for which the chip select signal is to be active. Using three bits, a selection between eight available sizes may be encoded. In the preferred embodiment, one of the available sizes is zero, which provides a means for disabling the chip select and bus stretch logic without the need of a separate enable control bit.

Whenever the address being accessed by CPU 11 falls within the range defined by the start address register and the SIZ control bits, address compare logic 20 produces an enable signal, which is provided to an input of priority logic 23. Priority logic 23 serves to avoid conflicts between several devices which, because of the values stored by user-supplied software in registers 21 and 22, would otherwise be located at overlapping sites within the memory map. In other words, if the control, status and data registers of timer 12 appear in the memory map of CPU 11 at addresses $E000 - $E004 (addresses are given in hexadecimal), if the value $E000 has been stored in start address register 21 and if the SIZ control bits specify a size of

1K bytes, then there is a potential conflict between the off-chip device to which the chip select signal is coupled and timer 12. Priority logic 23 receives inputs from the address decoding circuits for each of the devices with which there is a potential conflict and allows the enable signal from address compare logic 20 to pass only if there is no actual conflict.

In the preferred embodiment, any on-board device has priority over any off-chip device and a predetermined scheme exists for assigning priority between off-chip devices.

If no other, higher priority device preempts it from doing so, priority logic 23 passes the enable signal from address compare logic 20 to an enable input of pin driver 24. Pin driver 24 responds to its enable input by driving an active chip select signal out via the chip select pin. The timing and polarity of the chip select signal are determined according to the TIM and POL bits, respectively, of control register 22.

Any logic signal may be either active high or active low. By common usage, chip select signals are most often active low. However, to provide as much flexibility as possible, it may be advantageous to provide at least one chip select signal which may be selected to be active high. The POL bit allows the user to select the active state of the chip select signal. Similarly, chip select signals are sometimes active, or valid, during a particular phase of the E-clock signal (or similar signal in other bus systems), or may be valid as long as the address signals are valid. The TIM bit allows the user to chose between, in the preferred embodiment, whether the chip select signal will be active simultaneously with the high phase of the E-clock (referred to as E-valid) or simultaneously with the presence of a valid address (address-valid).

In addition to being coupled to the enable input of pin driver 24, the output of priority logic 23 is coupled to an input of clock logic 16. Thus, whenever pin driver 24 is enabled to drive a chip select signal active, clock logic 16 is enabled to execute a bus stretch operation, if programmed to do so by the WAIT bits of control register 22.

Using two bits from control register 22, as shown here, one can program four different bus stretch periods. In the preferred embodiment, the data value stored in WAIT1 and WAIT2 may represent the digital values 0,1,2 or 3. This is interpreted by clock logic 16 as a number of extra E-clock cycles, or wait states, to be inserted into the current bus cycle. Of course, with other common microcomputer buses, the details of the encoding and implementation of the bus stretch bits may be slightly different.

As is described more fully with reference to FIG.s 3A and 3B, clock logic 16 responds to the input from priority logic 23 and the value of the WAIT bits by modifying some, but not all, of the clock signals it provides to the various internal and external devices. The E-clock signal is frozen, effectively stretching time for external devices. In addition, the clock signal supplied to CPU 11 is frozen, since it must wait for the bus cycle to properly terminate before continuing. The clock supplied to external bus interface 15 is also frozen, so that the address and read/write line drivers remain frozen.

However, the clock signals supplied by clock logic 16 to timer 12 and serial interface 13 (and to any other on-board devices which might need a steady clock signal) are not frozen. This provides, for instance, that free-running counters in timer 12 which are used to generate real-time signals are not rendered inaccurate by the use of stretched bus cycles. Similarly, baud rate generators in serial interface 13 which rely on the system clock as a time base are not interfered with. Similar benefits are available to other devices which may be integrated on the microcomputer chip.

Referring now to FIG. 3A the unaltered external bus timing of the microcomputer of FIG. 1 is illustrated. The uppermost trace of FIG. 3A represents the E-clock signal produced by clock logic 16. The E-clock signal is, roughly, a square wave of a predetermined period. For instance, if the basic bus speed of the microcomputer is 2 MHz, the period of the E-clock signal will be approximately 500 nanoseconds.

The next trace of FIG. 3A represents the presence and absence of valid signals on the external address bus. Normally, address information changes shortly after a falling edge of the E-clock and remains valid until after the next falling edge of the E-clock. An external device must respond to the valid address by (in the case of a read cycle) placing data on the data bus no later than a predetermined time, t_{ACC}, after the address becomes valid, as shown by the next trace of FIG. 3A. As shown, t_{ACC} is less than one E-clock period, which may be substantially less than the minimum access time for some slow memories, for instance.

The last trace of FIG. 3A illustrates the activity of a programmed chip select signal. In this case, assume that the start address for this particular chip select signal has been set at $1800 and that the size has been set to 2K bytes. Further assume that the timing of the signal has been set to E-valid and that the signal has been programmed to active low. Thus, shortly after the address $1800 is placed on the address lines, the chip select signal becomes active (goes low), thus enabling the peripheral to respond to the address. As illustrated, the next two bus cycles, which access addresses $E000 and $E001, respectively, do not trigger the activation of the chip select signal, since they fall outside of the programmed address range.

Obviously, in the case illustrated in FIG. 3A, the programmed number of wait states, or bus stretch cycles, is zero. FIG. 3B illustrates the use of the programmable bus stretch feature to accommodate a peripheral device which has a minimum access time, t'_{ACC}, which is longer than t_{ACC}. The programming of

the chip select logic for this device is the same as that described above, except that a bus stretch of 1 E-clock cycle has been programmed. As illustrated, both the address and chip select signals become valid at their respective normal times with respect to the E-clock, but they each remain valid for an additional period equal to one "normal" E-clock period, as does the E-clock signal itself. In this case, the slow peripheral is allowed its necessary access time. Meanwhile, as pointed out above, any timers, serial interfaces and other on-board, system clock-dependent devices remain accurate, since their clock signals are not interrupted.

While the description above involves a very flexible and powerful programmable chip select and bus stretch implementation, certain modifications and changes may be made to accommodate particular situations. For instance, in a preferred embodiment of the present invention, a microcomputer has four chip select pins. One, referred to as the general purpose chip select, is substantially as described above.

Another, referred to as the program chip select, does not have the same flexibility as to location as does the general purpose chip select. Its size is determined by a two-bit control register field to be one of 64K, 32K, 16K or 8K bytes and its upper bound is always $FFFF. Its polarity is always active low and it is always address valid. A one-bit control field acts to enable or disable this chip select and bus stretch mechanism, since no zero-size option is available. Also, a one-bit control field determines whether the program or the general purpose chip select has a higher priority. The program chip select has the same programmable bus stretches as does the general purpose chip select.

The program chip select is optimized for selecting an external memory device or devices which contain user-supplied programs. The program chip select requires only 6 bits of control information as opposed to 13 for the general purpose chip select.

The other two chip selects, referred to as the register selects, also have less flexible location and size. The location of the register selects is determined by the location of the register space of the microcomputer, which is mappable to any 4K boundary within the memory map. The register selects and the register space occupy a total of 4K of memory space. The first register select has a size of 2K and the other is 2K minus the size of the register space. Each register select has one enable bit, one polarity bit and a two-bit bus stretch field. The timing is always E-valid. The register selects have higher priority than the other selects, but lower than internal devices. The register selects require a total of 6 bits of control information.

Claims

1. A microcomputer comprising:
   a central processing unit;
   clock logic means for providing a first timing signal to said central processing unit;
   another device which receives a second timing signal from said clock logic means;
   external bus interface means for providing communication between said central processing unit and devices external to the microcomputer, said external bus interface means provides a chip select signal when an address provided by said central processing unit is within a pre-selected range of address values; and
   bus stretch means for selectably stretching a bus cycle;
   the microcomputer being characterized in that:
   the bus stretch means also freezes said first timing signal for a preselected period while said chip select signal is active while continuing said second timing signal unaffected.

2. A microcomputer according to claim 1 wherein said bus stretch means further comprises:
   register means for storing a value indicative of said pre-selected period; and
   means responsive to an indication that an address supplied by said central processing unit is within a preselected range of address values to freeze said first timing signal for said pre-selected period.

3. A microcomputer according to claim 2 wherein:
   said register means is writable by said central processing unit.

4. In a microcomputer comprising a central processing unit; clock logic means for providing a first timing signal to said central processing unit; another device which receives a second timing signal from said clock logic means; and external bus interface means for providing communication between said central processing unit and devices external to the microcomputer, a method of selectably stretching a bus cycle for a predetermined period comprising the steps of:
   selectably providing to said external devices a chip select signal if an address provided by said central processing unit is within a pre-selected range of address values; said method being characterised by the steps of:
   freezing said first timing signal to said central processing unit for a preselected period while said chip select is active ;and
   continuing said second timing signal unaffected.

the chip select logic for this device is the same as that described above, except that a bus stretch of 1 E-clock cycle has been programmed. As illustrated, both the address and chip select signals become valid at their respective normal times with respect to the E-clock, but they each remain valid for an additional period equal to one "normal" E-clock period, as does the E-clock signal itself. In this case, the slow peripheral is allowed its necessary access time. Meanwhile, as pointed out above, any timers, serial interfaces and other on-board, system clock-dependent devices remain accurate, since their clock signals are not interrupted.

While the description above involves a very flexible and powerful programmable chip select and bus stretch implementation, certain modifications and changes may be made to accommodate particular situations. For instance, in a preferred embodiment of the present invention, a microcomputer has four chip select pins. One, referred to as the general purpose chip select, is substantially as described above.

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Claims

1. A microcomputer comprising:
   a central processing unit;
   clock logic means for providing a first timing signal to said central processing unit;
   another device which receives a second timing signal from said clock logic means;
   external bus interface means for providing communication between said central processing unit and devices external to the microcomputer, said external bus interface means provides a chip select signal when an address provided by said central processing unit is within a pre-selected range of address values; and
   bus stretch means for selectably stretching a bus cycle;
   the microcomputer being characterized in that:
   the bus stretch means also freezes said first timing signal for a preselected period while said chip select signal is active while continuing said second timing signal unaffected.

2. A microcomputer according to claim 1 wherein said bus stretch means further comprises:
   register means for storing a value indicative of said pre-selected period; and
   means responsive to an indication that an address supplied by said central processing unit is within a preselected range of address values to freeze said first timing signal for said pre-selected period.

3. A microcomputer according to claim 2 wherein:
   said register means is writable by said central processing unit.

4. In a microcomputer comprising a central processing unit; clock logic means for providing a first timing signal to said central processing unit; another device which receives a second timing signal from said clock logic means; and external bus interface means for providing communication between said central processing unit and devices external to the microcomputer, a method of selectably stretching a bus cycle for a predetermined period comprising the steps of:
   selectably providing to said external devices a chip select signal if an address provided by said central processing unit is within a pre-selected range of address values; said method being characterised by the steps of:
   freezing said first timing signal to said central processing unit for a preselected period while said chip select is active ;and
   continuing said second timing signal unaffected.

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5. A method according to claim 4 wherein said step of selectably stretching further comprises the steps of:

storing a value in a register; and

operating said clock logic to freeze said first timing signal for a period determined by said value stored in said register while leaving said second timing signal unaffected.

6. A method according to claim 5 further comprising the step of:

freezing a third timing signal provided by said clock logic to said external devices while said first timing signal is frozen.

Patentansprüche

1. Mikrocomputer mit:

einer zentralen Prozessoreinheit;

einer Taktlogikeinheit zum Bereitstellen eines ersten Zeitgebersignals an die zentrale Prozessoreinheit;

einer weiteren Einrichtung, die von der Taktlogikeinheit ein zweites Zeitgebersignal empfängt;

einer externen Busschnittstelle zur Herstellung einer Kommunikation zwischen der zentralen Prozessoreinheit und Einrichtungen außerhalb des Mikrocomputers, wobei die externe Busschnittstelle ein Chipauswahlsignal liefert, wenn eine von der zentralen Prozessoreinheit bereitgestellte Adresse innerhalb eines vorgewählten Bereichs von Adreßwerten liegt; und

einer Busdehnungseinrichtung zum wahlweisen Dehnen eines Buszyklus;

dadurch gekennzeichnet, daß, solange das Chipauswahlsignal aktiv ist, die Busdehnungseinrichtung für eine vorgewählte Zeitspanne auch das erste Zeitgebersignal einfriert, dabei aber das zweite Zeitgebersignal unbeeinflußt fortsetzt.

2. Mikrocomputer nach Anspruch 1, bei dem die Busdehnungseinrichtung ferner aufweist:

ein Register zum Speichern eines die vorgewählte Zeitspanne angebenden Werts; und

eine Einrichtung zum Einfrieren des ersten Zeitgebersignals für die vorgewählte Zeitspanne, wenn eine Angabe vorliegt, daß eine von der zentralen Prozessoreinheit gelieferte Adresse innerhalb eines vorgewählten Bereichs von Adreßwerten liegt.

3. Mikrocomputer nach Anspruch 2, bei dem die zentrale Prozessoreinheit in das Register schreiben kann.

4. In einem Mikrocomputer mit einer zentralen Prozessoreinheit; einer Taktlogikeinheit zum Bereitstellen eines ersten Zeitgebersignals an die zentrale Prozessoreinheit; einer weiteren Einrichtung, die von der Taktlogikeinheit ein zweites Zeitgebersignal empfängt; und einer externen Busschnittstelle zur Herstellung einer Kommunikation zwischen der zentralen Prozessoreinheit und Einrichtungen außerhalb des Mikrocomputers, ein Verfahren zum wahlweisen Dehnen eines Buszyklus für eine vorgegebene Zeitspanne, mit den Schritten, daß an die externen Einrichtungen wahlweise ein Chipauswahlsignal geliefert wird, wenn eine von der zentralen Prozessoreinheit gelieferte Adresse innerhalb eines vorgewählten Bereichs von Adreßwerten liegt;

gekennzeichnet durch die Verfahrensschritte, daß

das erste, der zentralen Prozessoreinheit bereitgestellte Zeitgebersignal für eine vorgewählte Zeitspanne eingefroren wird, solange das Chipauswahlsignal aktiv ist; und

das zweite Zeitgebersignal unbeeinflußt fortgesetzt wird.

5. Verfahren nach Anspruch 4, bei dem der Schritt des wahlweisen Dehnens ferner die Schritte umfaßt, daß

ein Wert in einem Register gespeichert wird; und

die Taktlogik so betrieben wird, daß das erste Zeitgebersignal für eine durch den im Register gespeicherten Wert bestimmte Zeitspanne eingefroren wird, während das zweite Zeitgebersignal unbeeinflußt gelassen wird.

6. Verfahren nach Anspruch 5, mit dem weiteren Schritt, daß ein von der Taktlogik an die externen Einrichtungen geliefertes drittes Zeitgebersignal eingefroren wird, solange das erste Zeitgebersignal eingefroren ist.

Revendications

1. Micro-ordinateur comprenant:

une unité centrale de traitement;

un moyen logique à horloge pour fournir un premier signal de synchronisation à ladite unité centrale de traitement;

un autre dispositif qui reçoit un second signal de synchronisation dudit moyen logique à horloge;

un moyen d'interface de bus externe pour assurer une communication entre ladite unité centrale de traitement et des dispositifs à l'extérieur du micro-ordinateur, ledit moyen d'interface de bus externe fournissant un signal de sélection

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de puce quand une adresse fournie par ladite unité centrale de traitement est comprise dans une plage de valeurs d'adresse présélectionnée; et

un moyen d'extension de bus pour prolonger d'une façon sélectionnable un cycle de bus;

le micro-ordinateur étant caractérisé en ce que:

le moyen d'extension de bus fige aussi ledit premier signal de synchronisation pendant une période présélectionnée alors que ledit signal de sélection de puce est actif tout en maintenant ledit second signal de synchronisation non modifié.

2. Micro-ordinateur selon la revendication 1, dans lequel ledit moyen d'extension de bus comprend en outre:

un moyen à registre pour mémoriser une valeur indiquant ladite période présélectionnée; et

un moyen réagissant à une indication qu'une adresse fournie par ladite unité centrale de traitement est comprise dans une plage de valeurs d'adresse présélectionnée pour figer ledit premier signal de synchronisation pendant ladite période présélectionnée.

3. Micro-ordinateur selon la revendication 2, dans lequel ladite unité centrale de traitement peut effectuer une écriture dans ledit moyen à registre.

4. Dans un micro-ordinateur comprenant une unité centrale de traitement; un moyen logique à horloge pour fournir un premier signal de synchronisation à ladite unité centrale de traitement; un autre dispositif qui reçoit un second signal de synchronisation dudit moyen logique à horloge; et un moyen d'interface de bus externe pour assurer une communication entre ladite unité centrale de traitement et des dispositifs à l'extérieur du micro-ordinateur, un procédé d'extension d'une façon sélectionnable d'un cycle de bus pendant une période prédéterminée comprenant l'étape qui consiste à:

fournir d'une façon sélectionnable auxdits dispositifs à l'extérieur un signal de sélection de puce si une adresse fournie par ladite unité centrale de traitement est comprise dans une plage de valeurs d'adresse présélectionnée; ledit procédé étant caractérisé par les étapes qui consistent à:

figer ledit premier signal de synchronisation fourni à ladite unité centrale de traitement pendant une période présélectionnée alors que ledit signal de sélection de puce est actif; et à

maintenir ledit second signal de synchronisation non modifié.

5. Procédé selon la revendication 4, dans lequel ladite étape d'extension d'une façon sélectionnable comprend en outre les étapes qui consistent à:

mémoriser une valeur dans un registre; et à

faire fonctionner ledit moyen logique à horloge pour figer ledit premier signal de synchronisation pendant une période déterminée par ladite valeur mémorisée dans ledit registre tout en maintenant non modifié ledit second signal de synchronisation.

6. Procédé selon la revendication 5, comprenant en outre l'étape qui consiste à :

figer un troisième signal de synchronisation fourni par ledit moyen logique à horloge auxdits dispositifs à l'extérieur alors que ledit premier signal de synchronisation est figé.

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