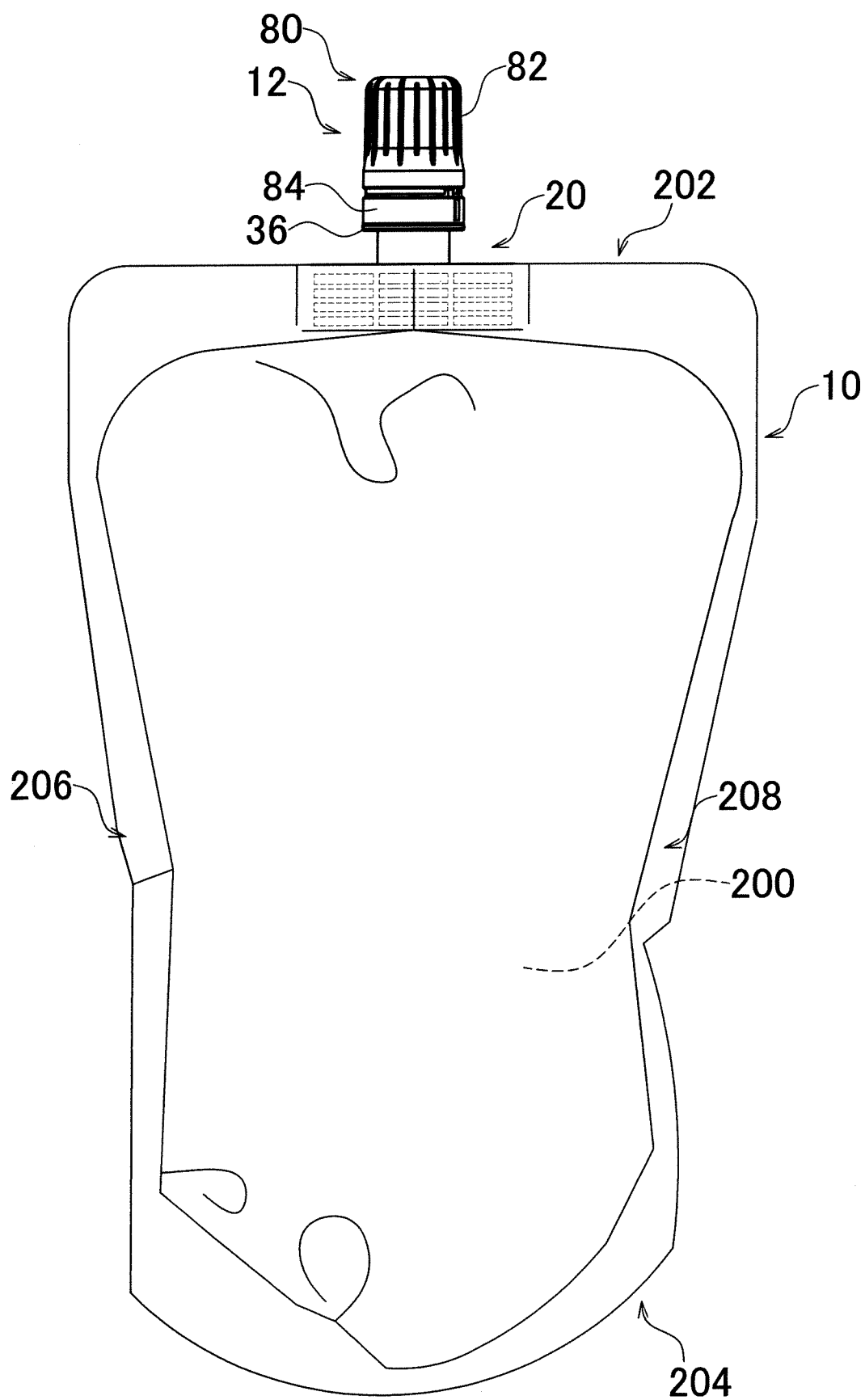


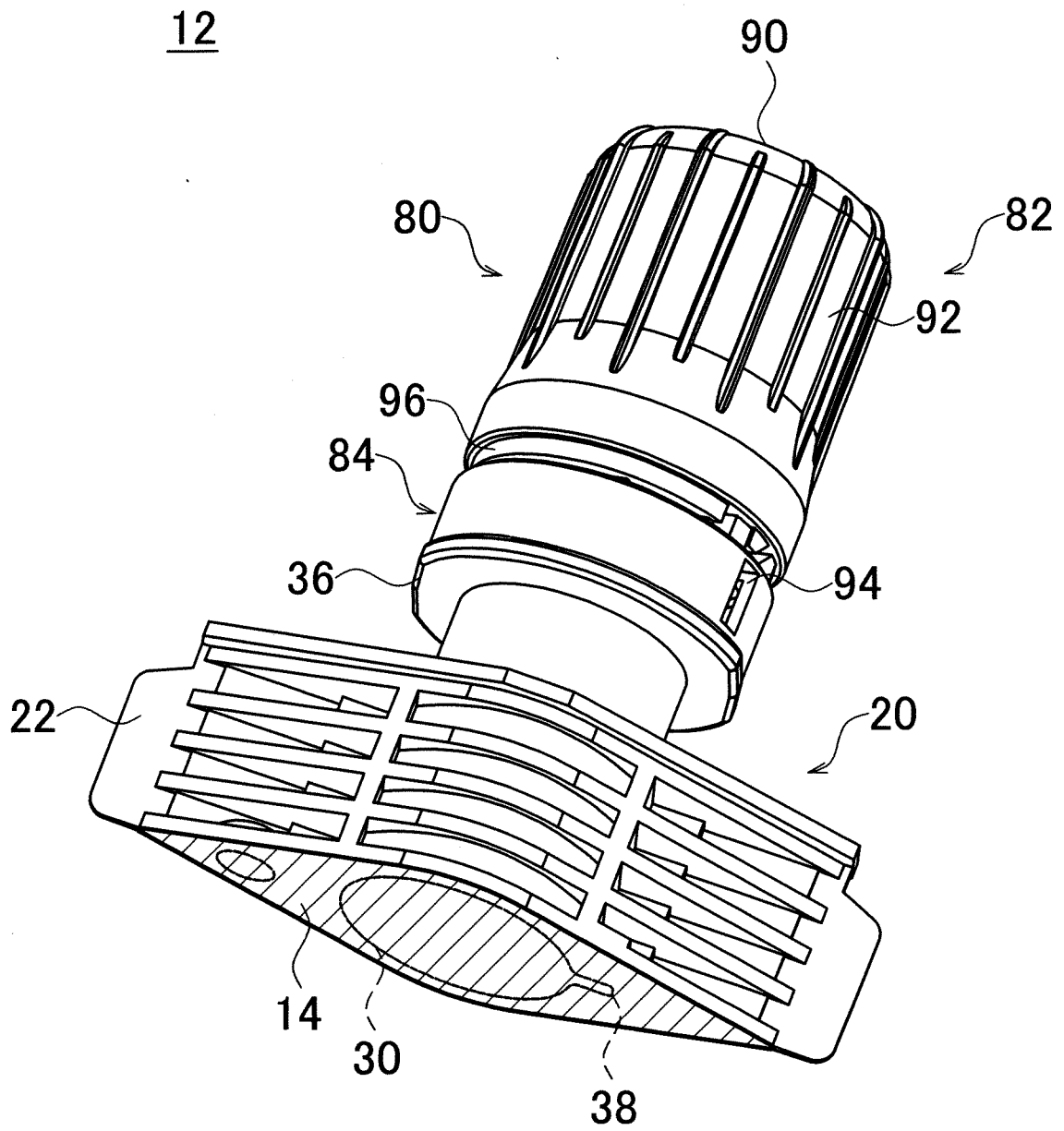
【FIG. 1】

FIG. 1



【FIG. 2】

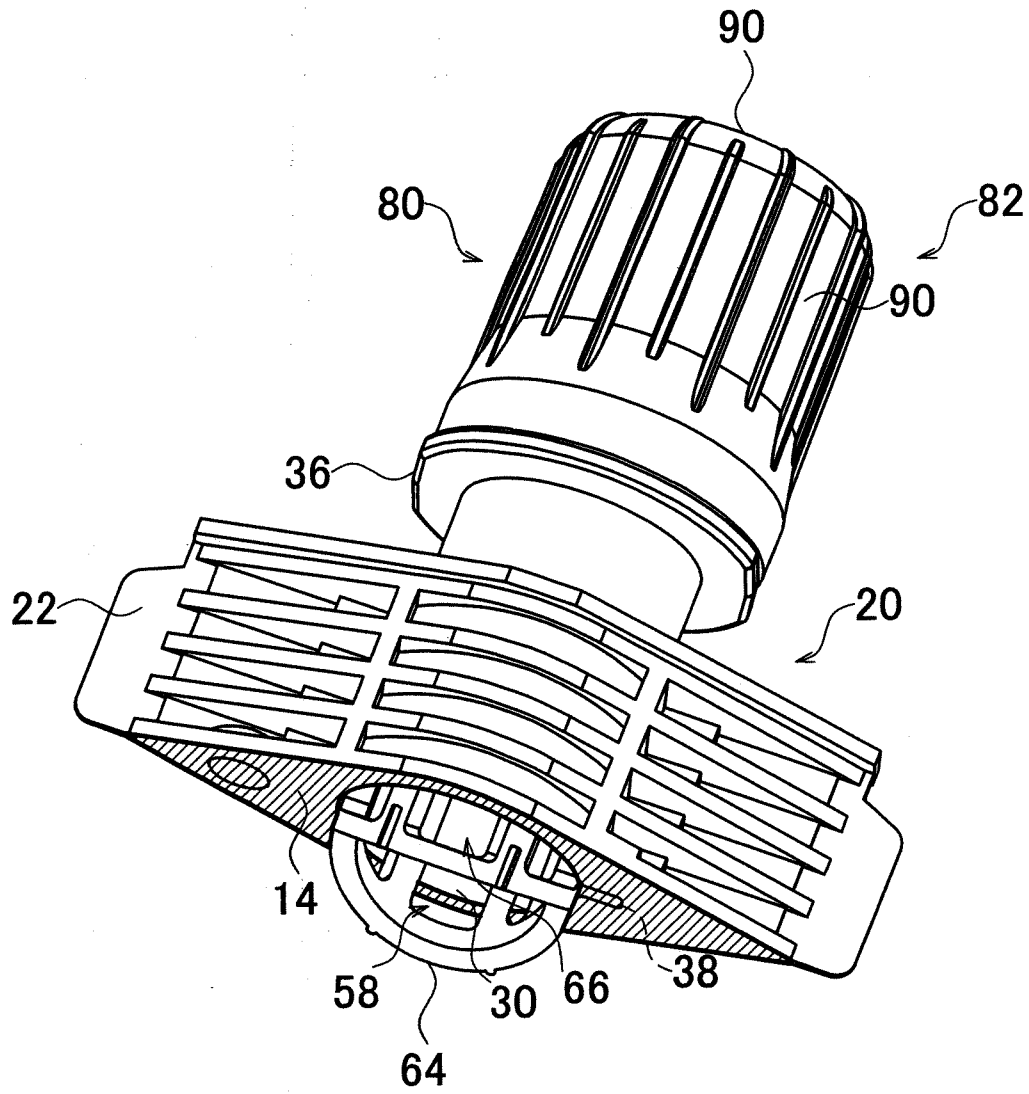
FIG. 2



80 { 82 { 90
92
84 { 94
96

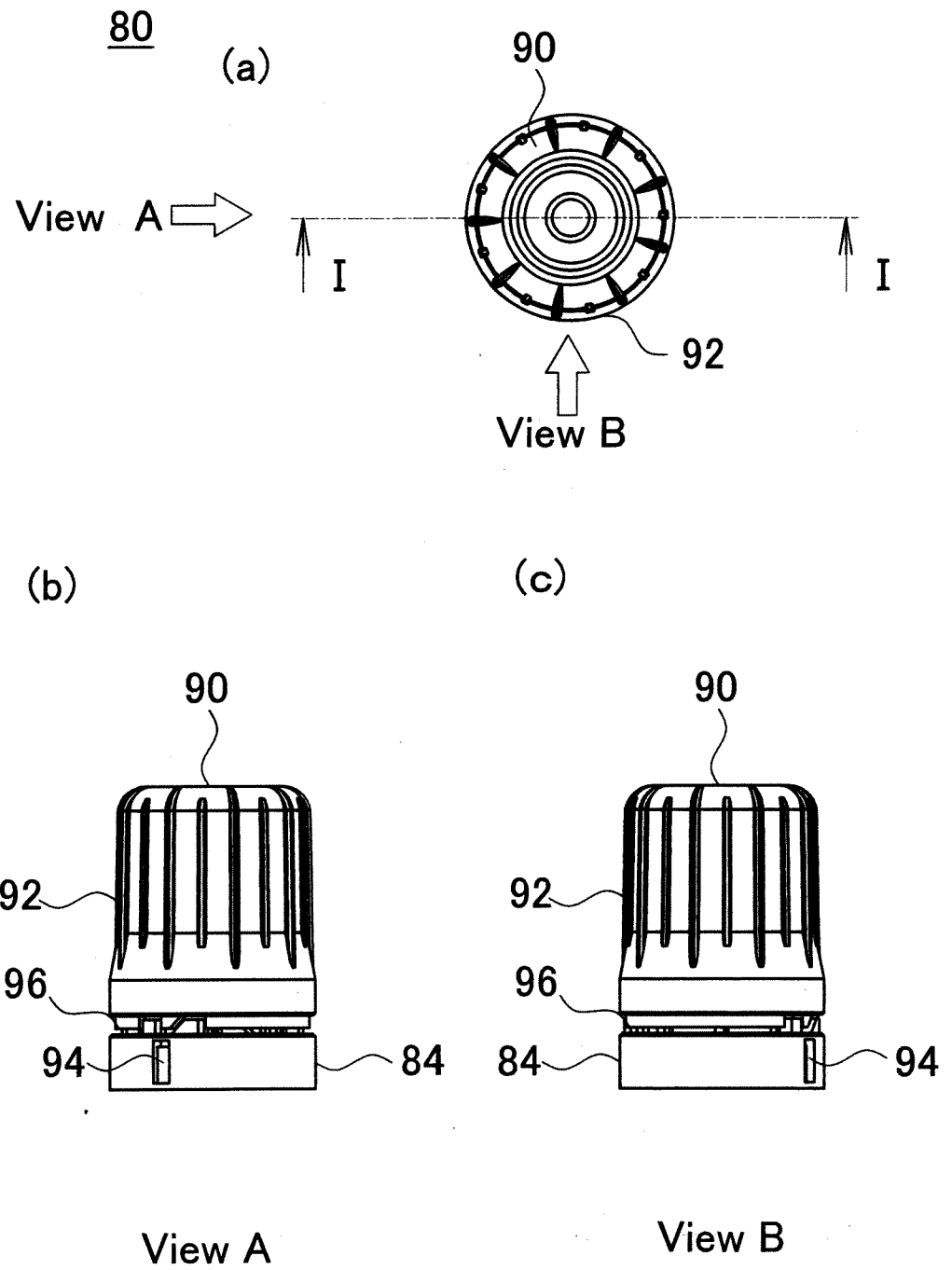
【FIG. 3】

FIG. 3

12

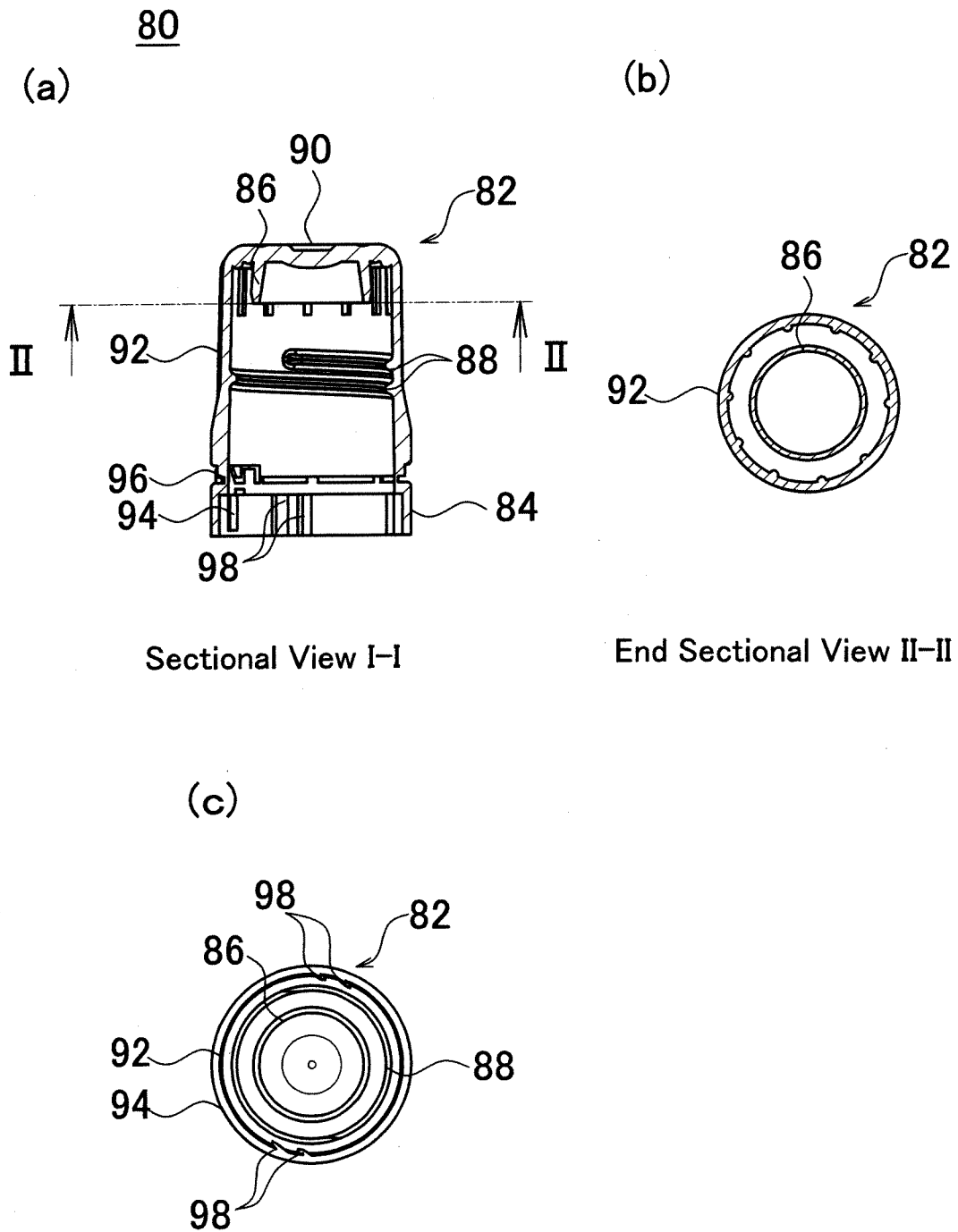
【FIG. 4A】

FIG. 4A



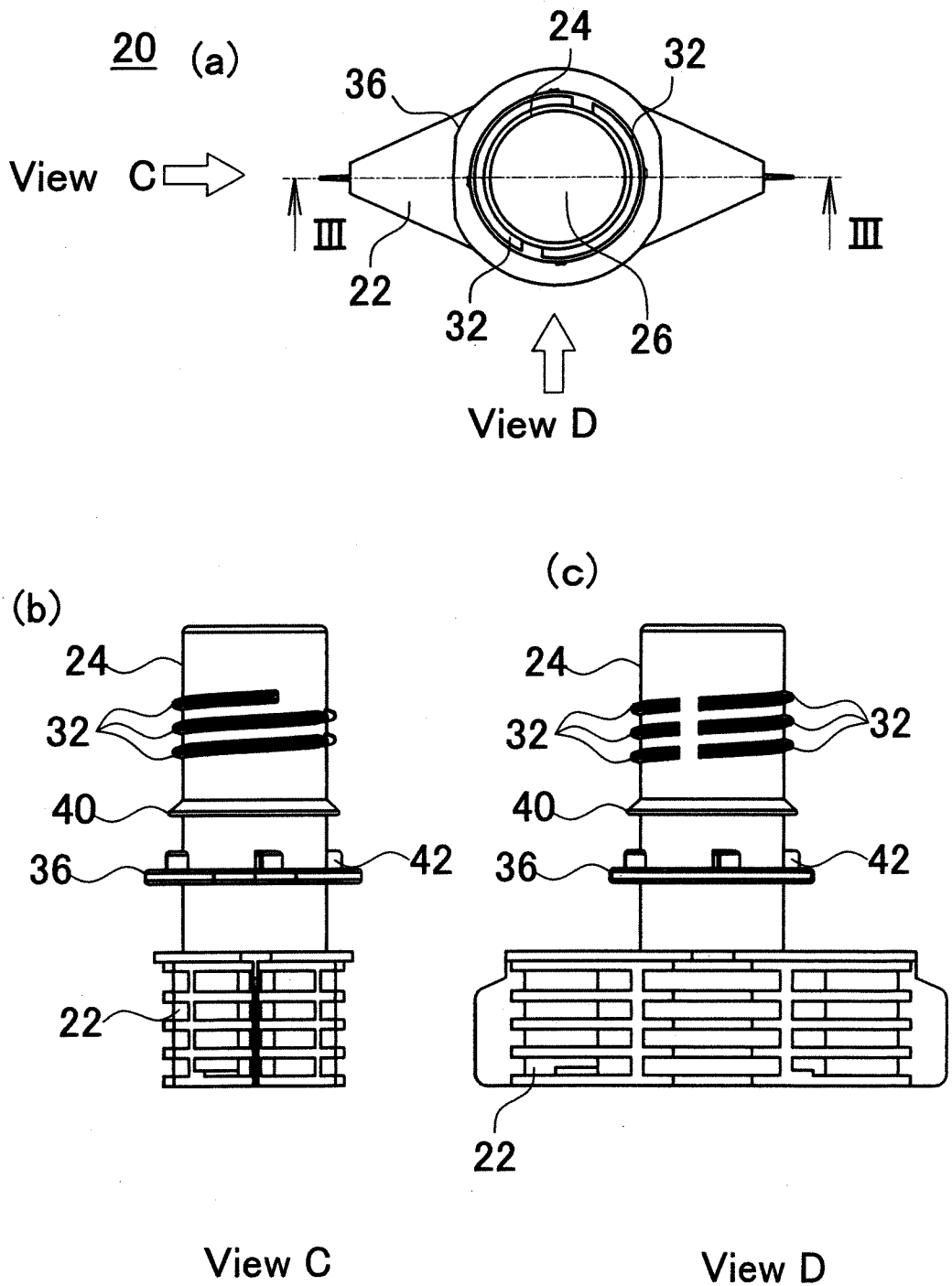
【FIG. 4B】

FIG. 4B



【FIG. 5A】

FIG. 5A

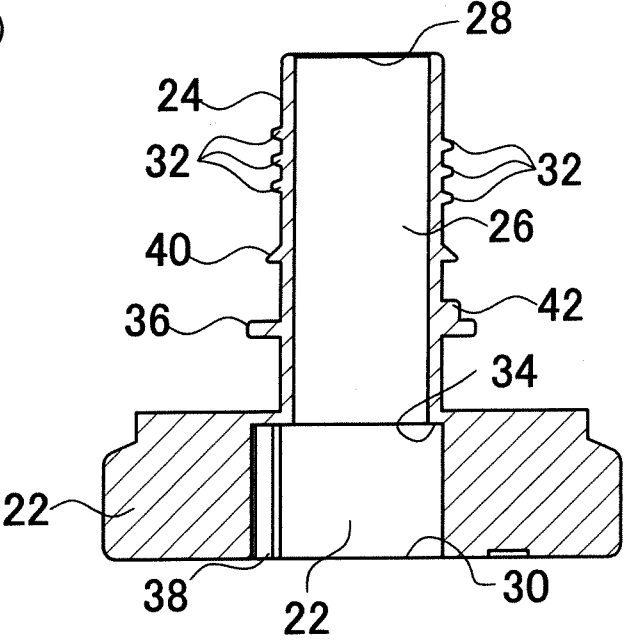


【FIG. 5B】

FIG. 5B

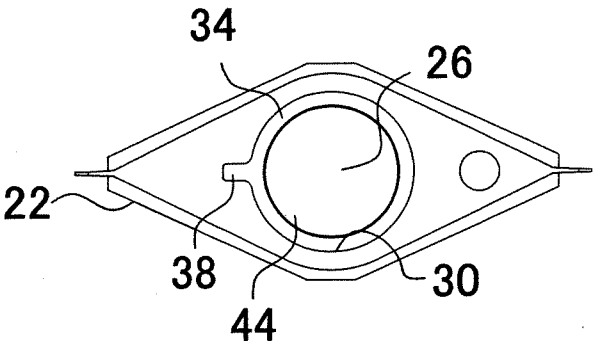
20

(a)



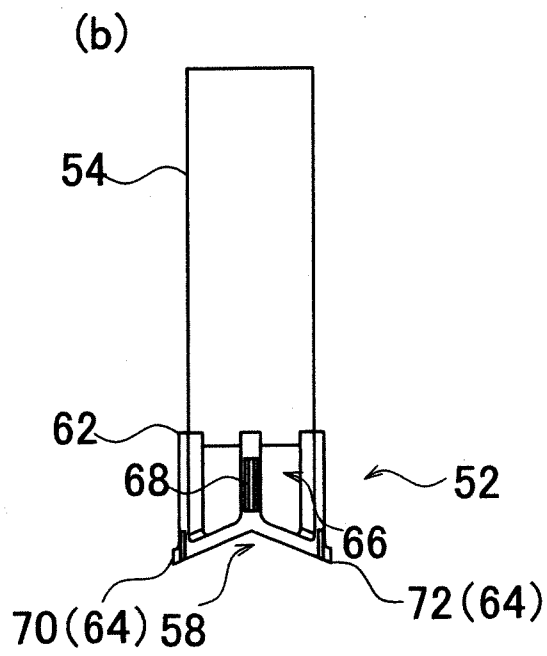
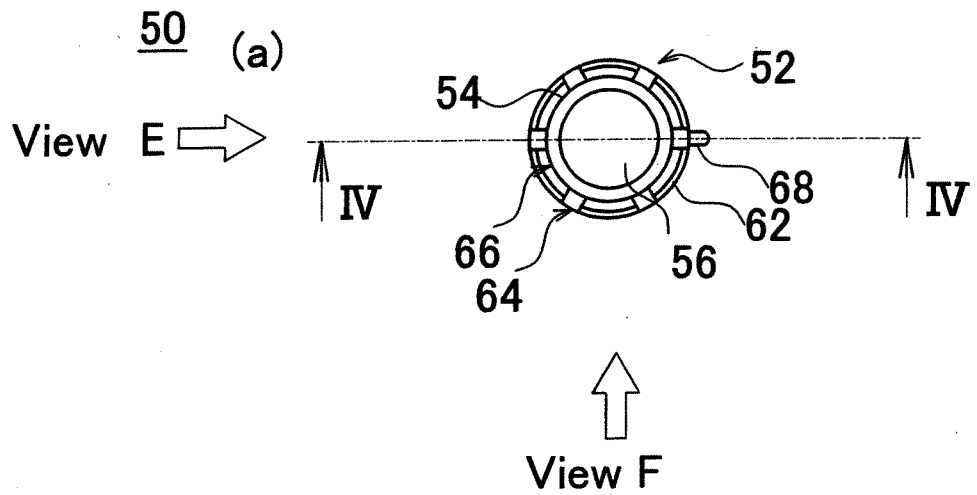
Sectional View III-III

(b)

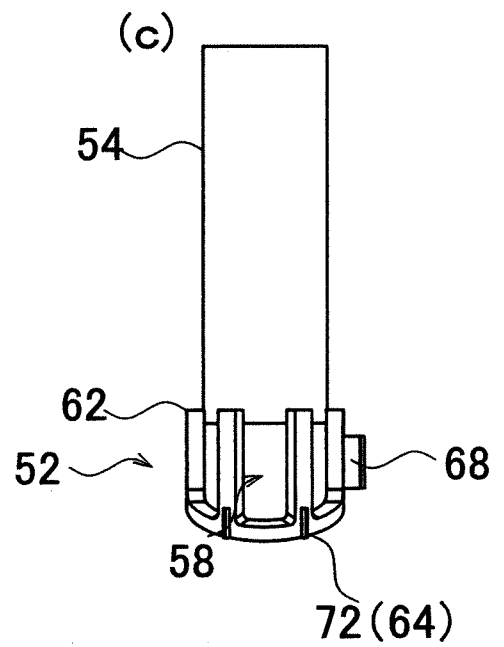


【FIG. 6A】

FIG. 6A



View E

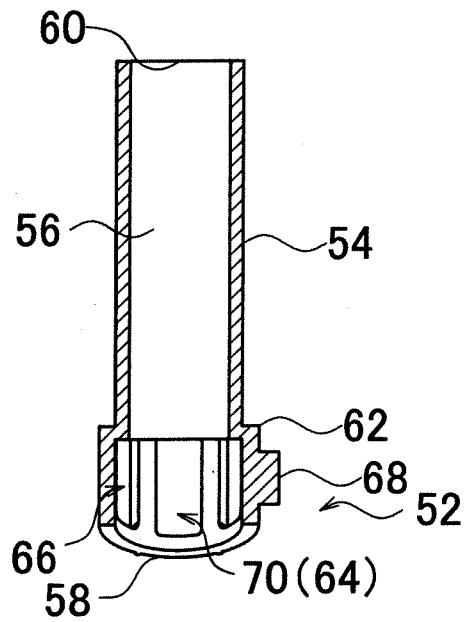


View F

【FIG. 6B】

FIG. 6B

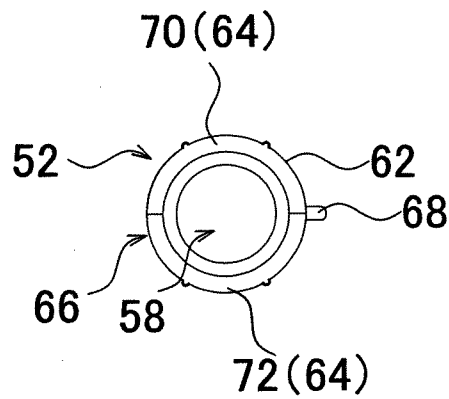
50
(a)



52 { 62
64 } 70
66 } 72
68

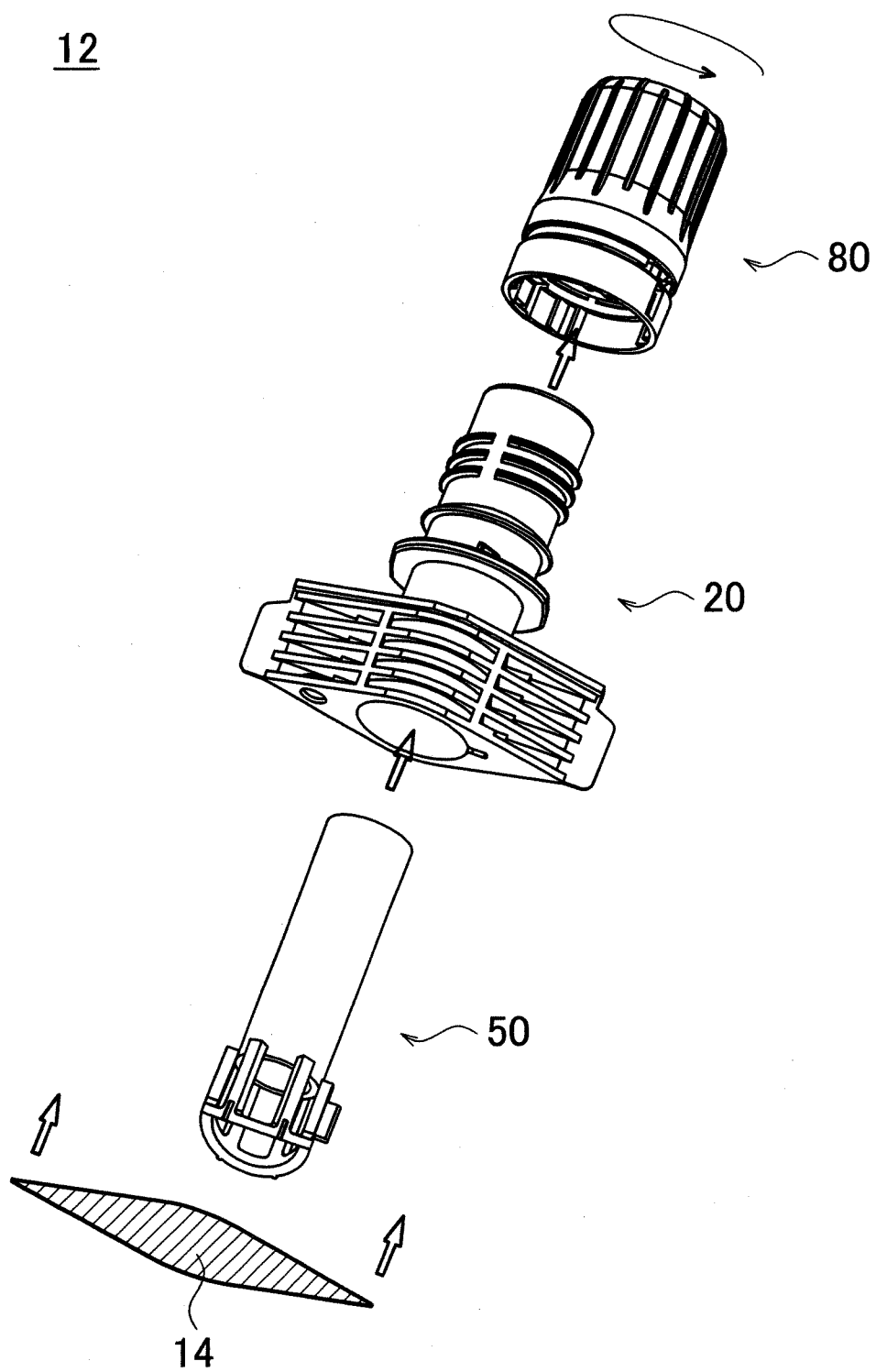
Sectional View IV-IV

(b)

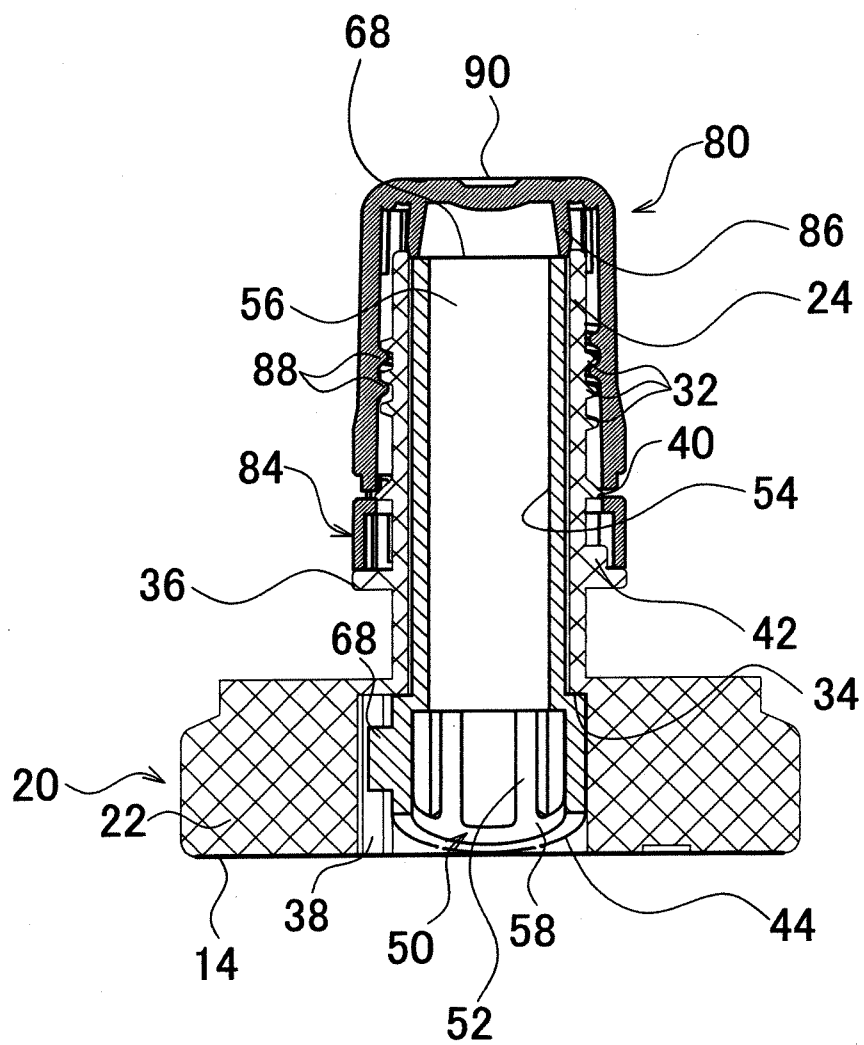


【FIG. 7A】

FIG. 7A

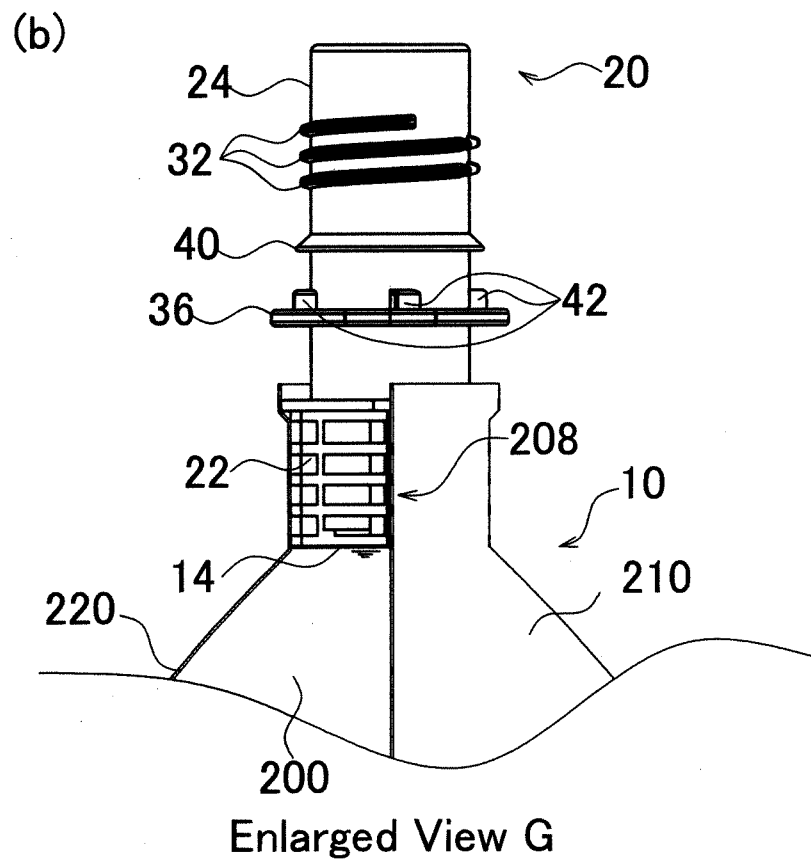
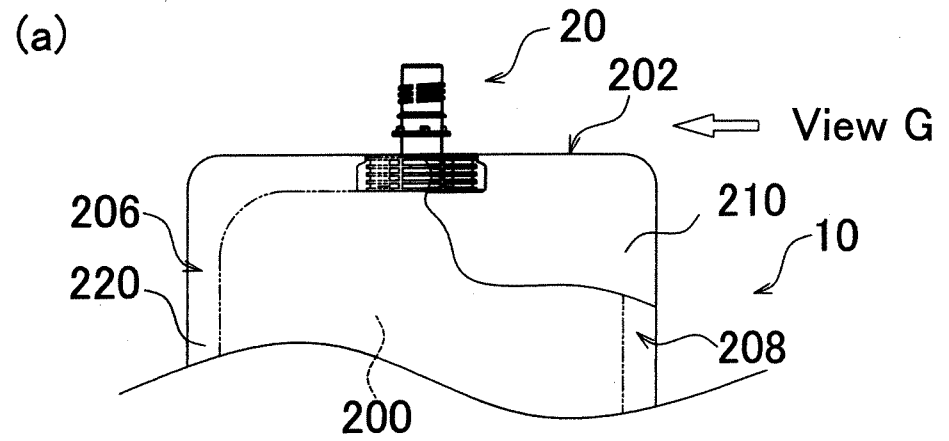
12

12



【FIG. 8】

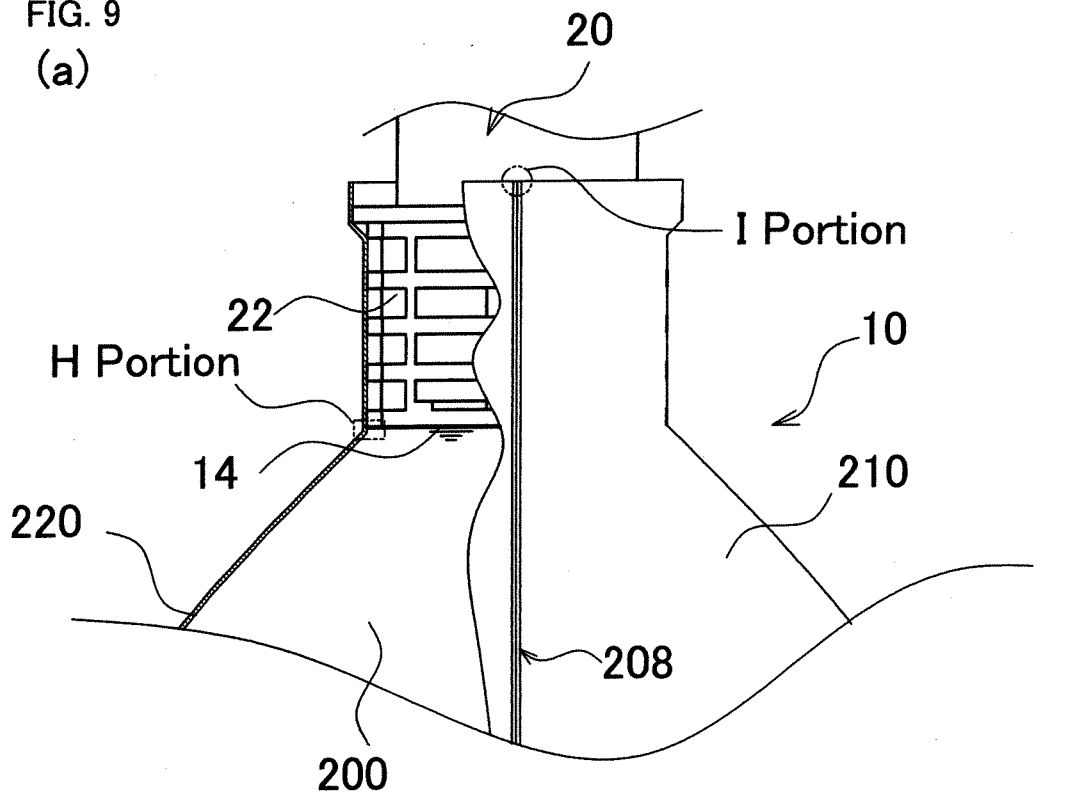
FIG. 8



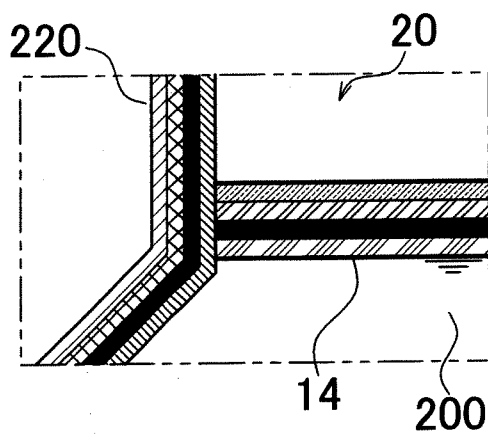
【FIG. 9】

FIG. 9

(a)

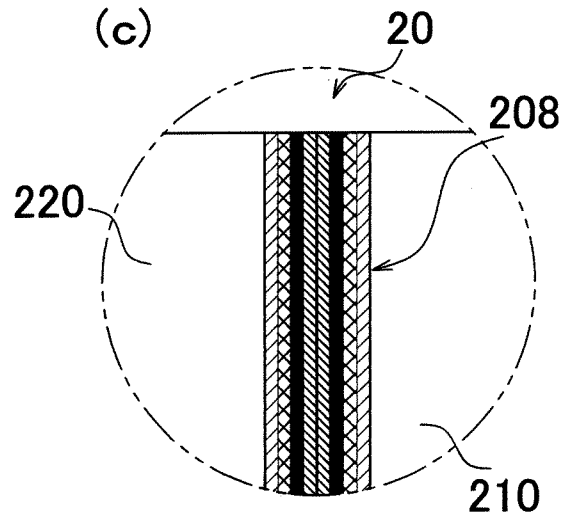


(b)



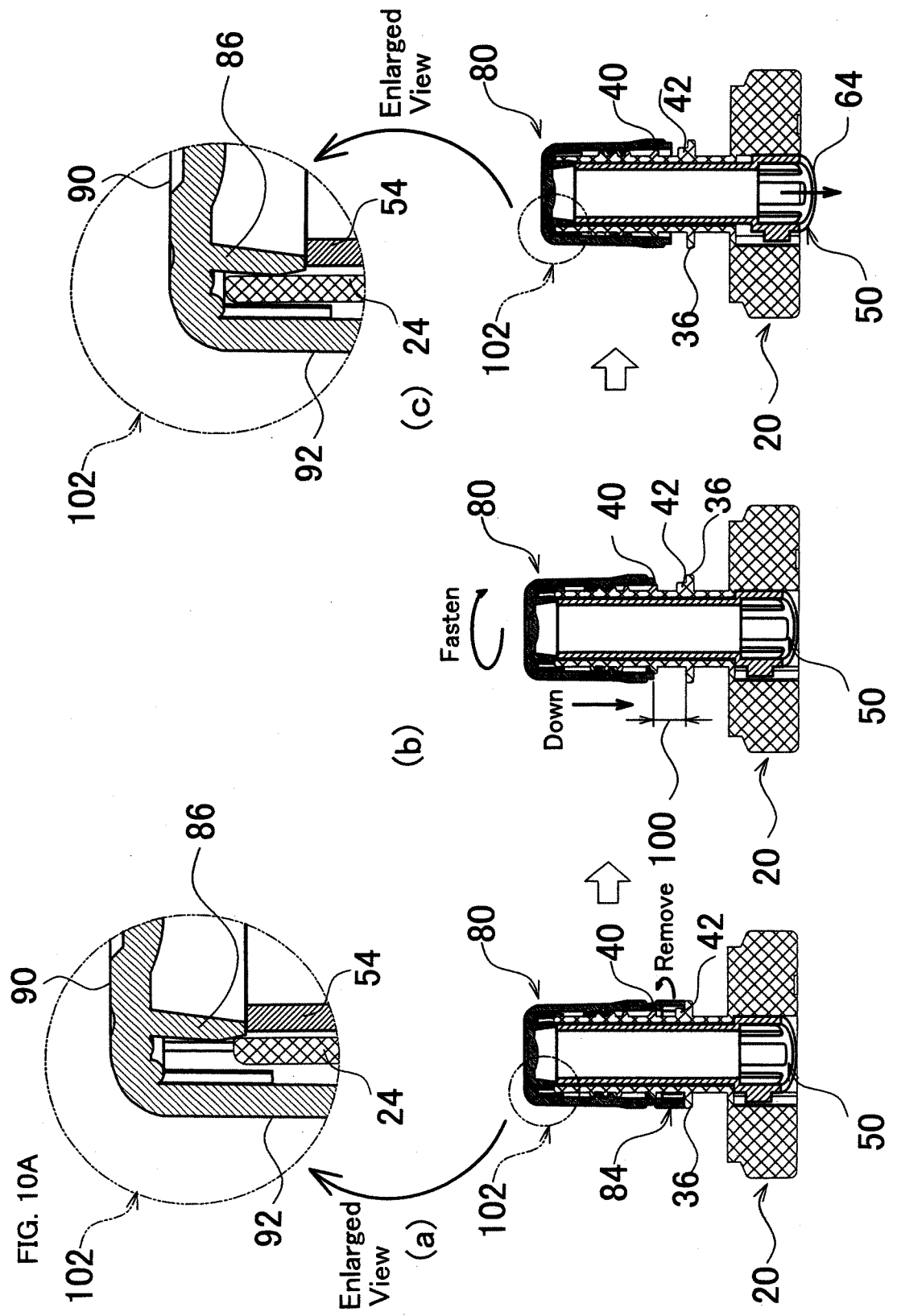
Detail of H Portion

(c)



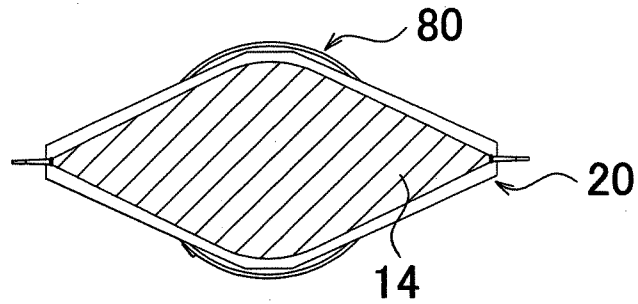
Detail of I Portion

【FIG. 10A】

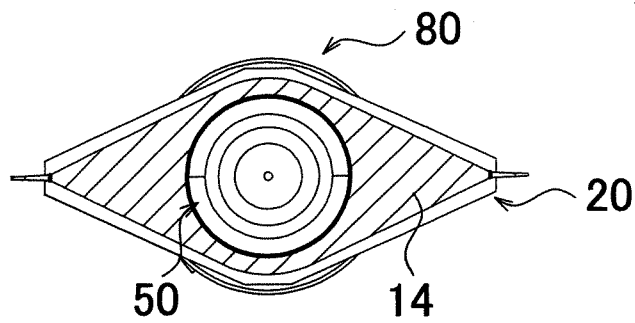


【FIG. 10B】

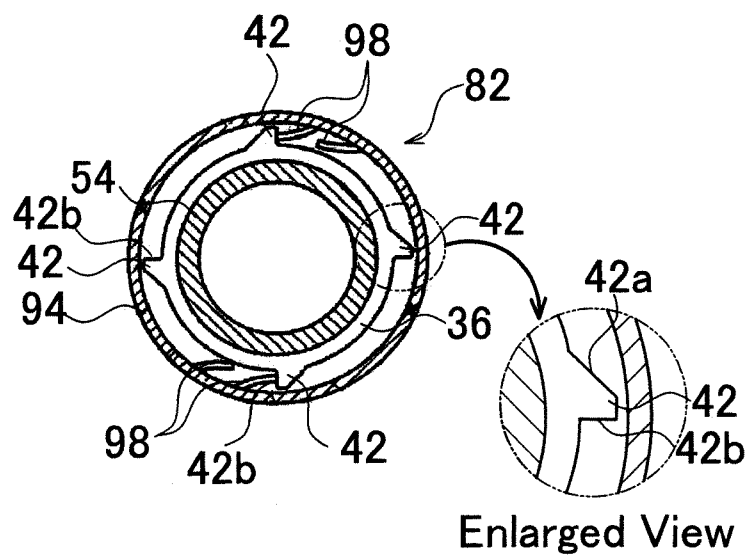
FIG. 10B

12 (a)

(b)



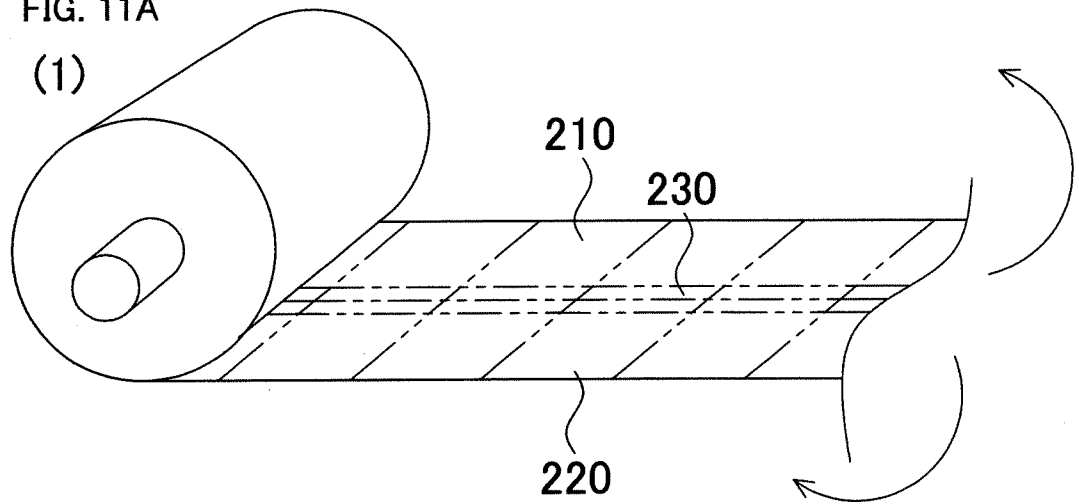
(c)



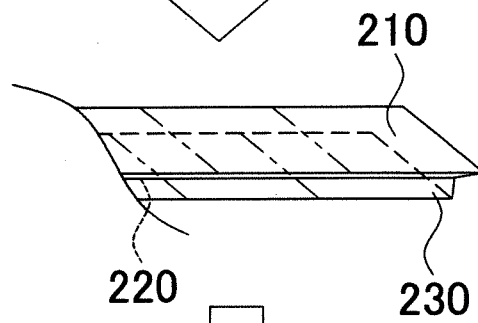
【FIG. 11A】

FIG. 11A

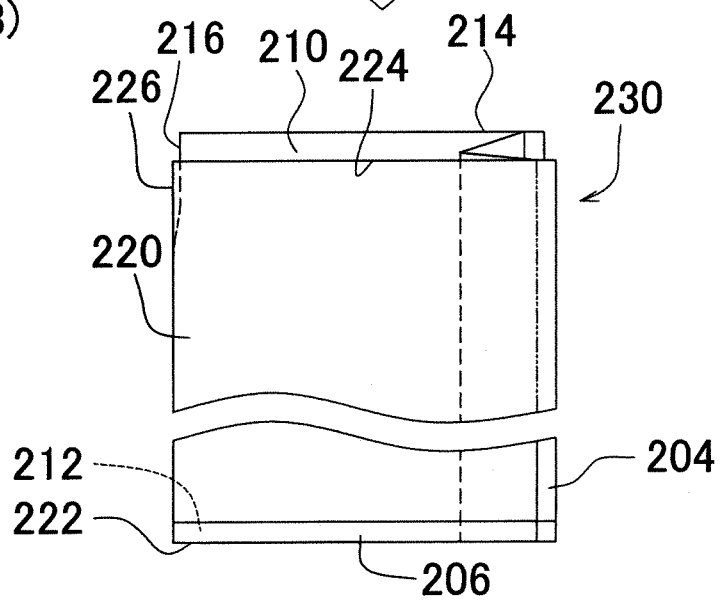
(1)



(2)

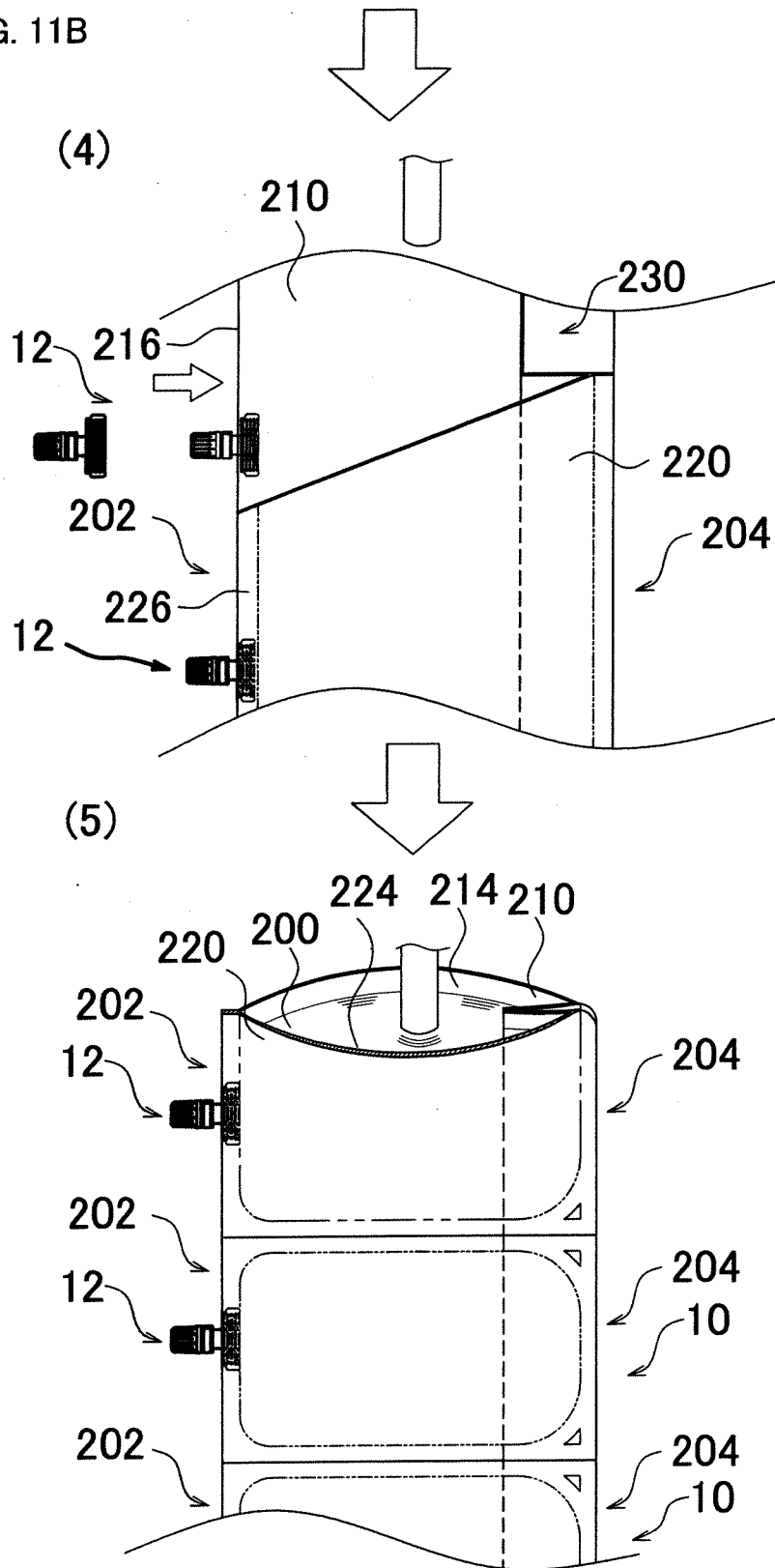


(3)



【FIG. 11B】

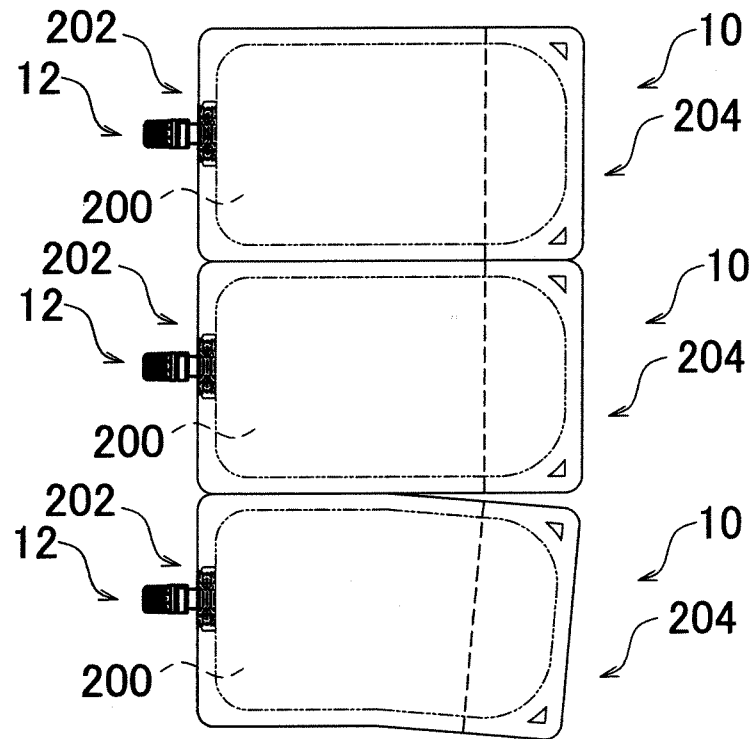
FIG. 11B



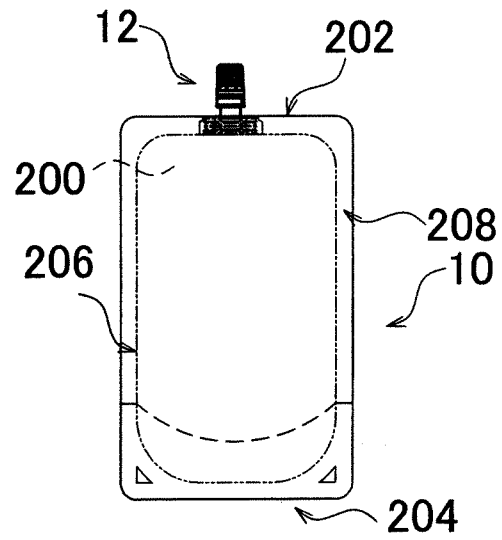
【FIG. 11C】

FIG. 11C

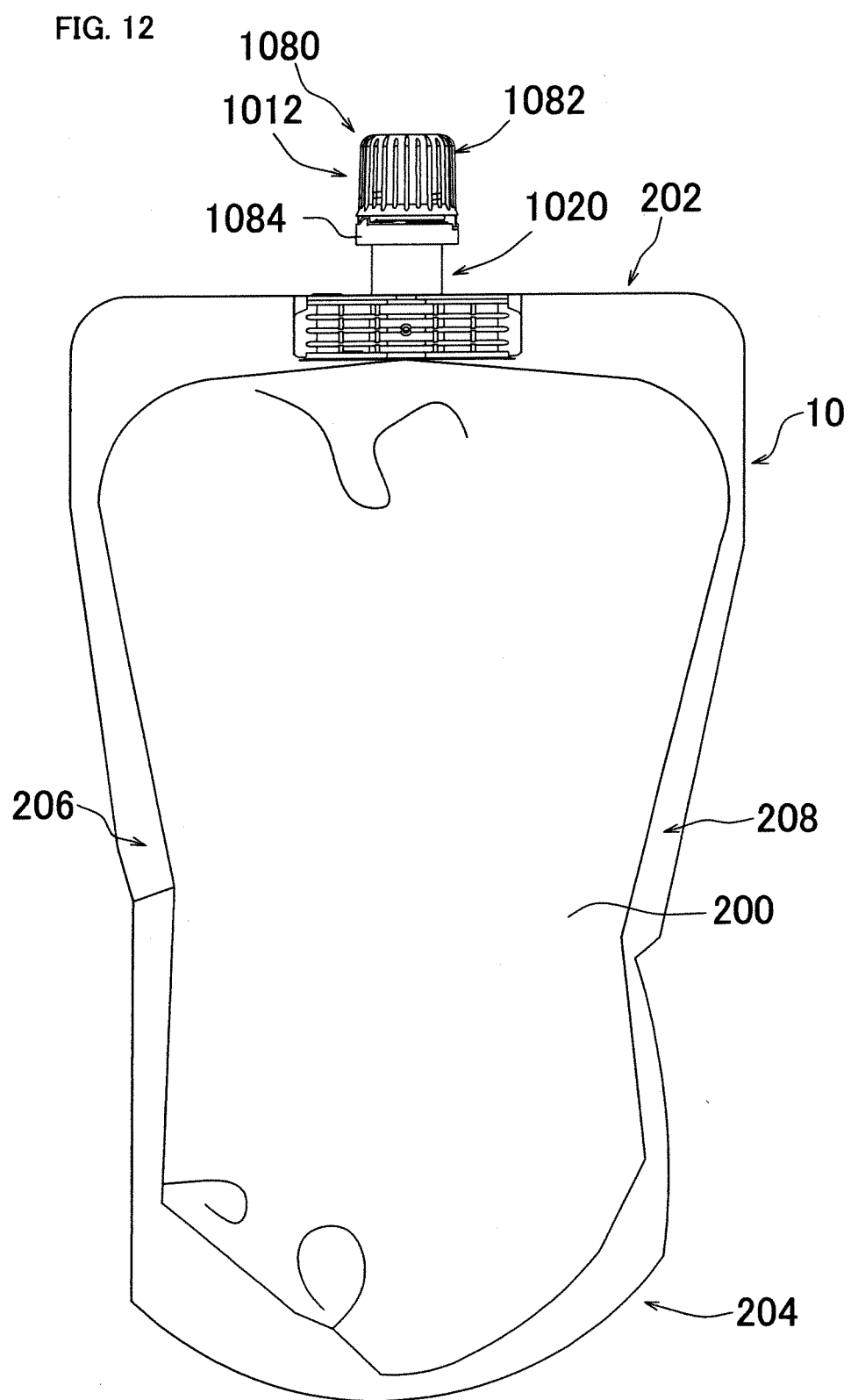
(6)



(7)

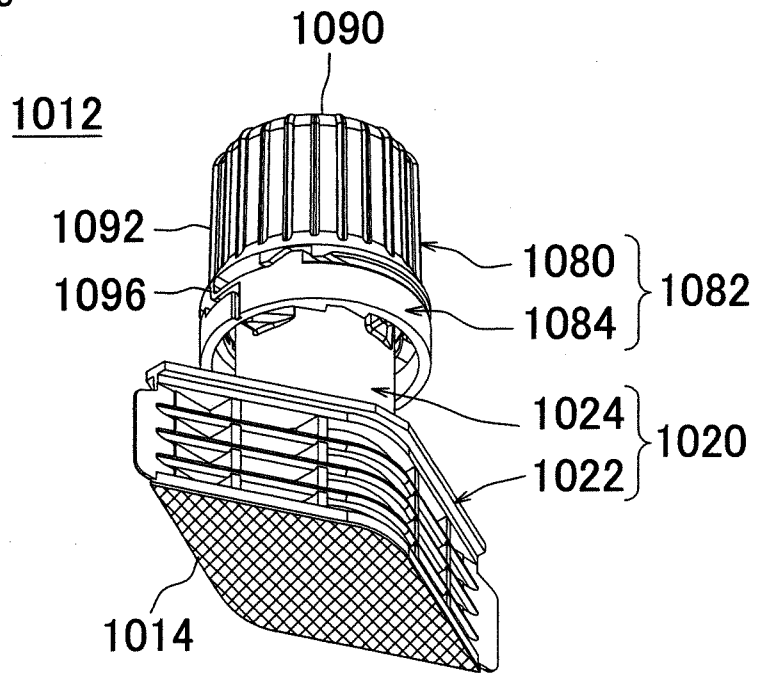


【FIG. 12】



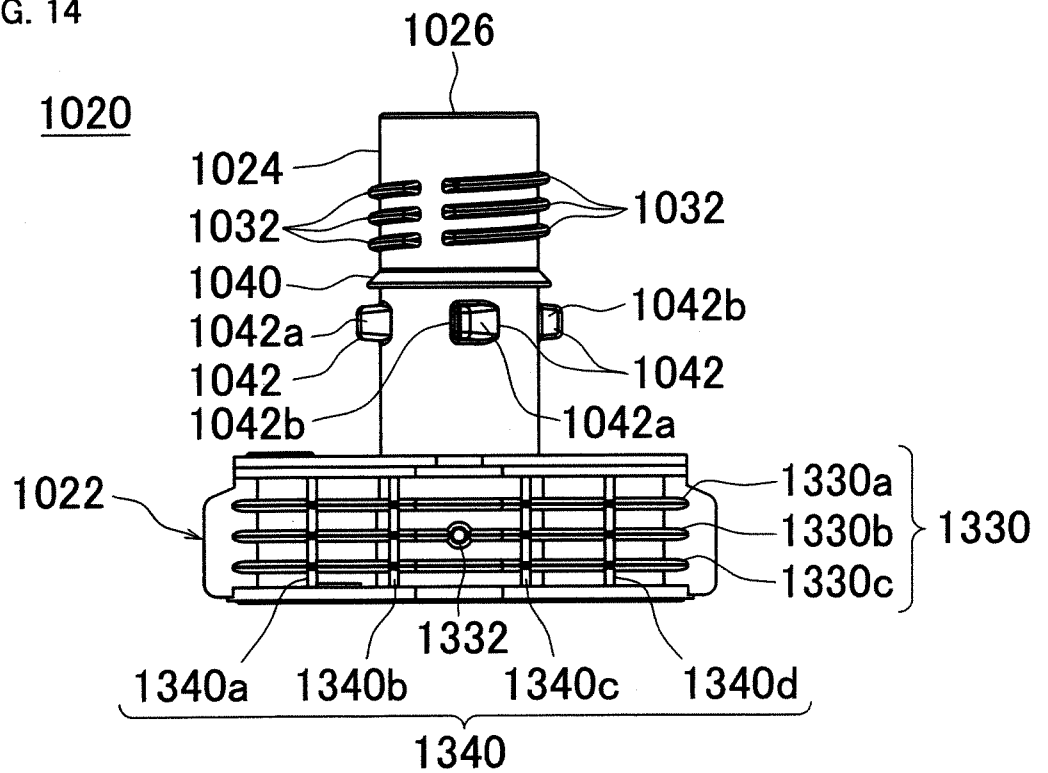
【FIG. 13】

FIG. 13



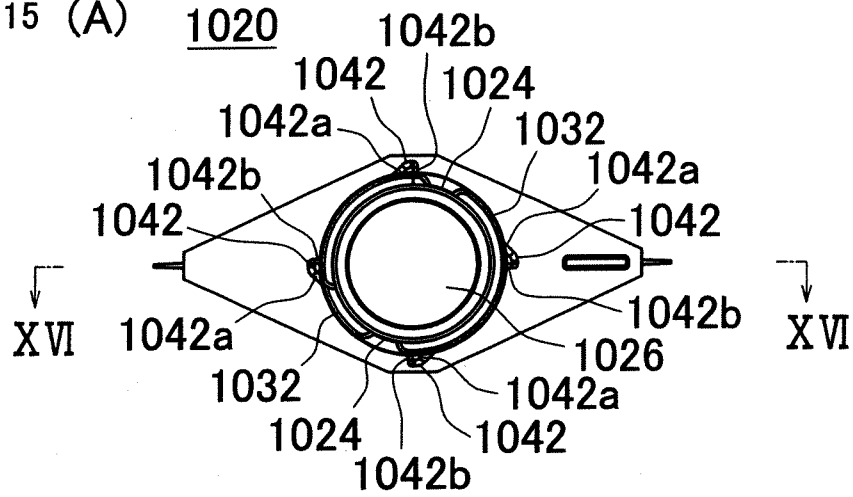
【FIG. 14】

FIG. 14

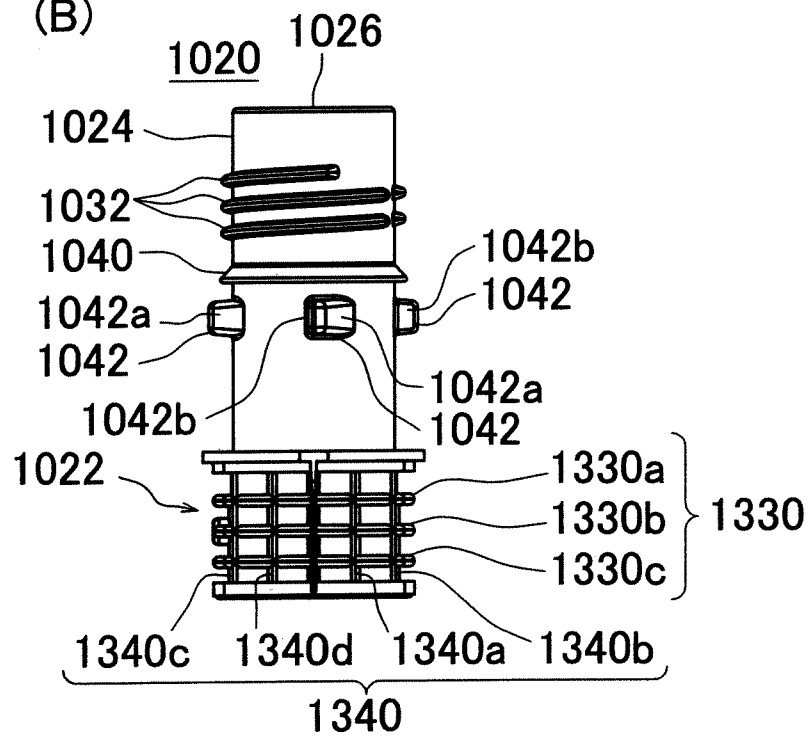


【FIG. 15】

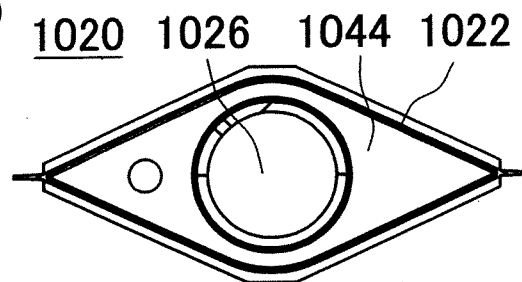
FIG. 15 (A)



(B)

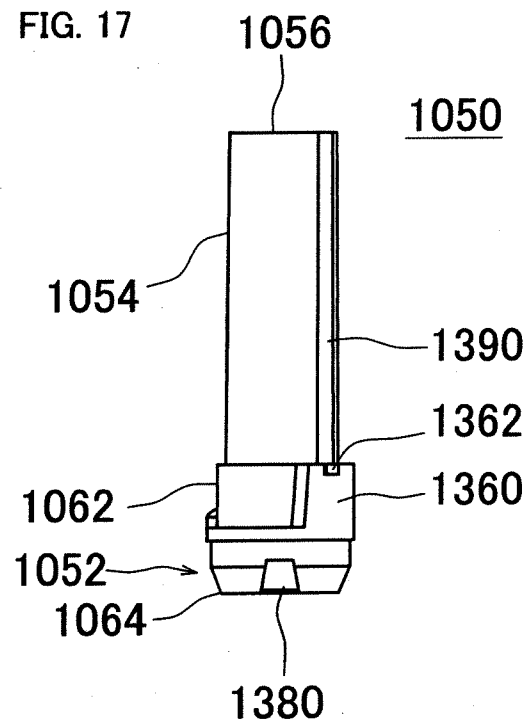


(C)



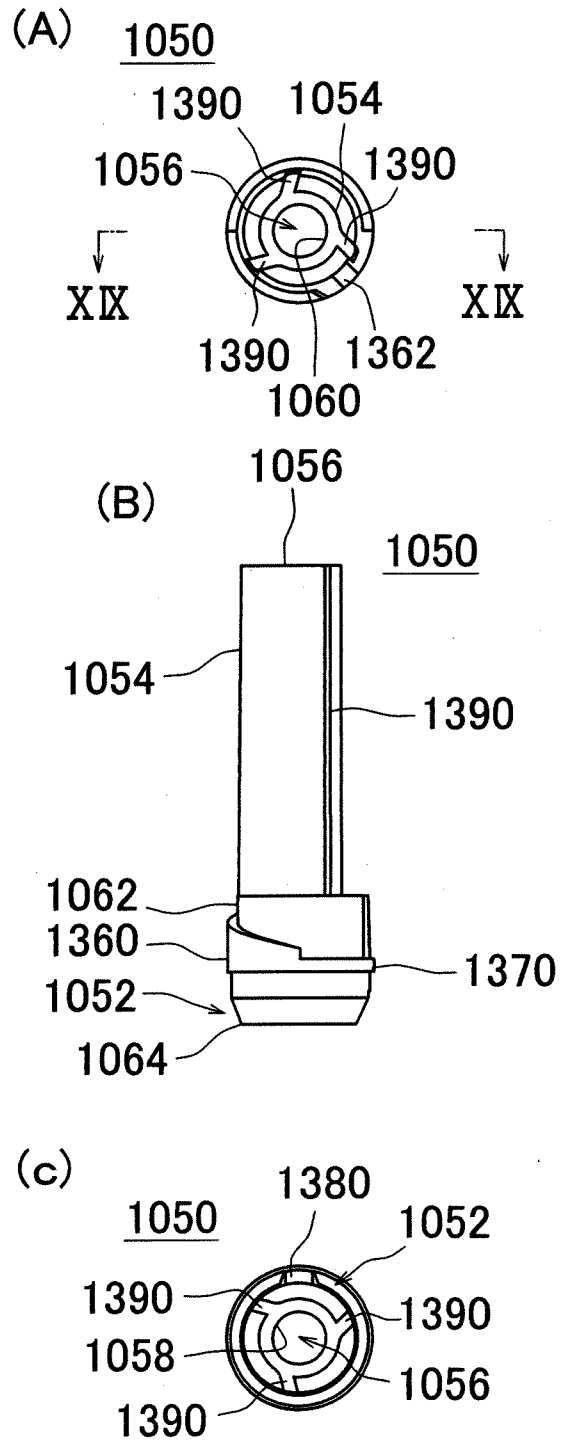
A cross-sectional view of a semiconductor device. A central channel 1028 is formed in a substrate 1022. The channel is bounded by side gates 1024 and 1032. The gates are connected to a common gate terminal 1030. The channel is also connected to a common gate terminal 1030. The device includes a gate stack 1040 and a gate electrode 1042. The channel is formed in a substrate 1022. The channel is bounded by side gates 1024 and 1032. The gates are connected to a common gate terminal 1030. The channel is also connected to a common gate terminal 1030. The device includes a gate stack 1040 and a gate electrode 1042.

【FIG. 17】



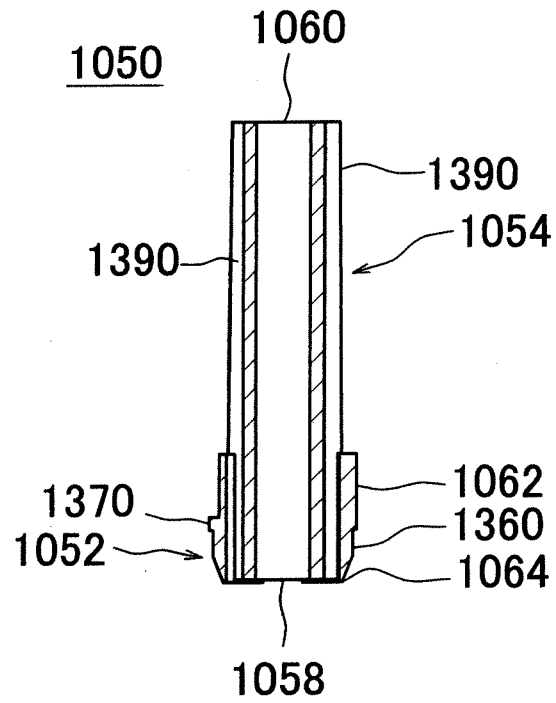
【FIG. 18】

FIG. 18



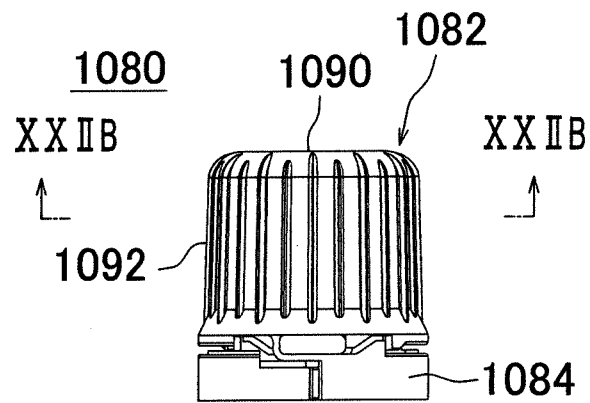
【FIG. 19】

FIG. 19



【FIG. 20】

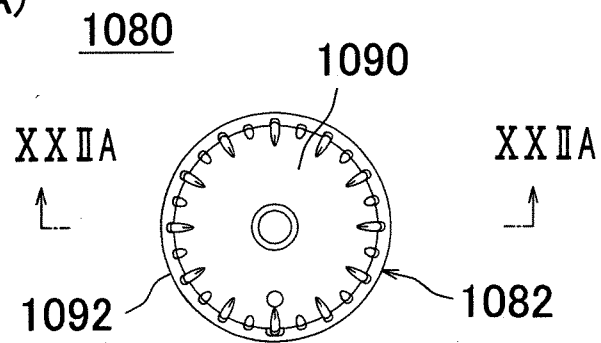
FIG. 20



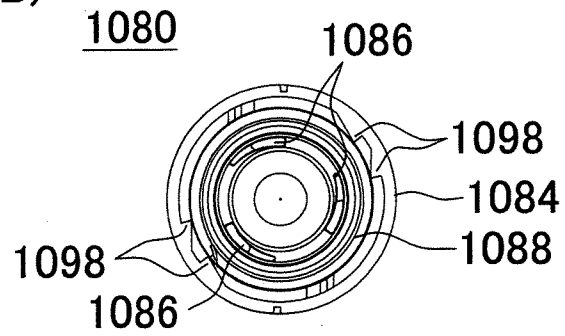
【FIG. 21】

FIG. 21

(A)

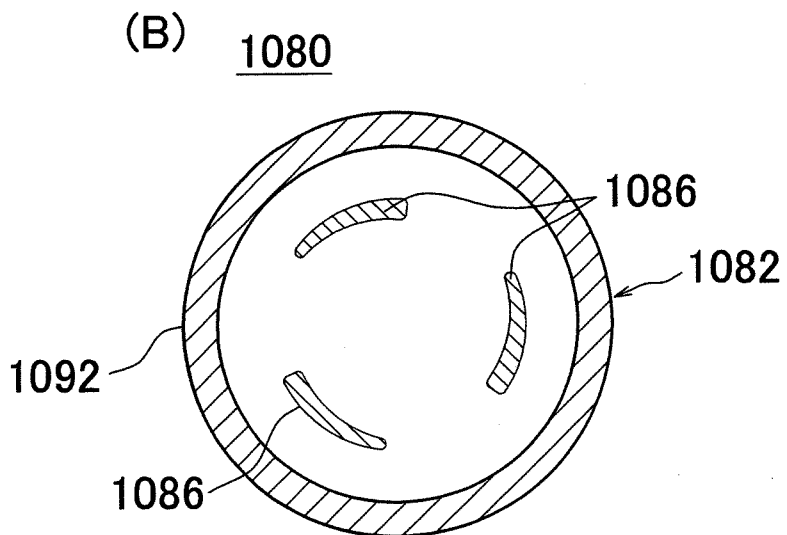
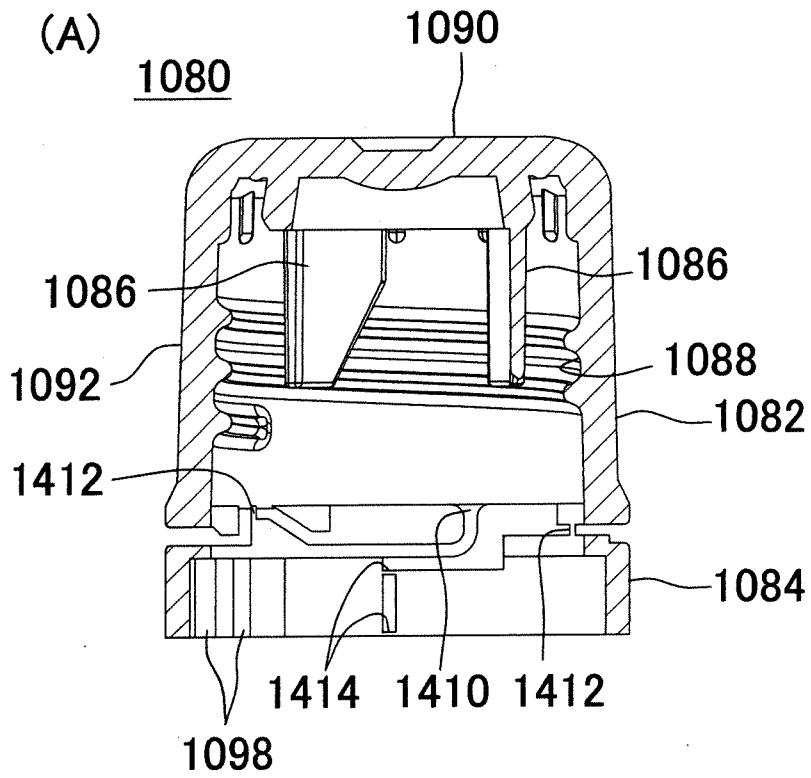


(B)



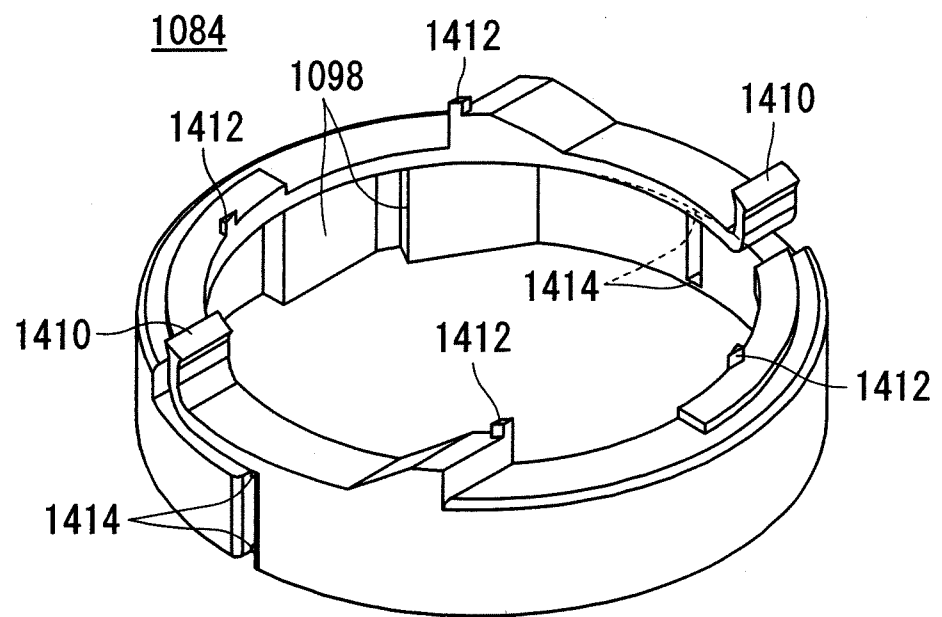
【FIG. 22】

FIG. 22



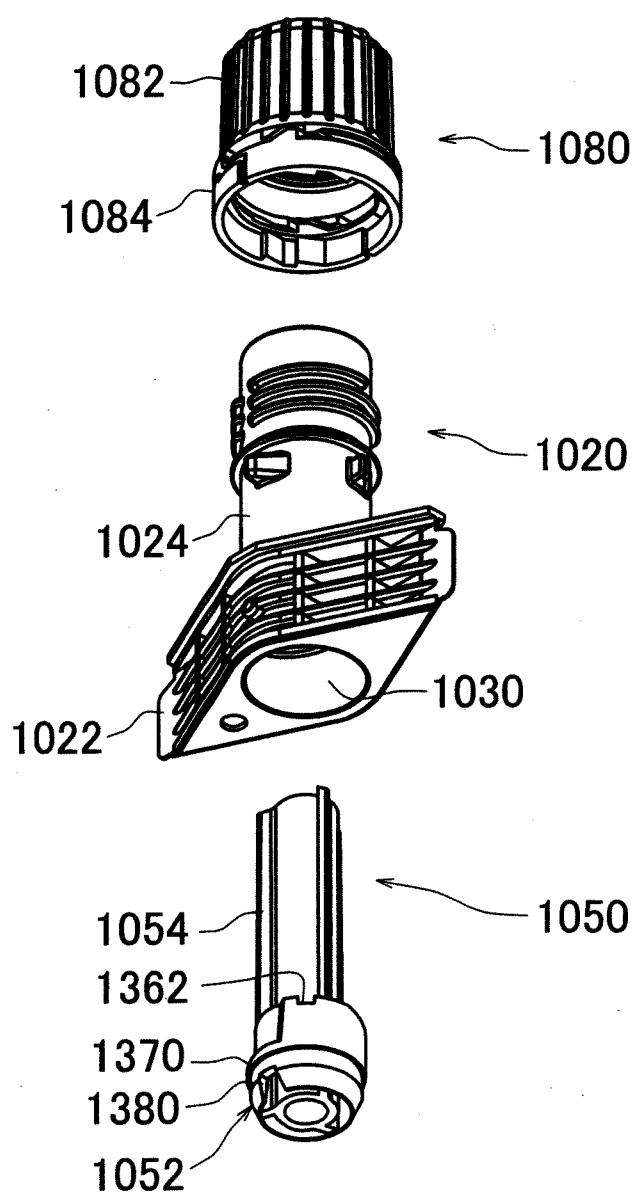
【FIG. 23】

FIG. 23



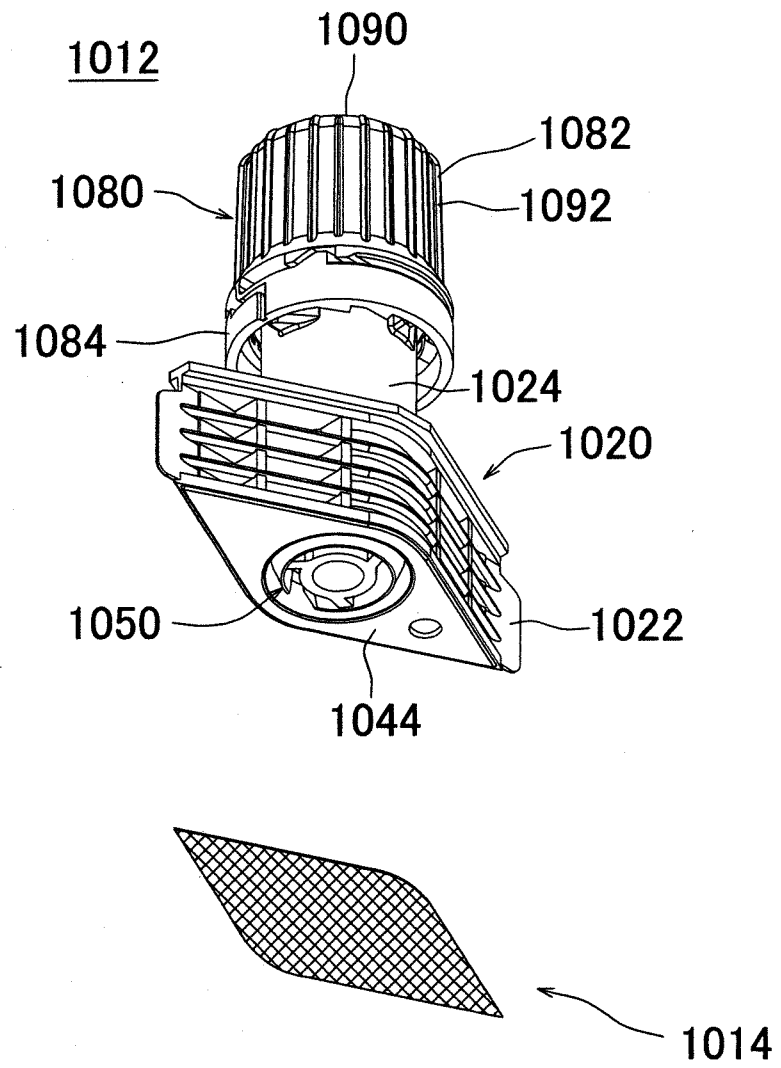
【FIG. 24】

FIG. 24



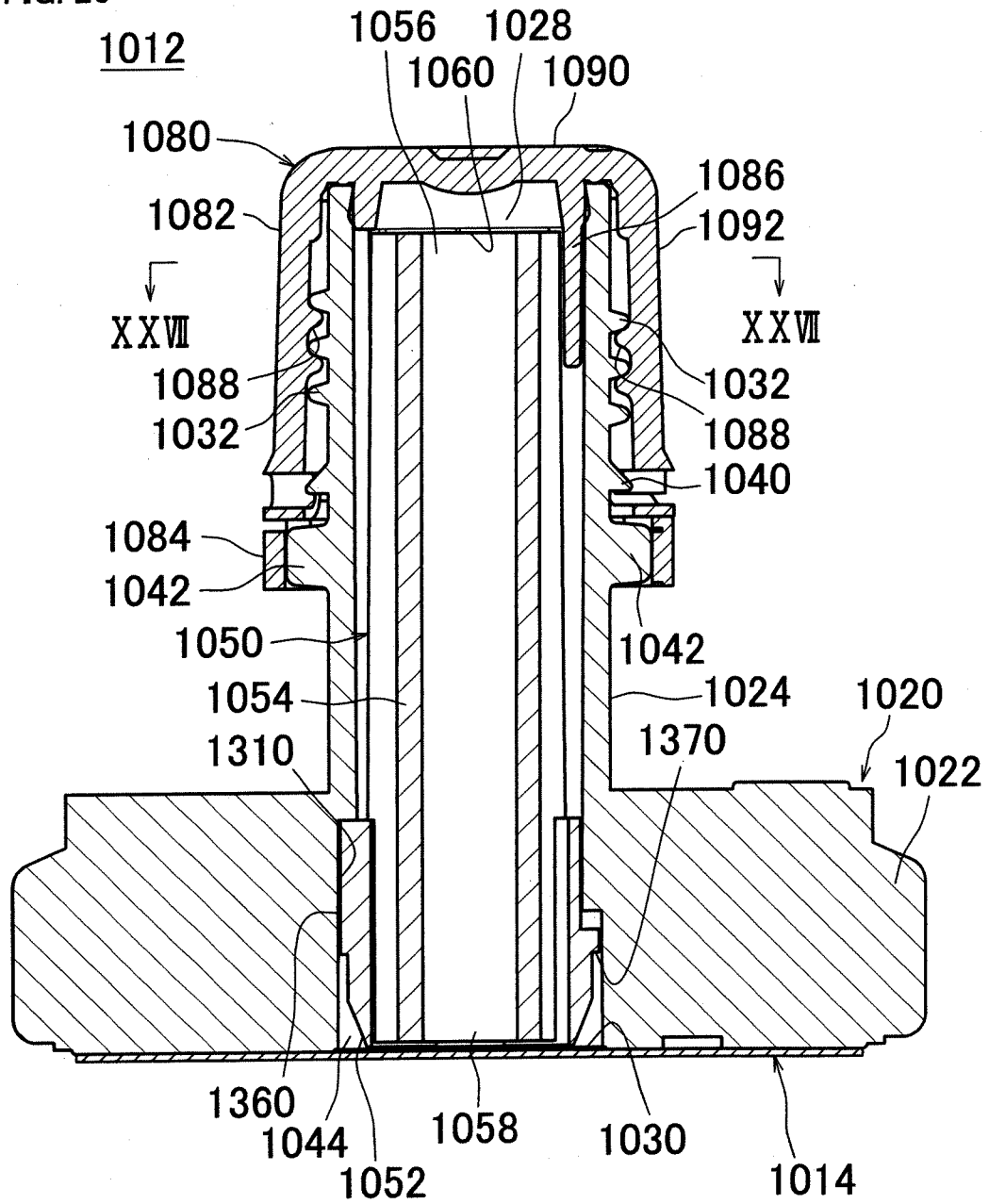
【FIG. 25】

FIG. 25



【FIG. 26】

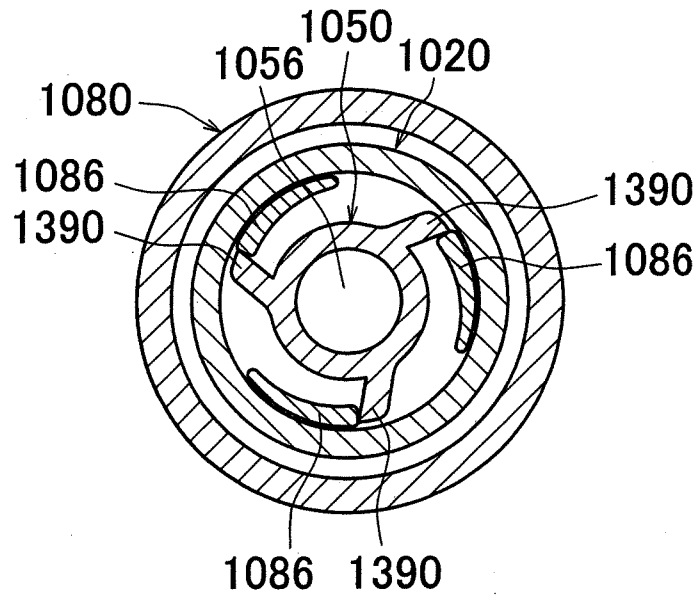
FIG. 26



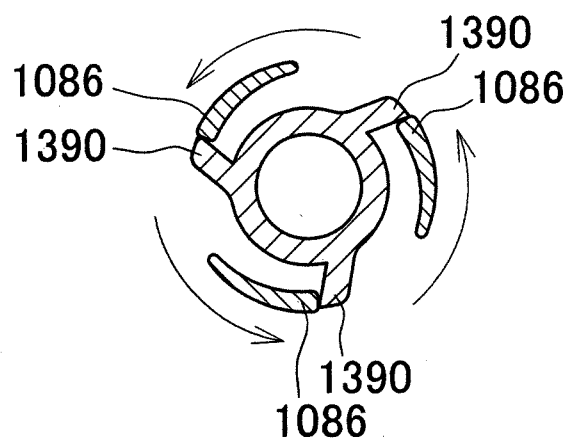
【FIG. 27】

FIG. 27

(A)

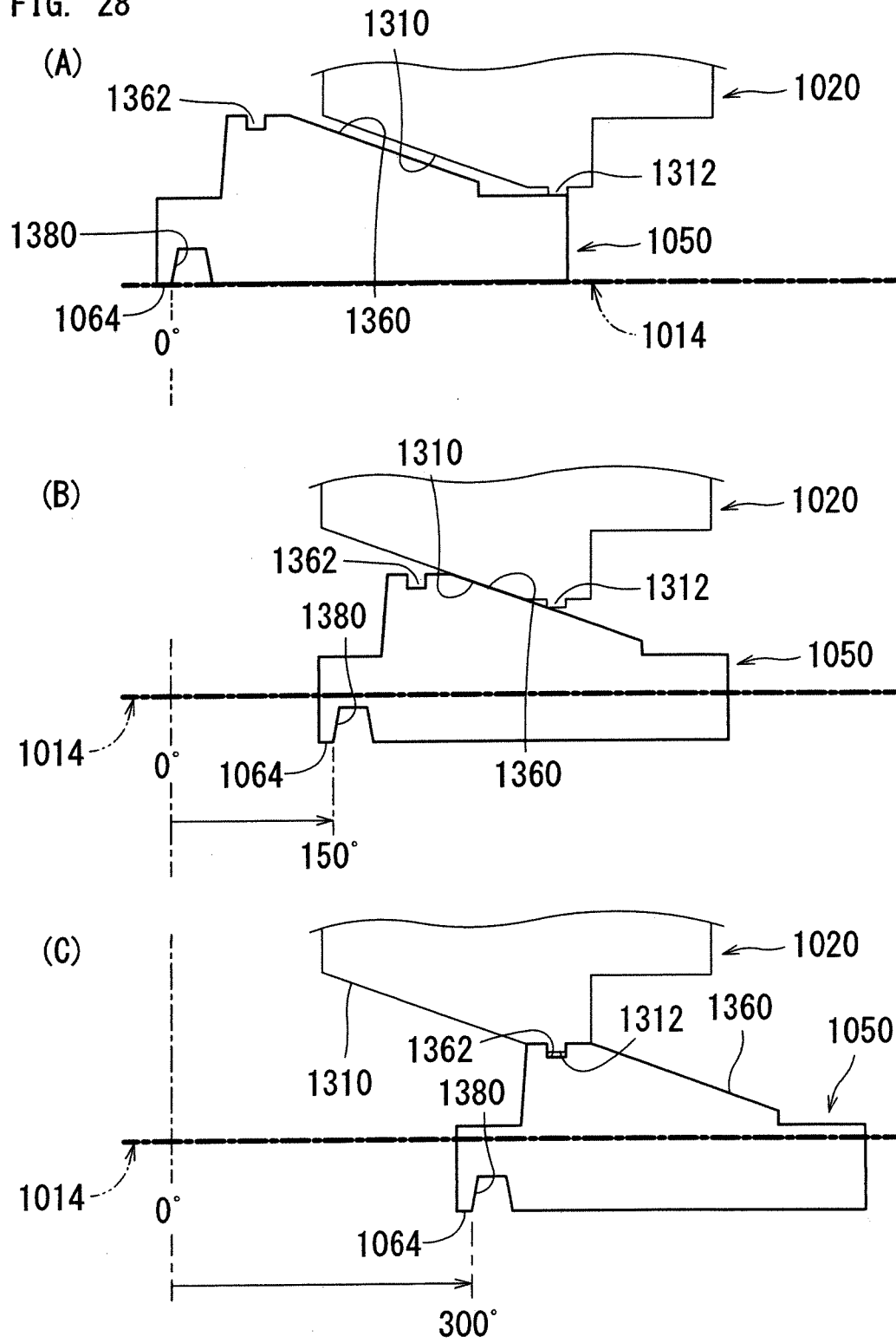
1012

(B)



【FIG. 28】

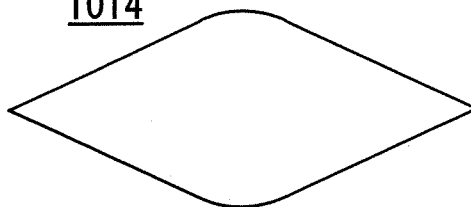
FIG. 28



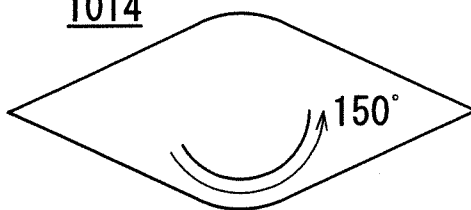
【FIG. 29】

FIG. 29

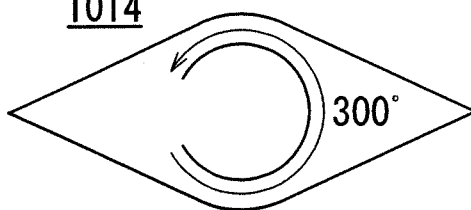
(A)

1014

(B)

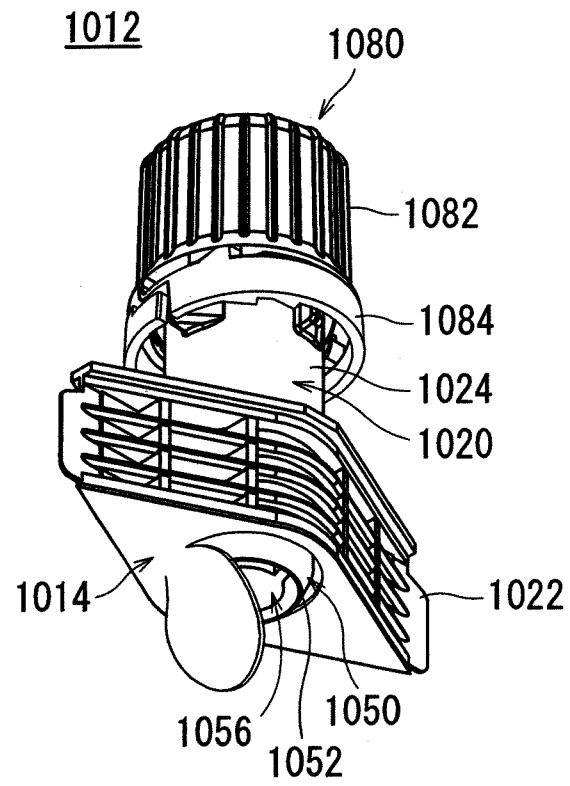
1014

(C)

1014

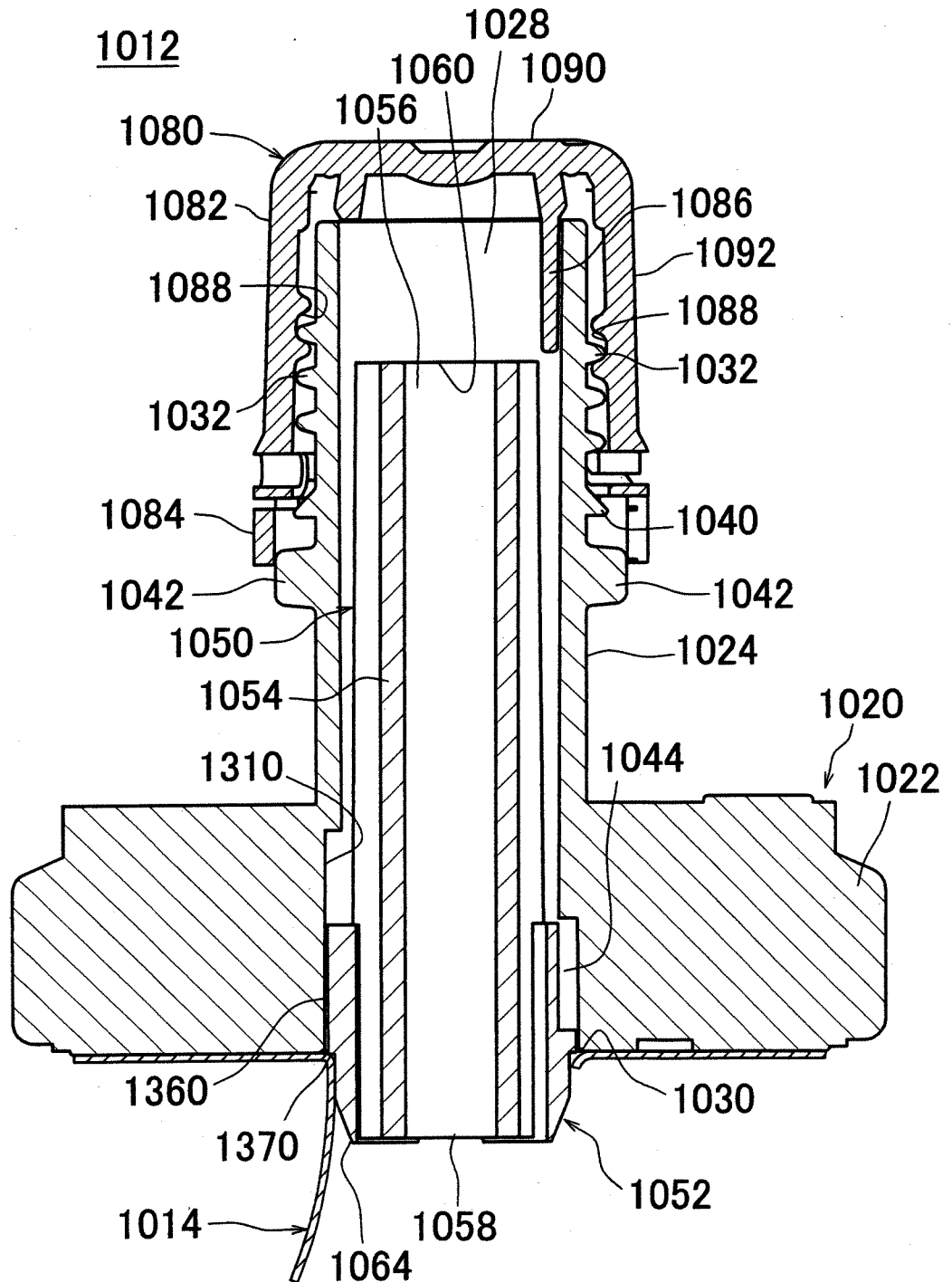
【FIG. 30】

FIG. 30



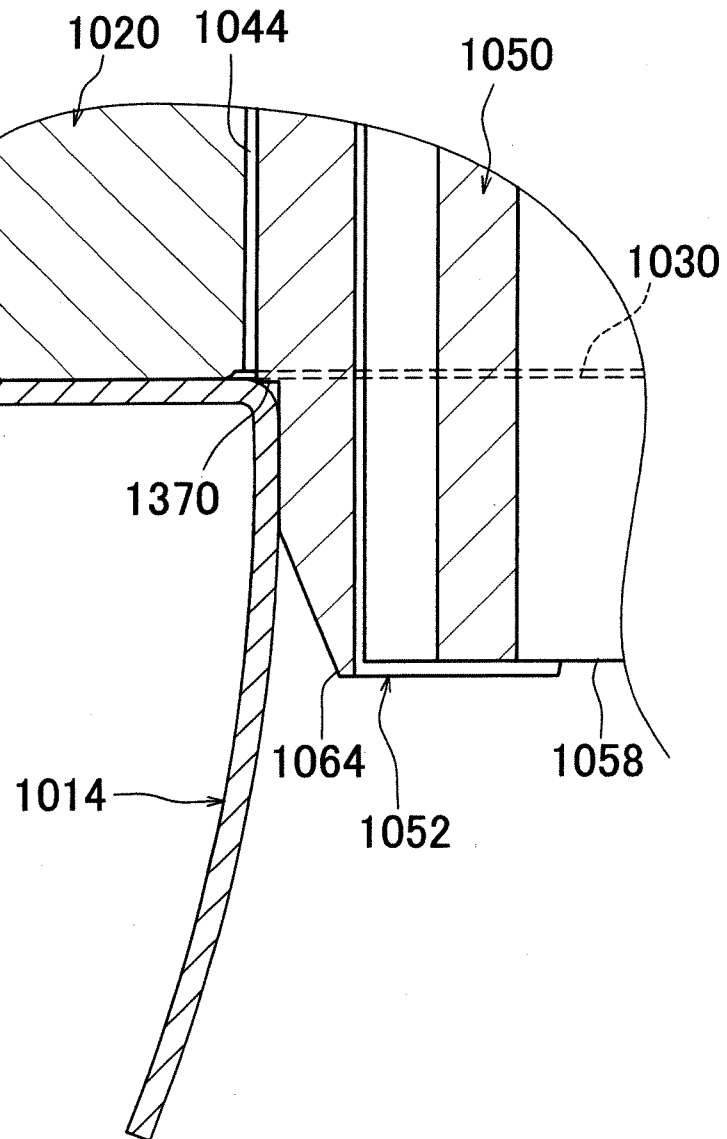
【FIG. 31】

FIG. 31



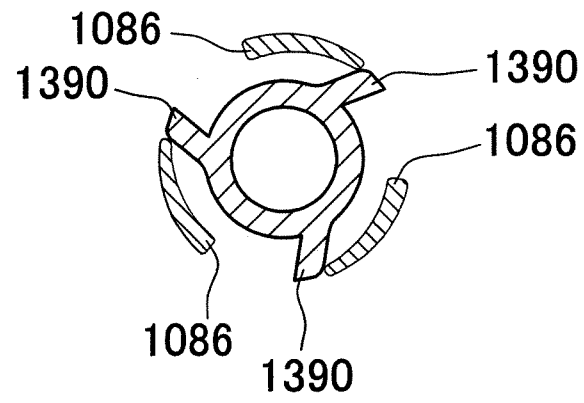
【FIG. 32】

FIG. 32

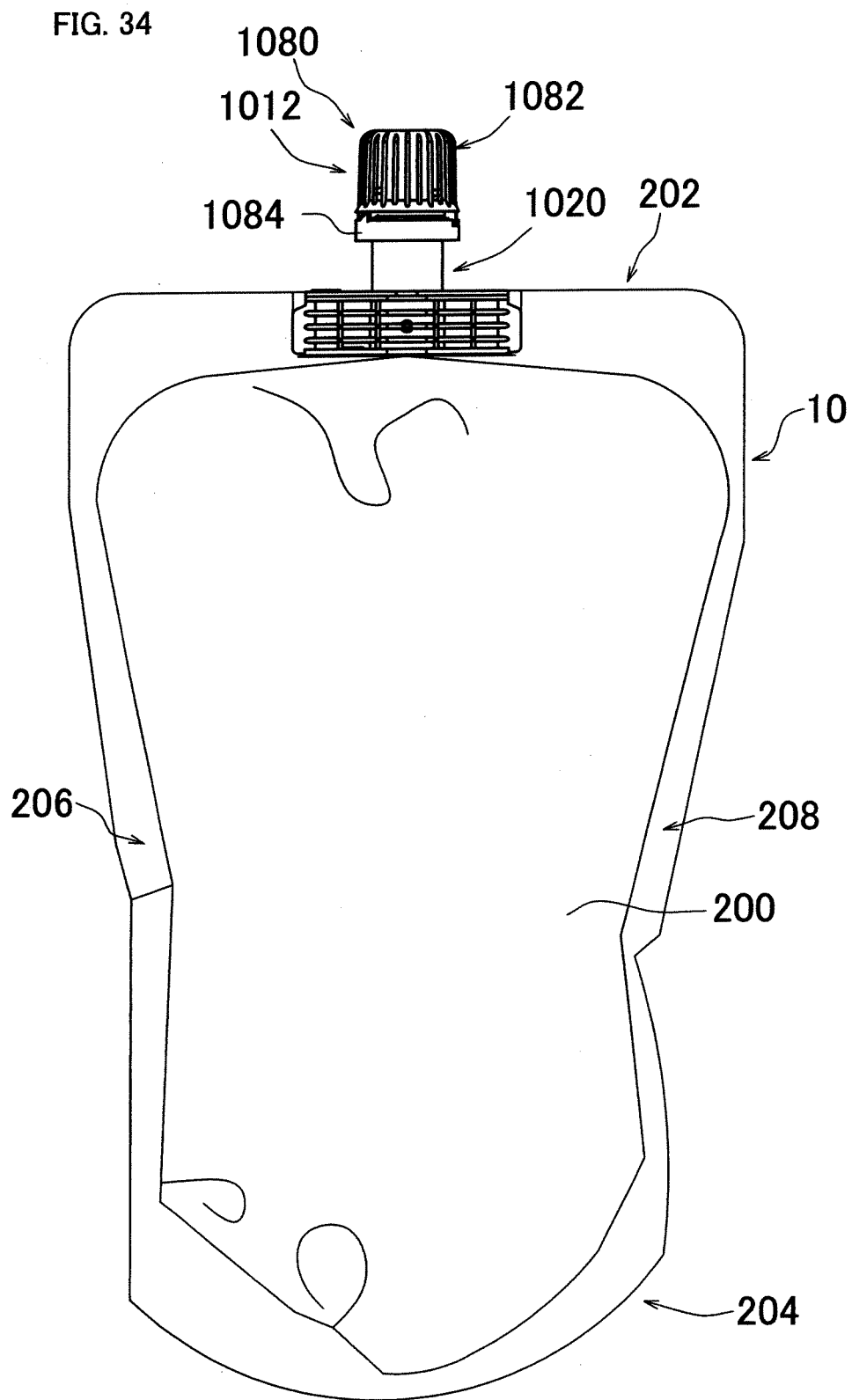


【FIG. 33】

FIG. 33

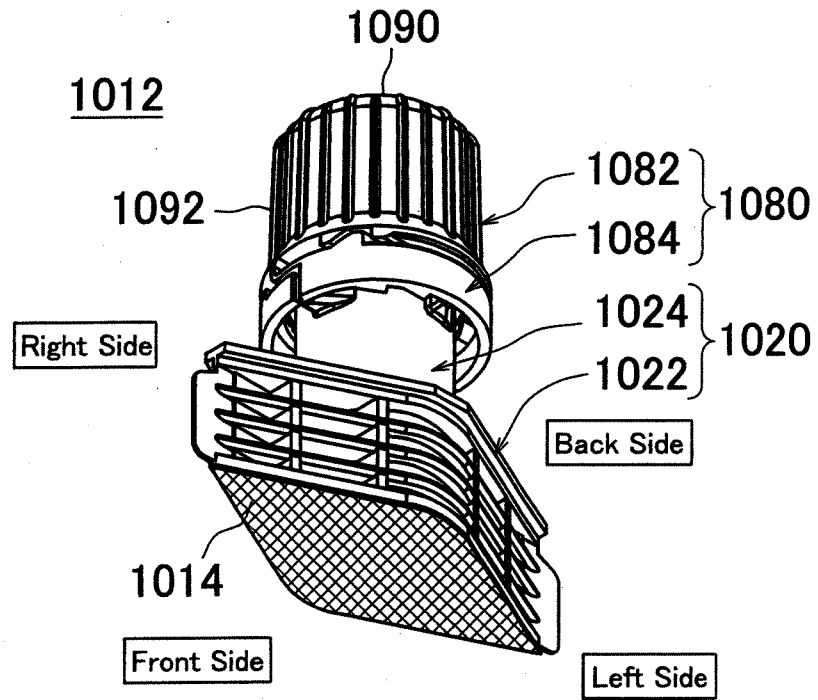


【FIG. 34】



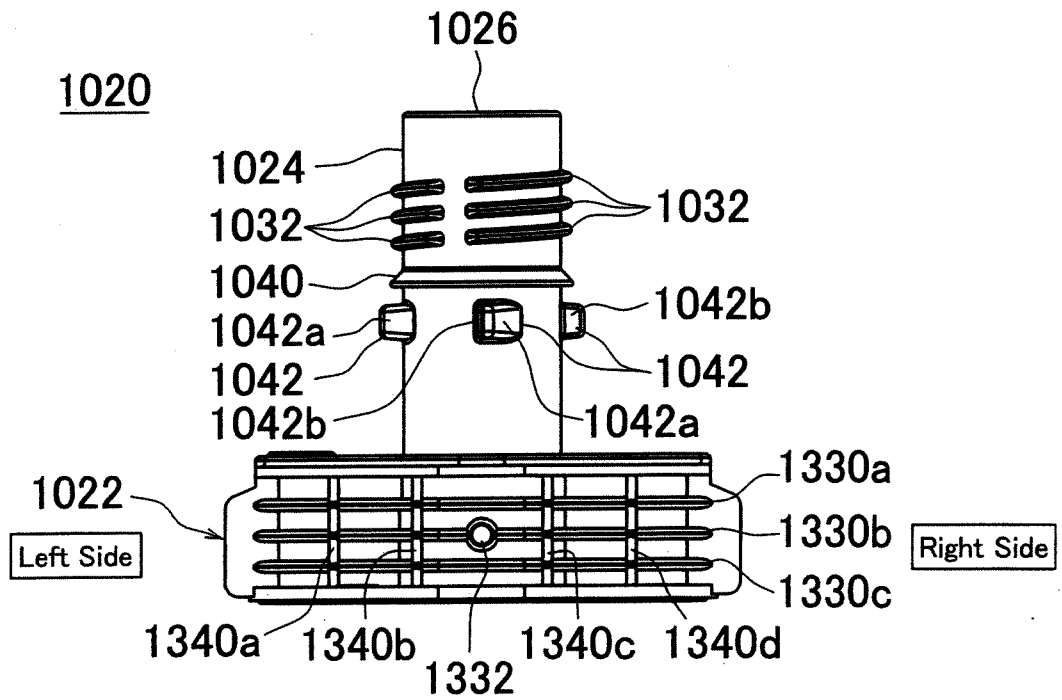
【FIG. 35】

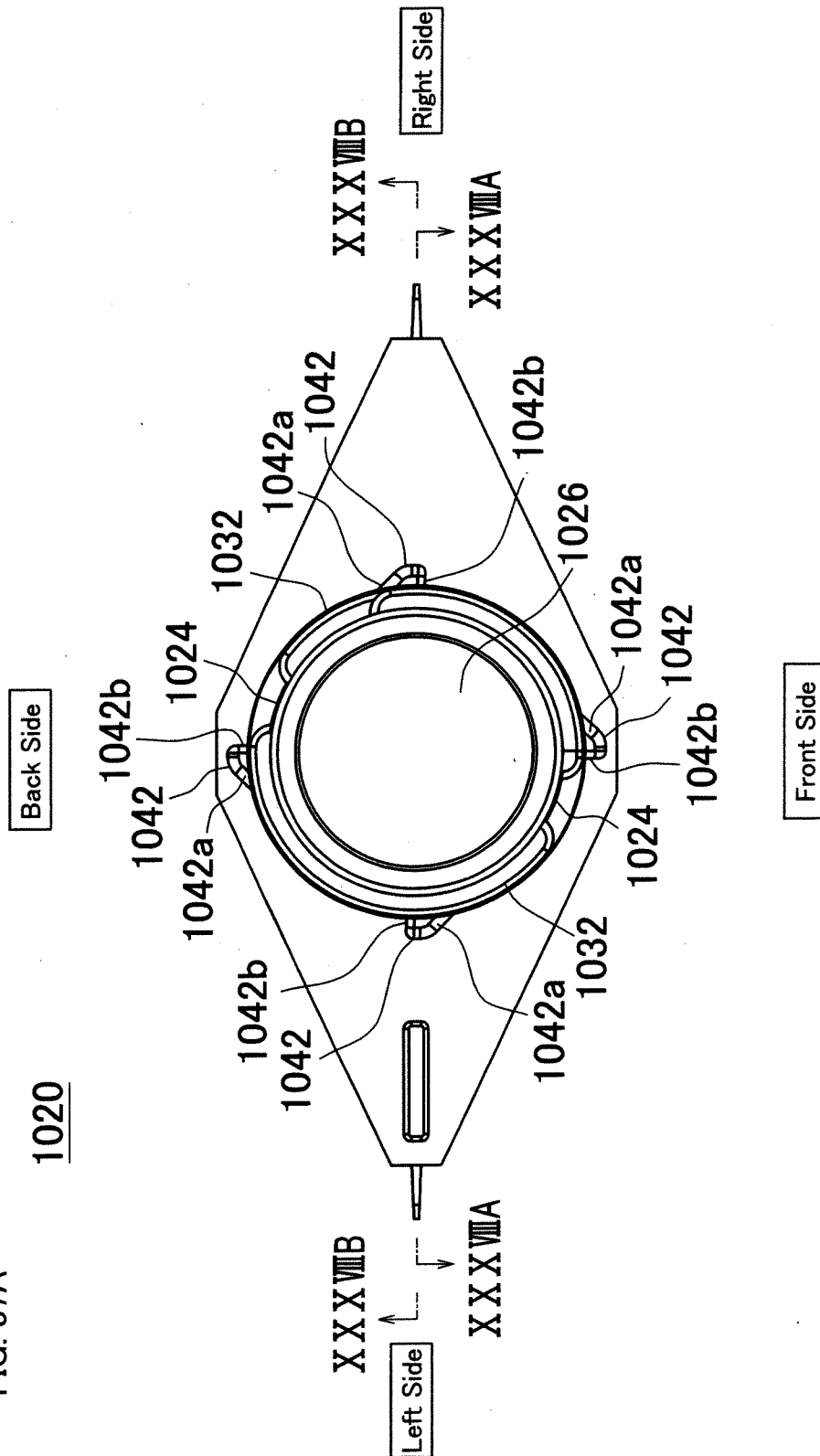
FIG. 35



【FIG. 36】

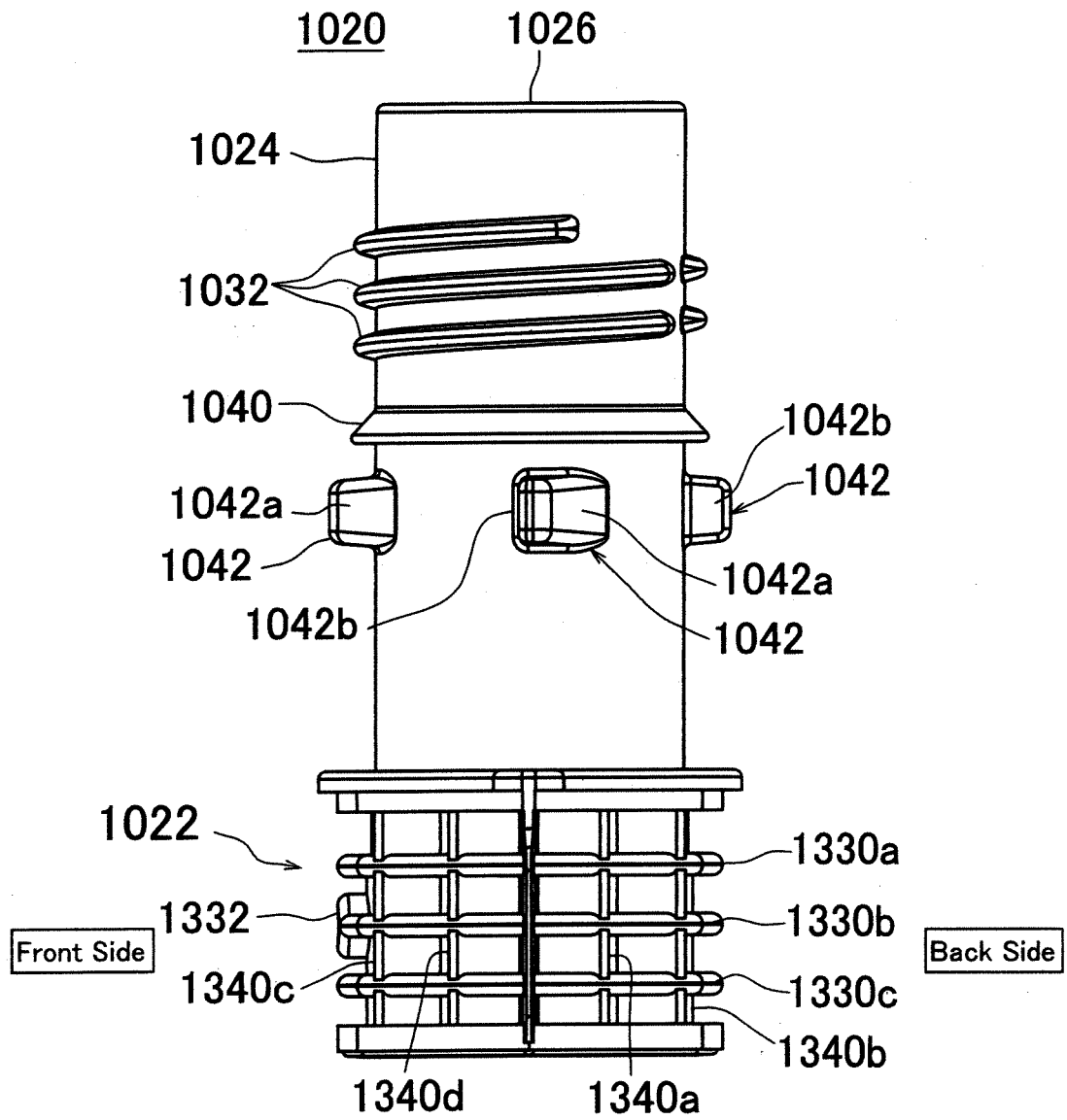
FIG. 36



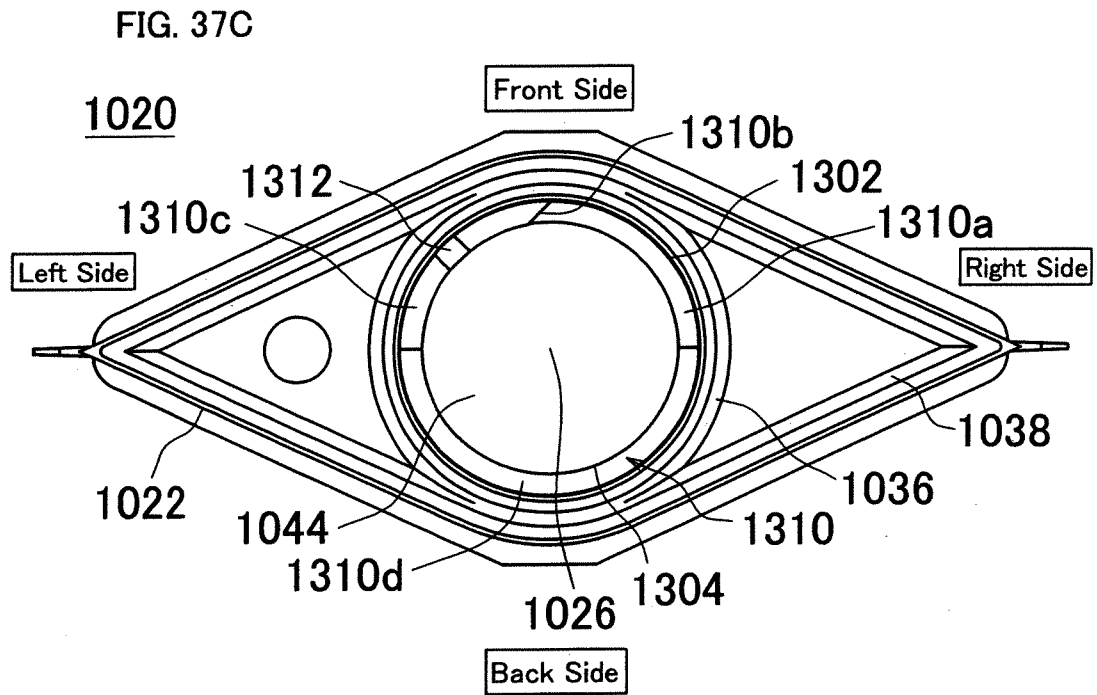
1020

【FIG. 37B】

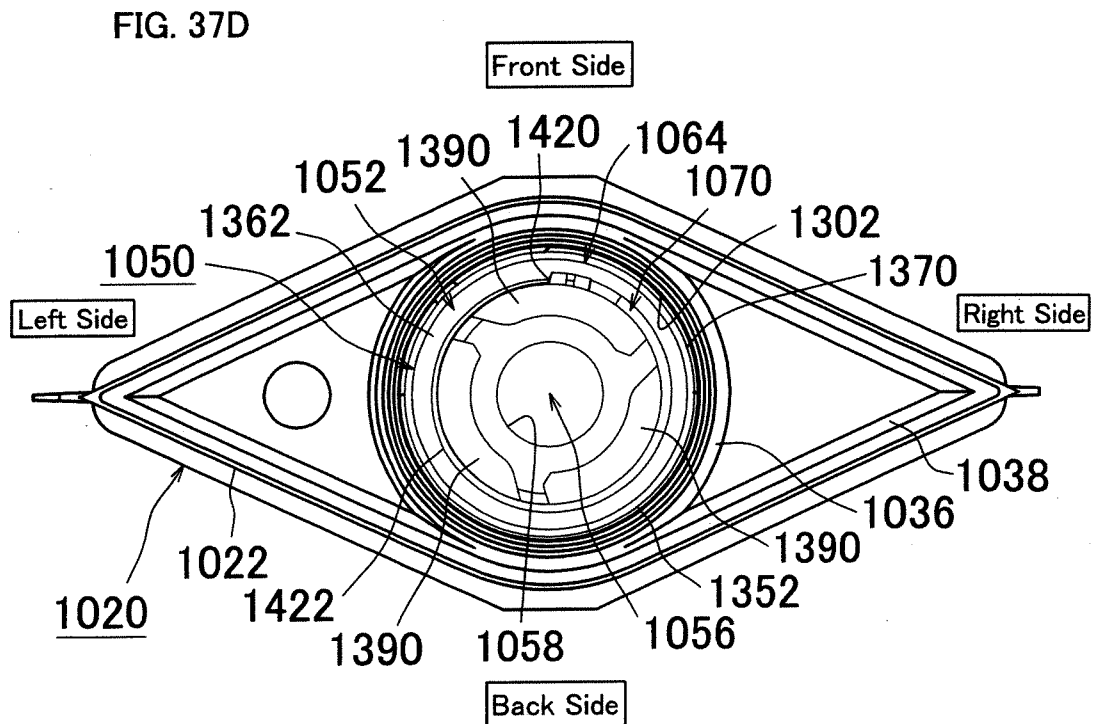
FIG. 37B



【FIG. 37C】



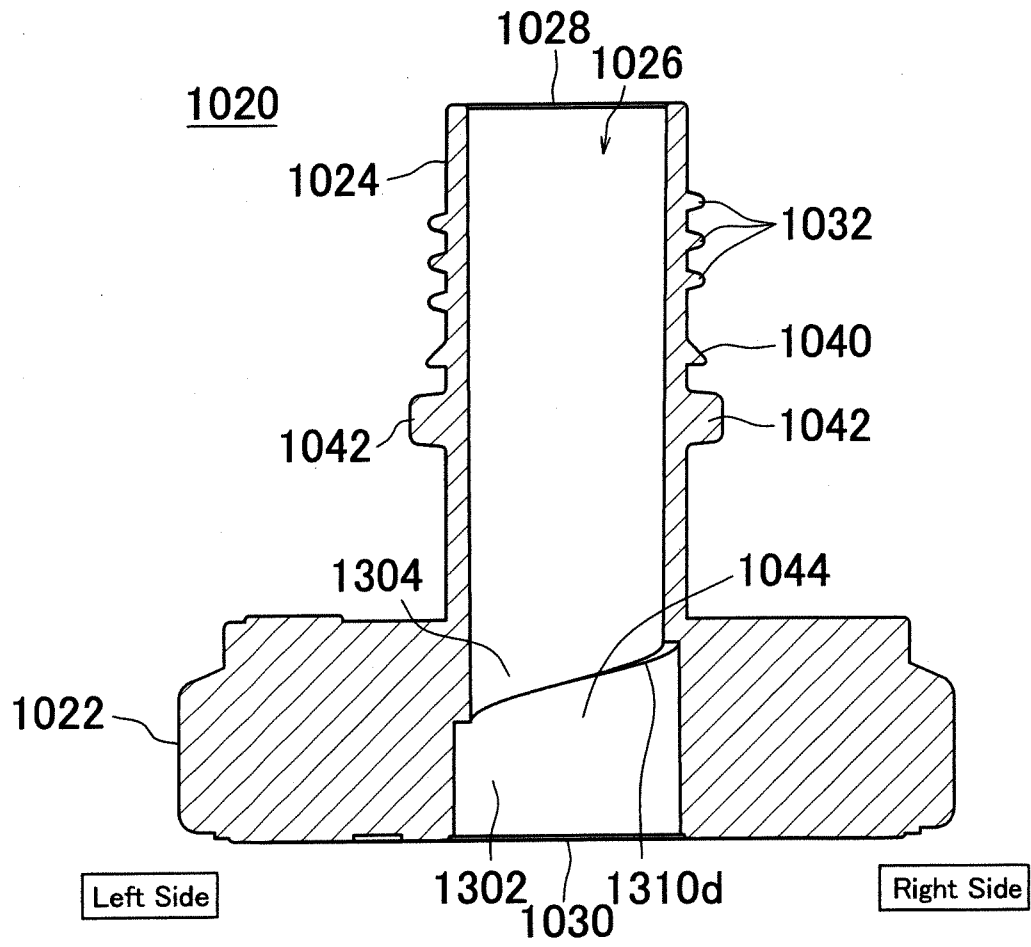
【FIG. 37D】



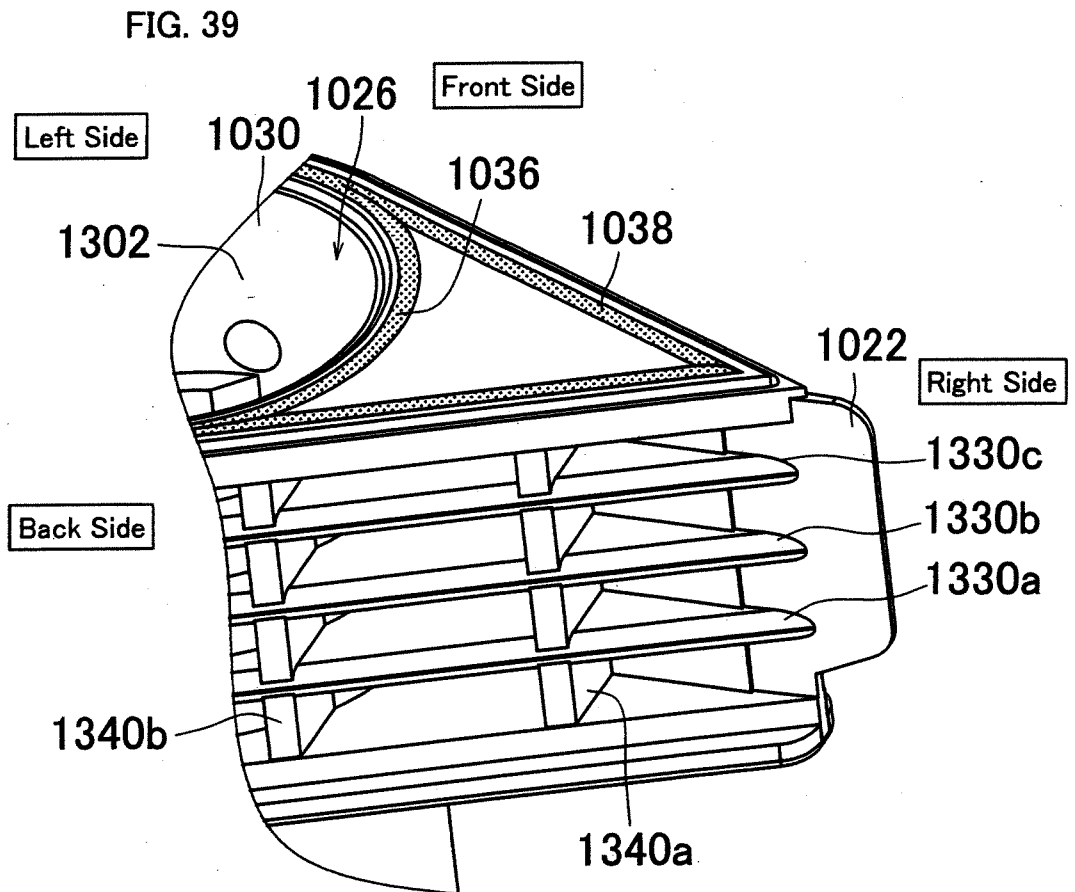
[illegible]

【FIG. 38B】

FIG. 38B

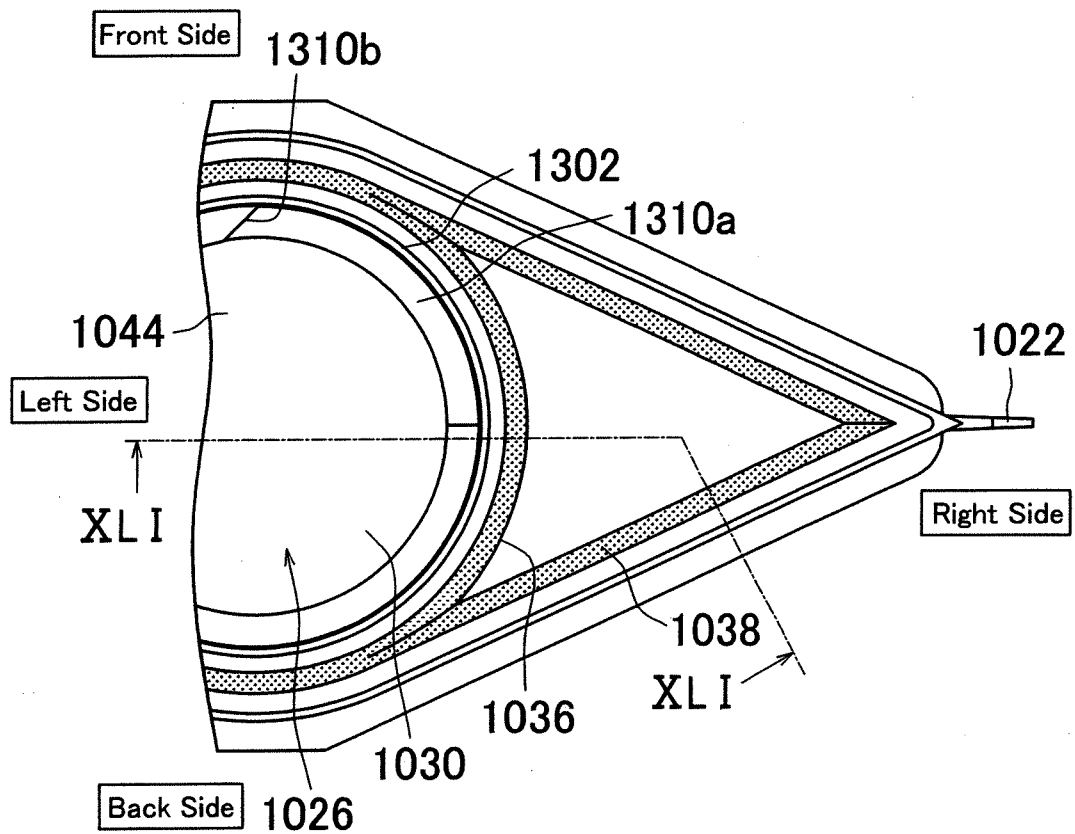


【FIG. 39】



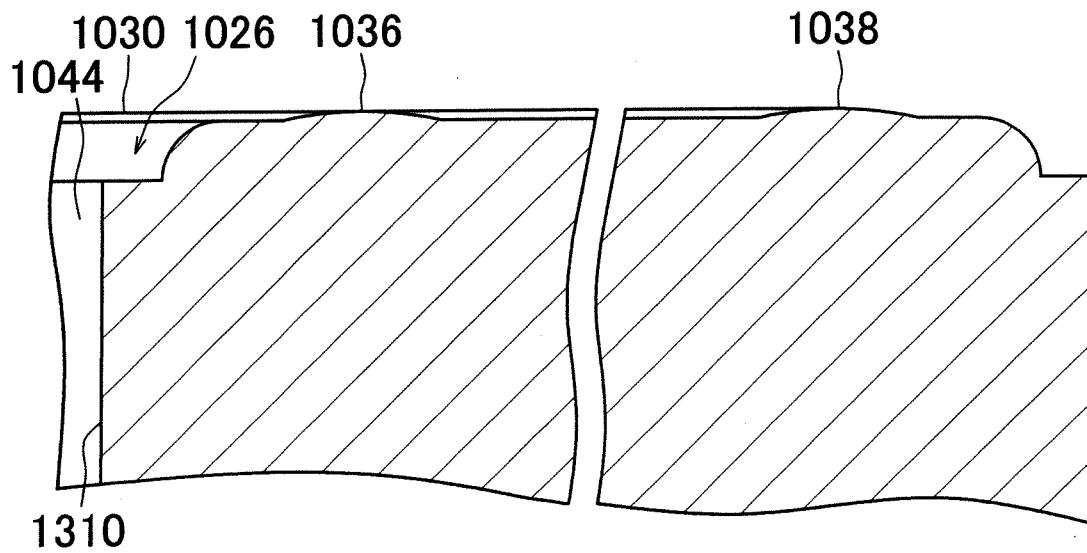
【FIG. 40】

FIG. 40



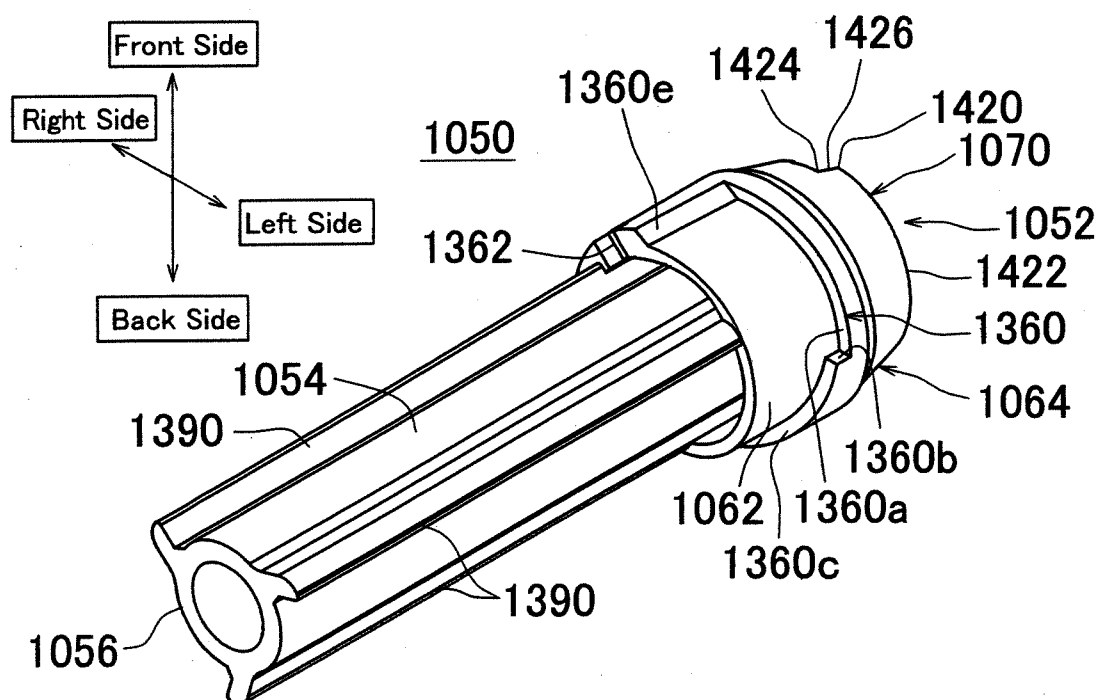
【FIG. 41】

FIG. 41



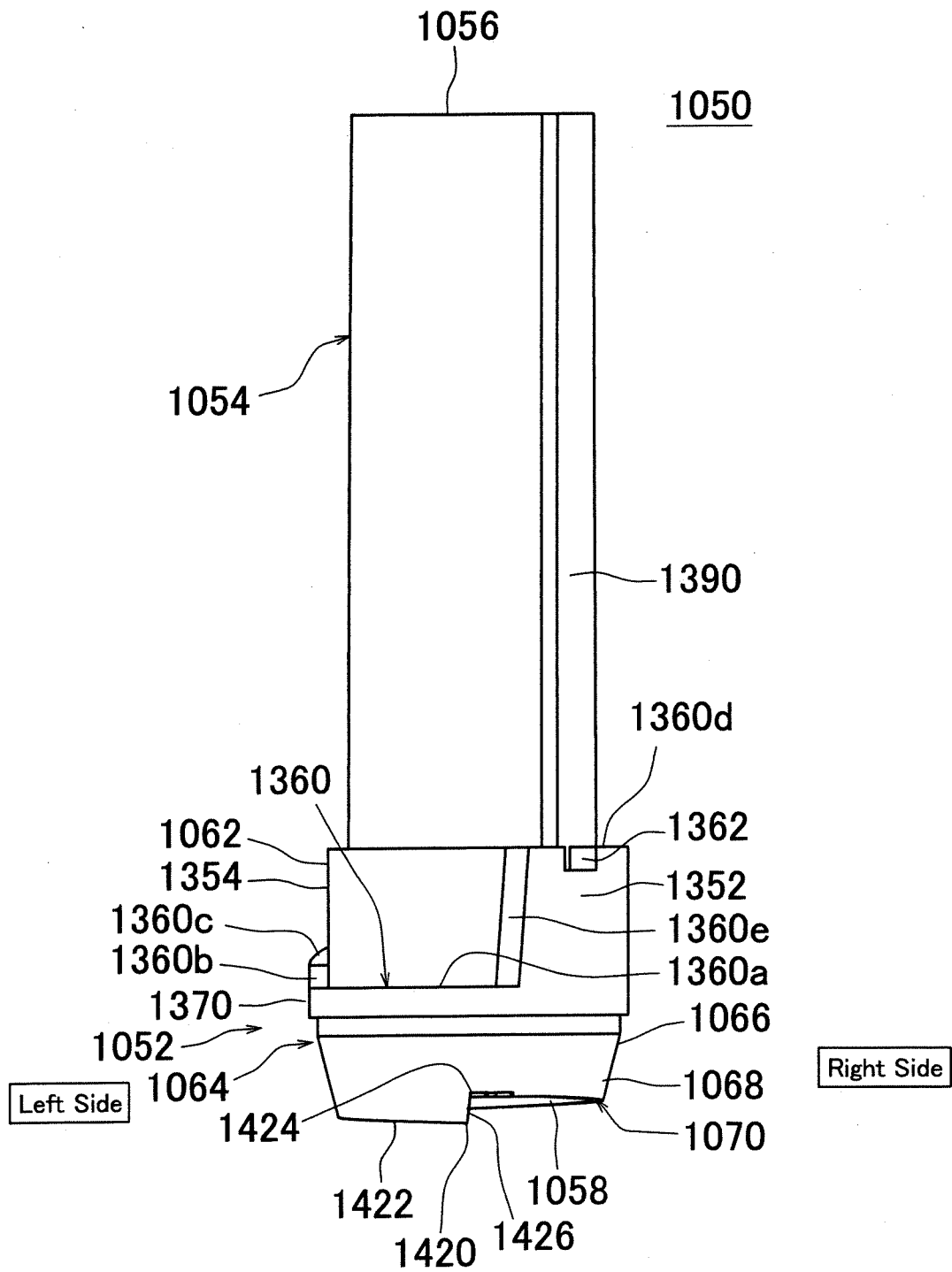
[illegible]

FIG. 43



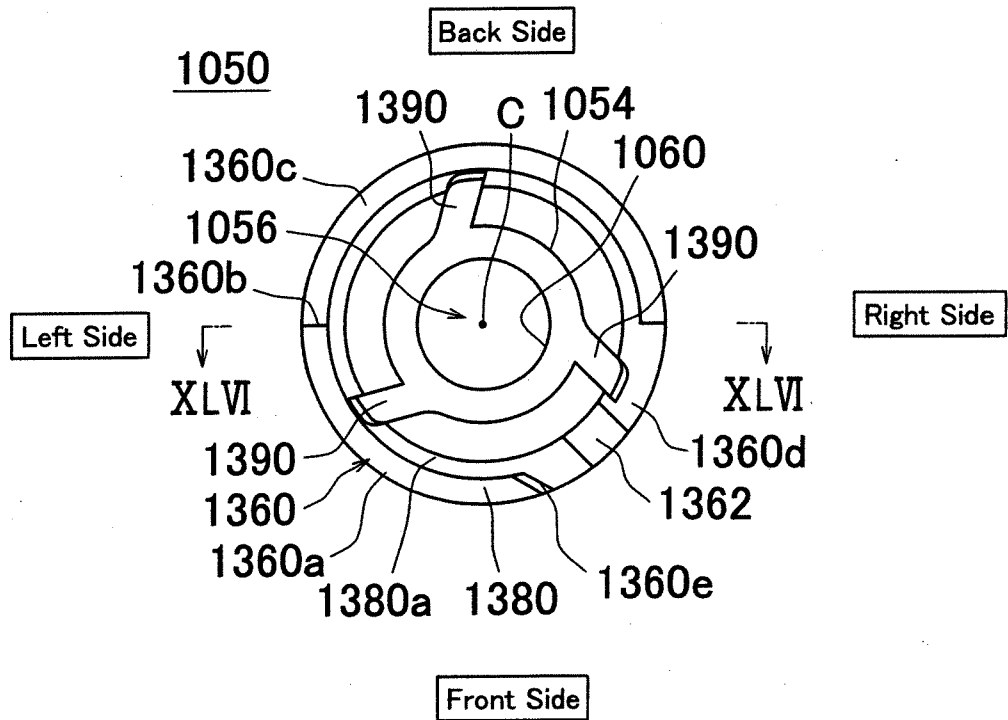
【FIG. 44】

FIG. 44



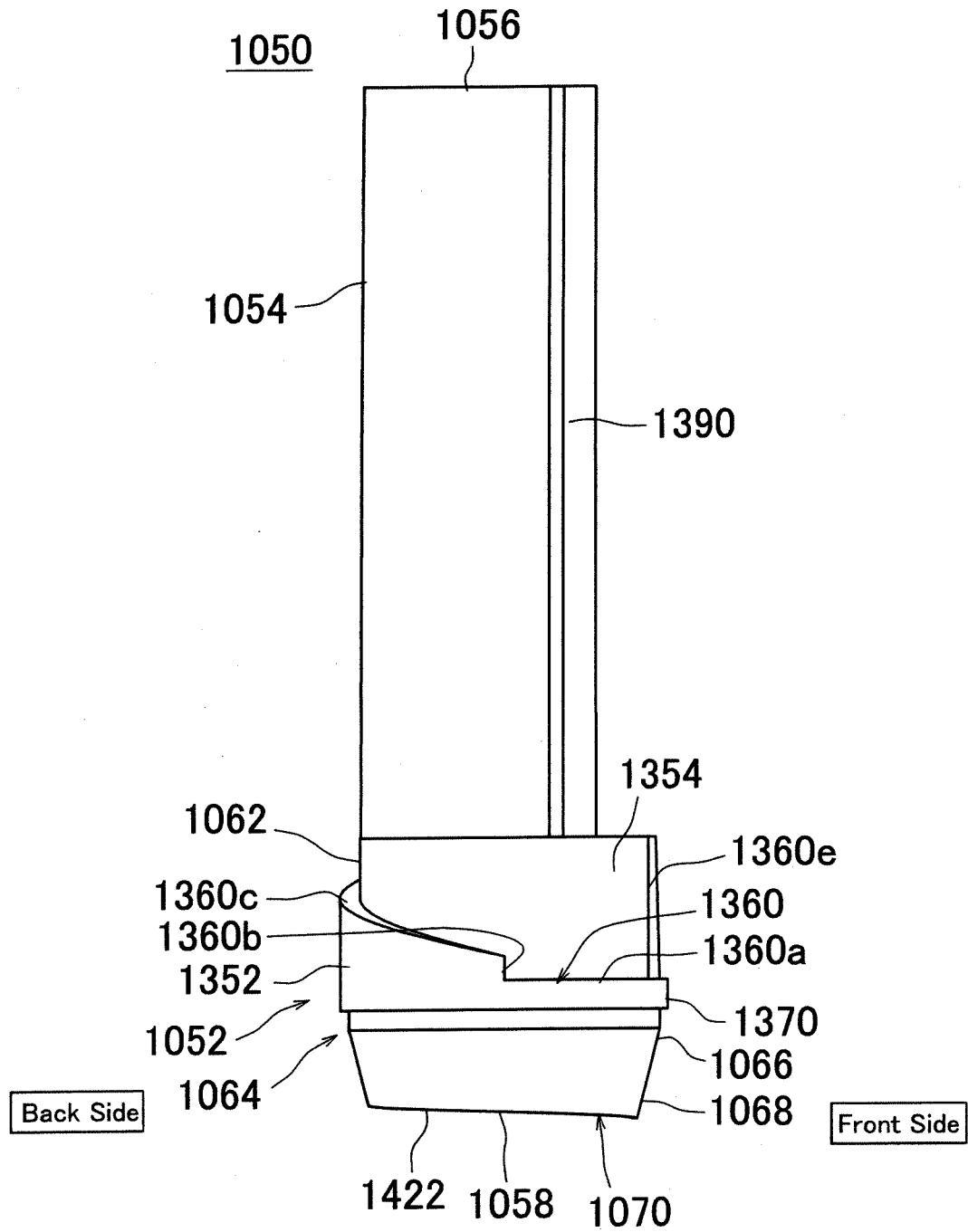
【FIG. 45A】

FIG. 45A



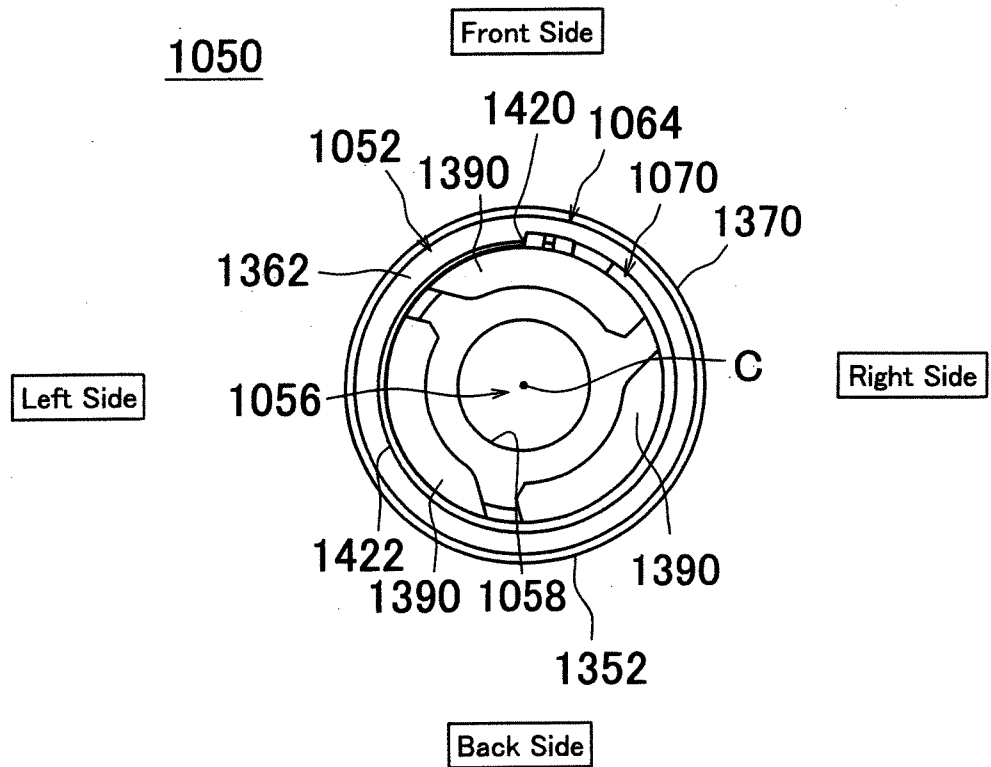
【FIG. 45B】

FIG. 45B



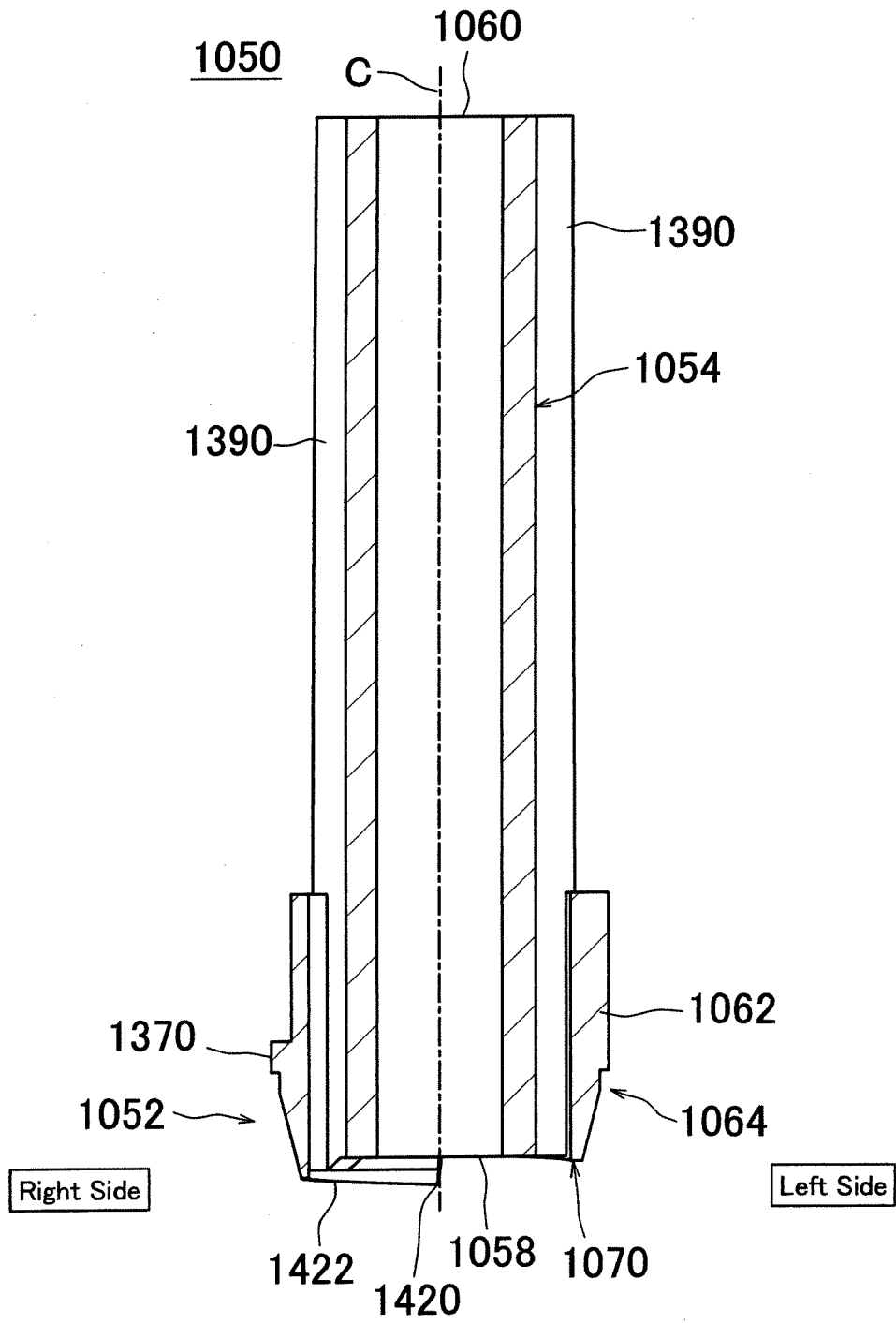
【FIG. 45C】

FIG. 45C



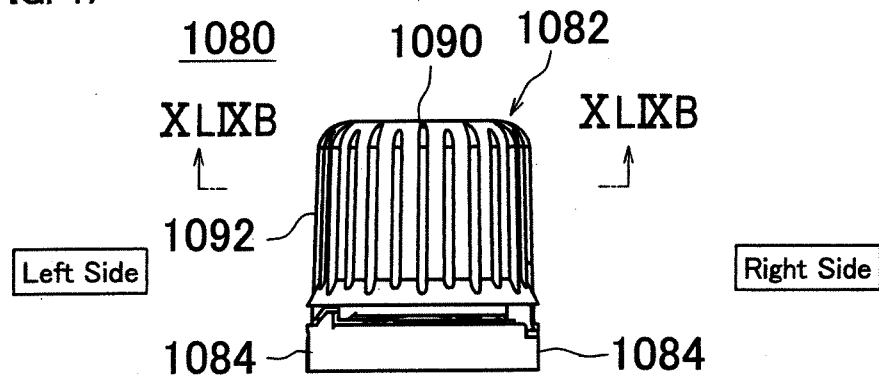
【FIG. 46】

FIG. 46



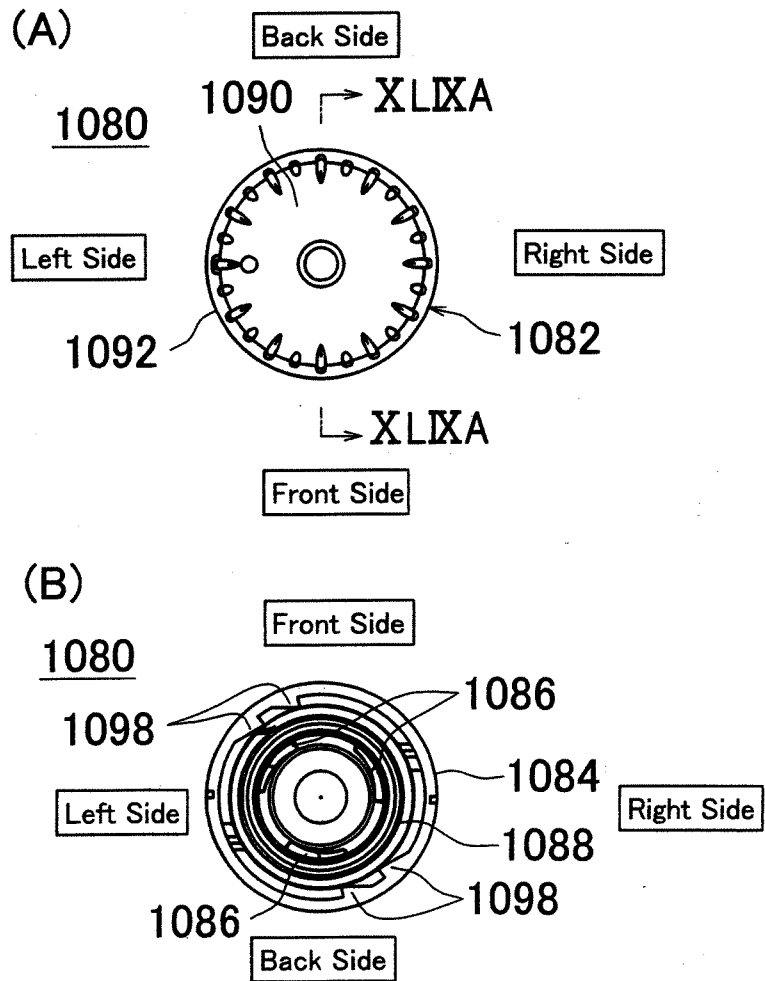
【FIG. 47】

FIG. 47



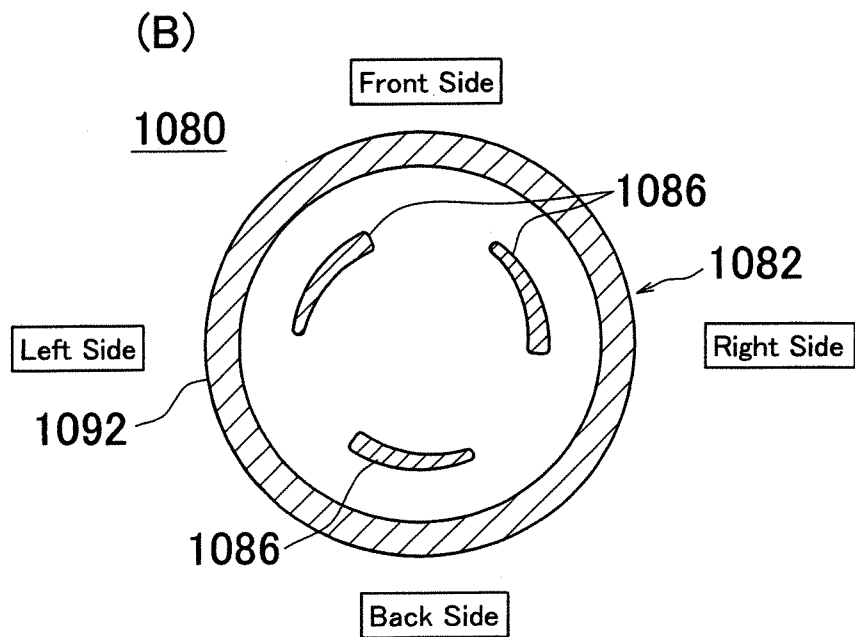
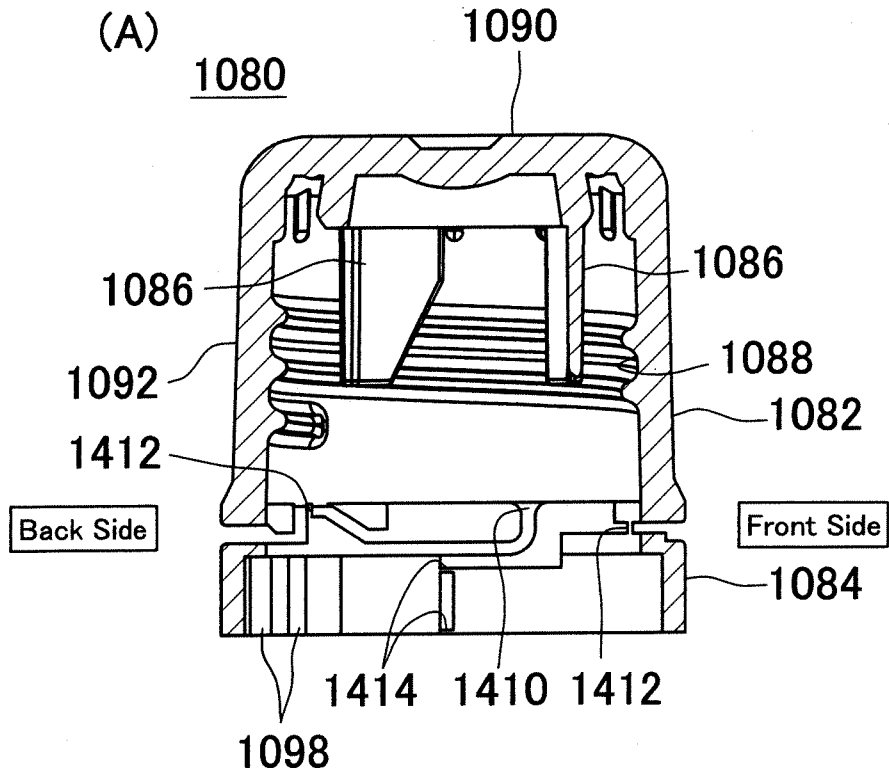
【FIG. 48】

FIG. 48



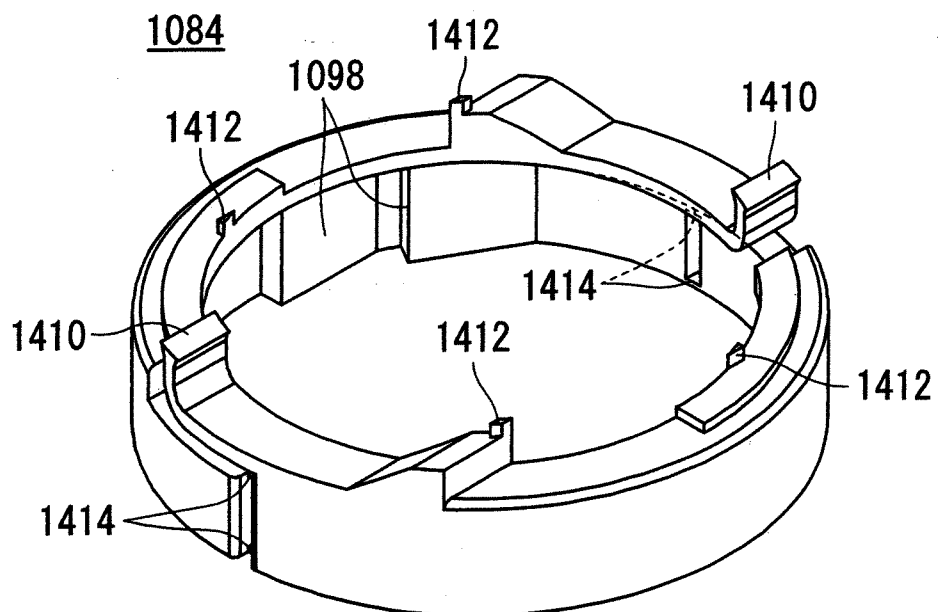
【FIG. 49】

FIG. 49



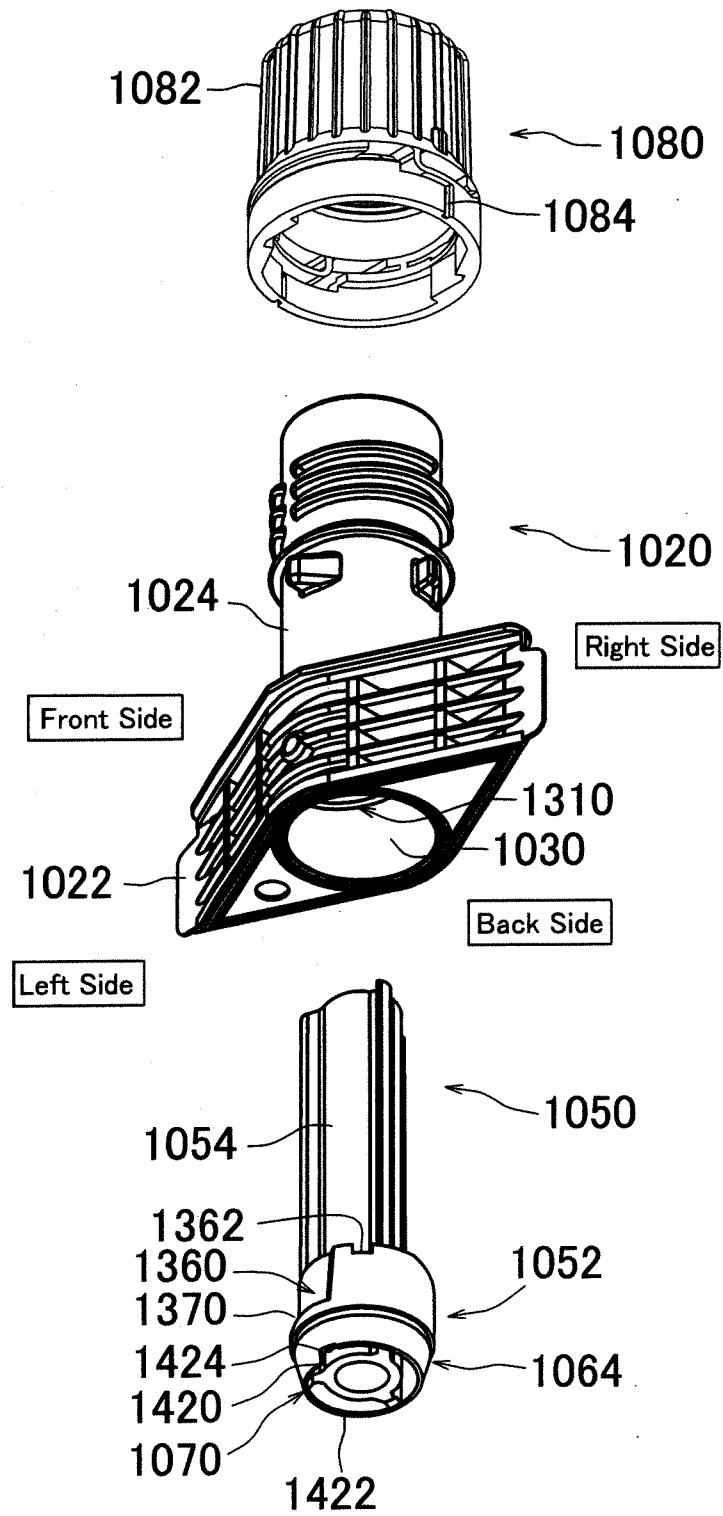
【FIG. 50】

FIG. 50



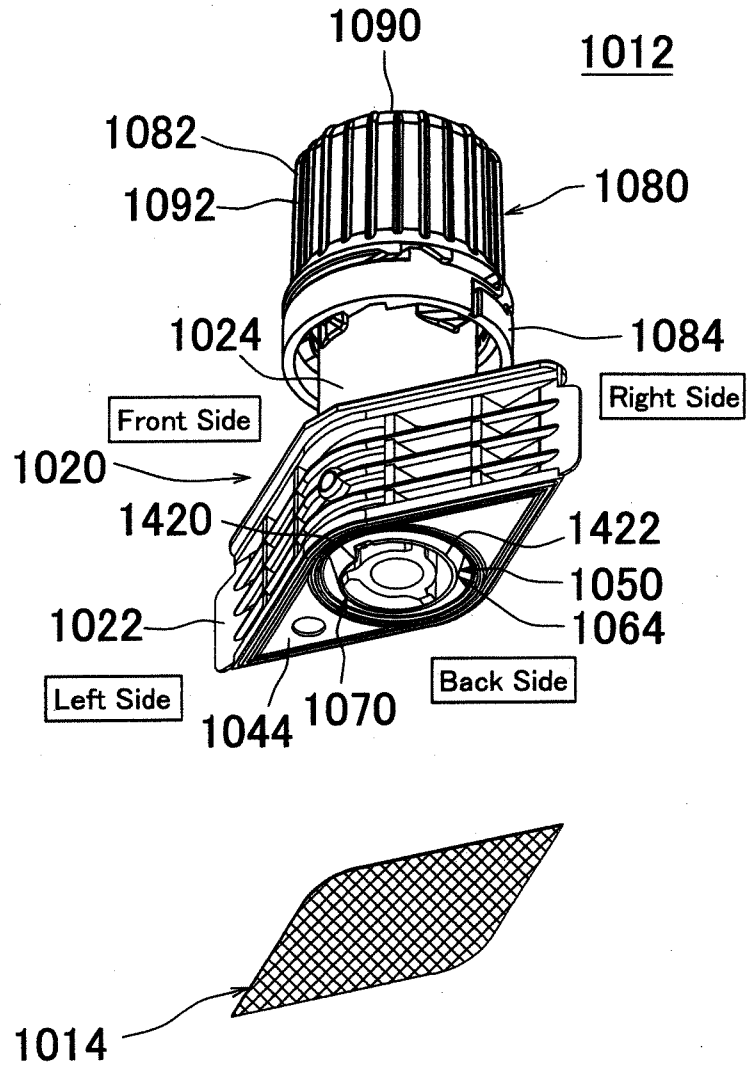
【FIG. 51】

FIG. 51



【FIG. 52】

FIG. 52

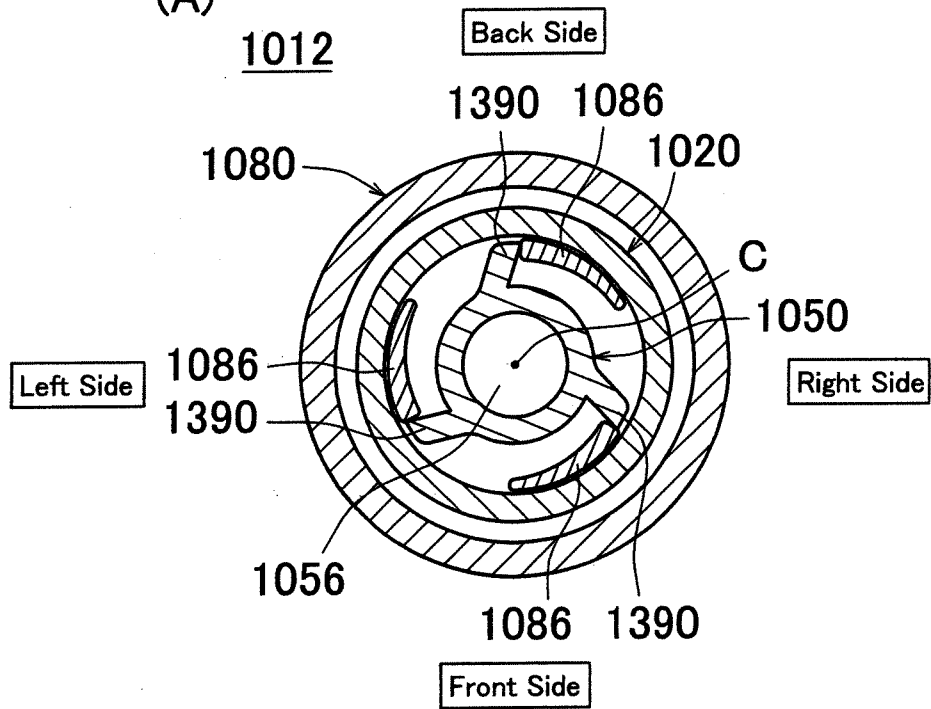


This cross-sectional view, taken along line C-C, illustrates the internal structure of the semiconductor device. A central core (1028) is surrounded by a series of layers including 1090, 1060, 1056, and 1086. The core is flanked by two main vertical sections, 1082 and 1088, which are part of a larger assembly 1080. The bottom of the device features a base layer 1014, with various internal structures like 1030, 1420, 1058, and 1070. The top of the device is capped with a layer 1012. The right side of the device is labeled 'Right Side' and the left side 'Left Side', both with 'LVI' (Lead Vertical Interconnect) indicators. Other labels include 1020, 1022, 1024, 1032, 1040, 1042, 1044, 1050, 1052, 1054, 1064, 1084, 1092, 1310, 1360, 1370, 1422, and 1500.

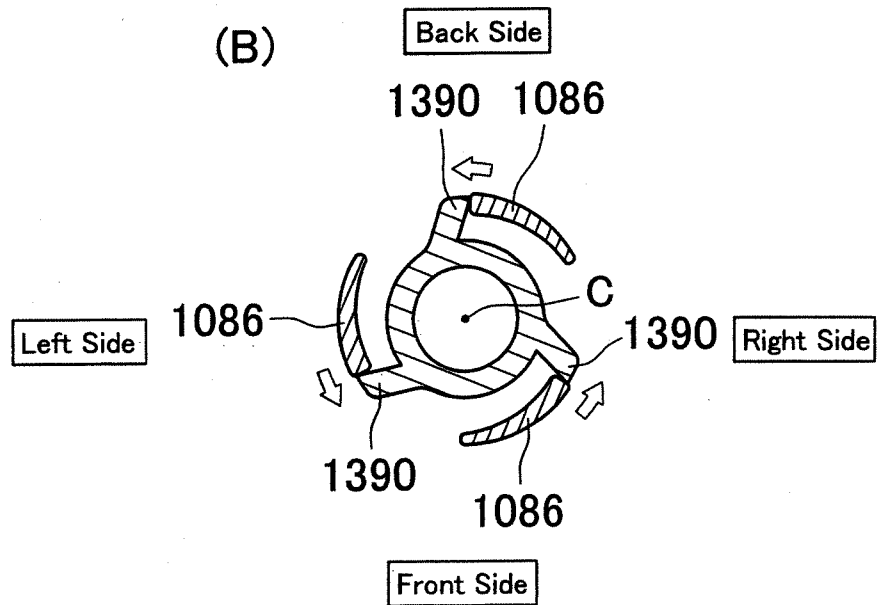
【FIG. 54】

FIG. 54

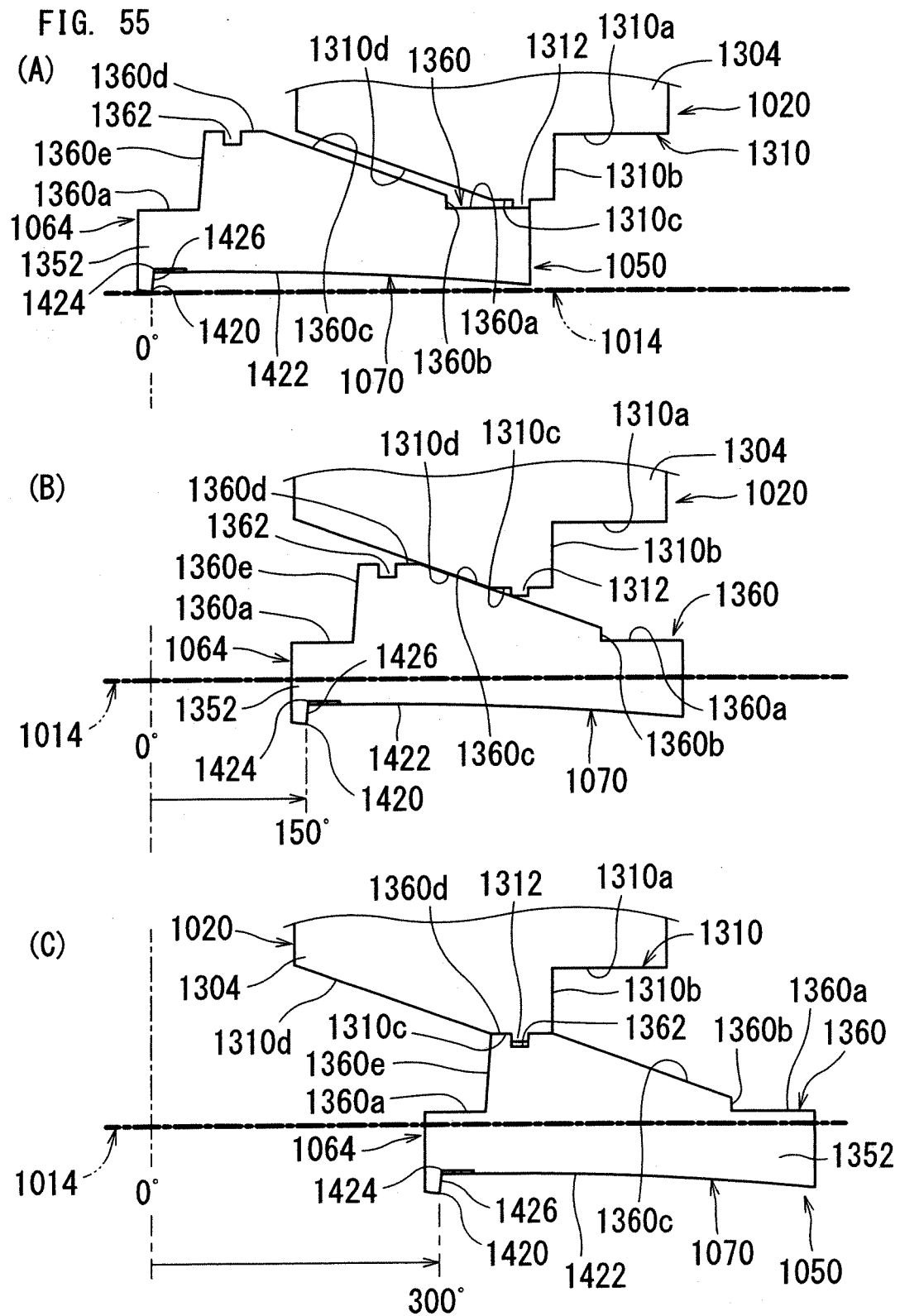
(A)



(B)

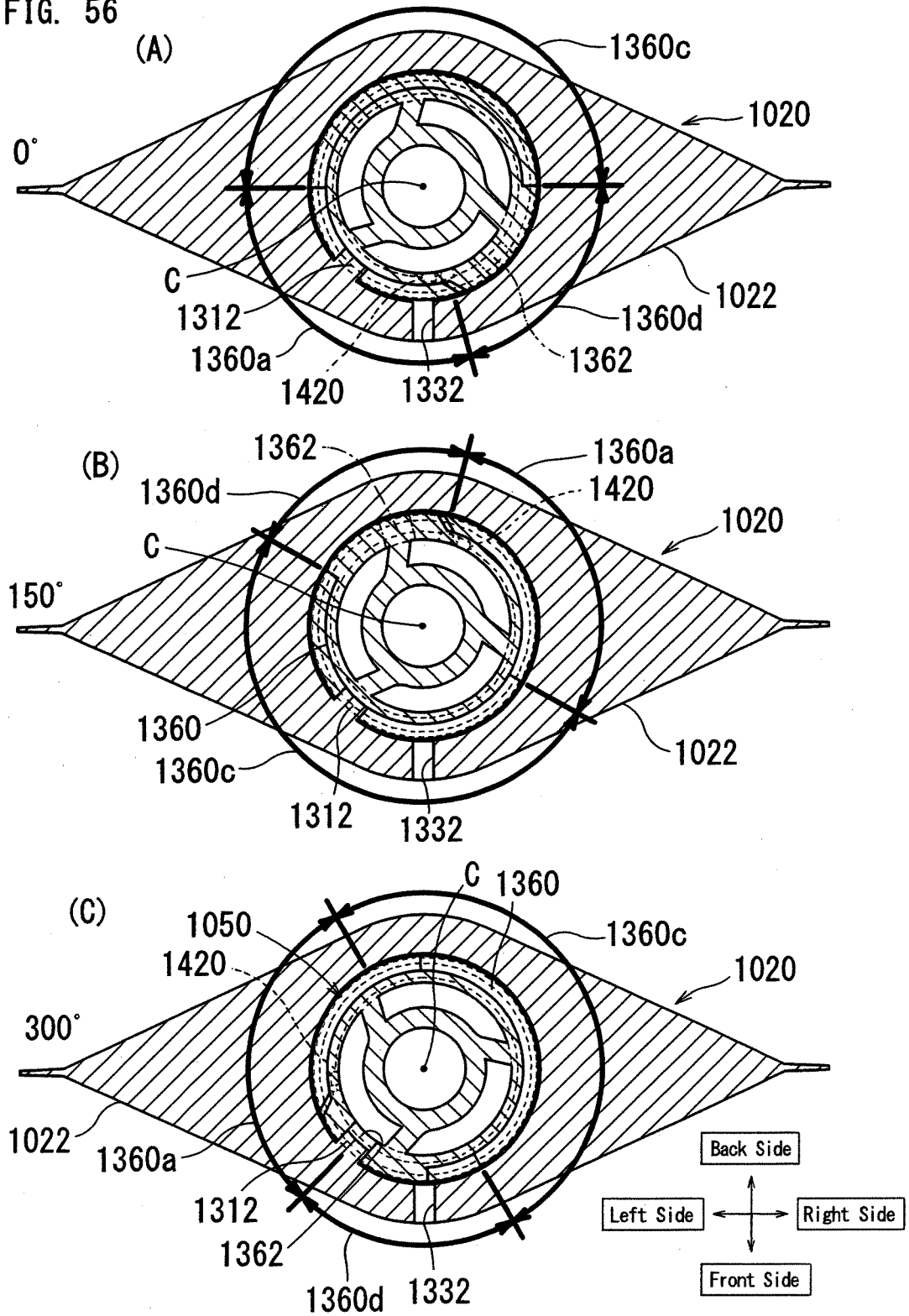


【FIG. 55】



【FIG. 56】

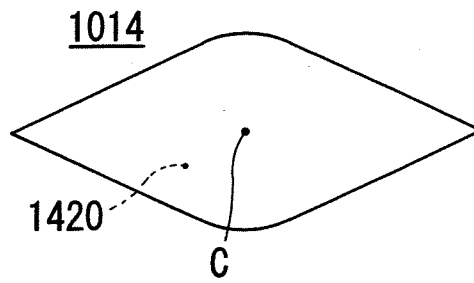
FIG. 56



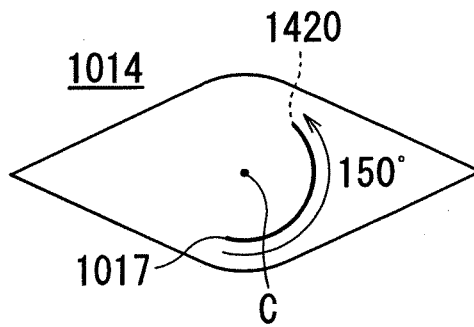
【FIG. 57】

FIG. 57

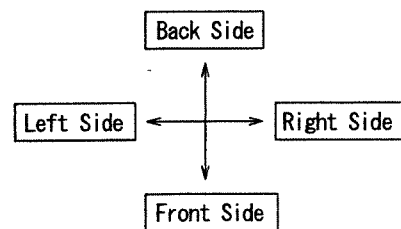
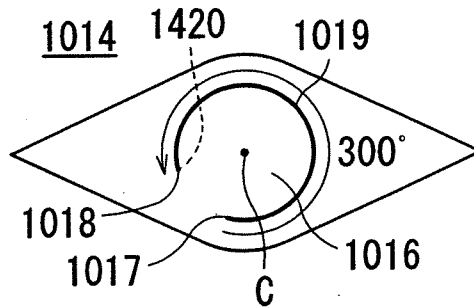
(A)



(B)

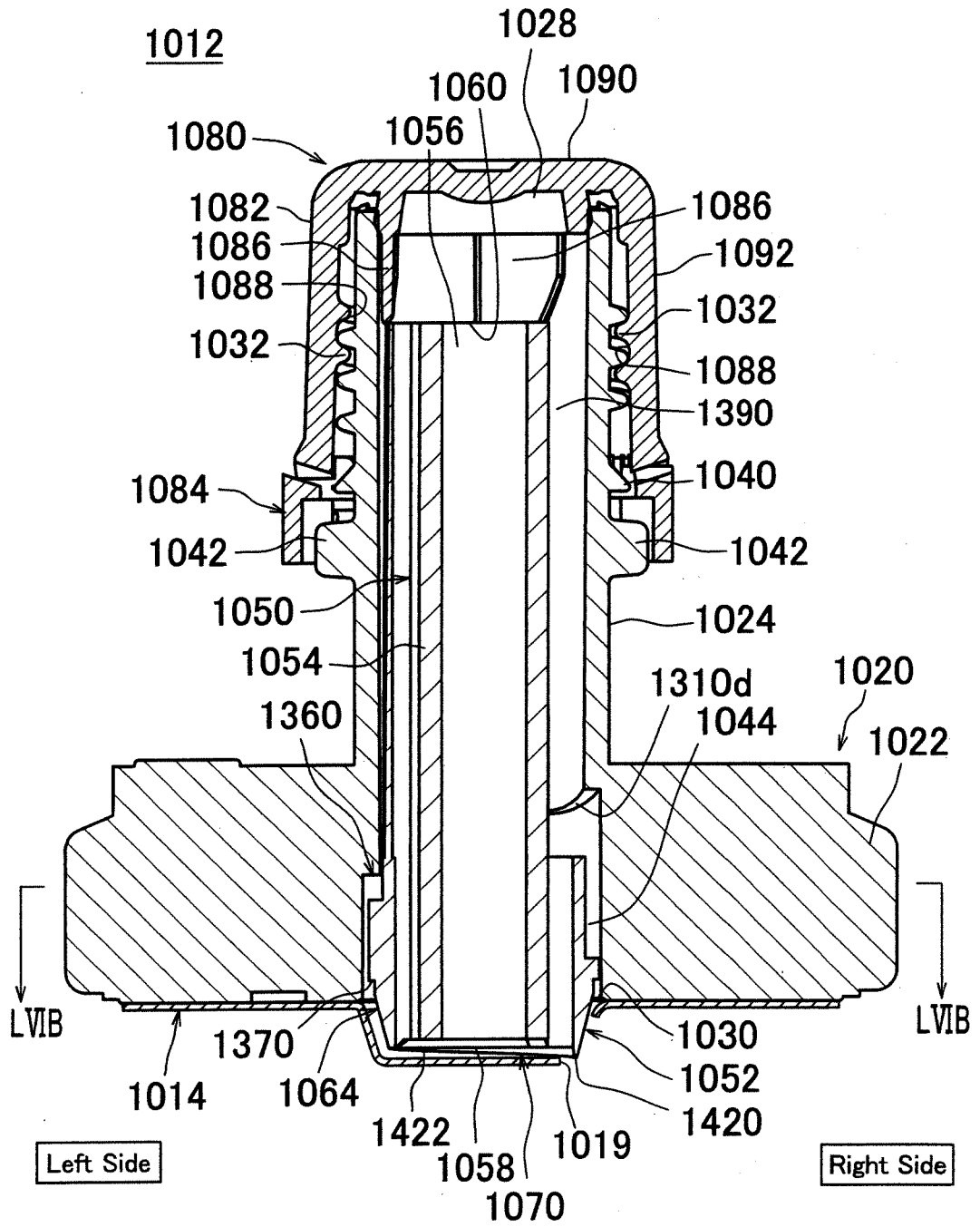


(C)



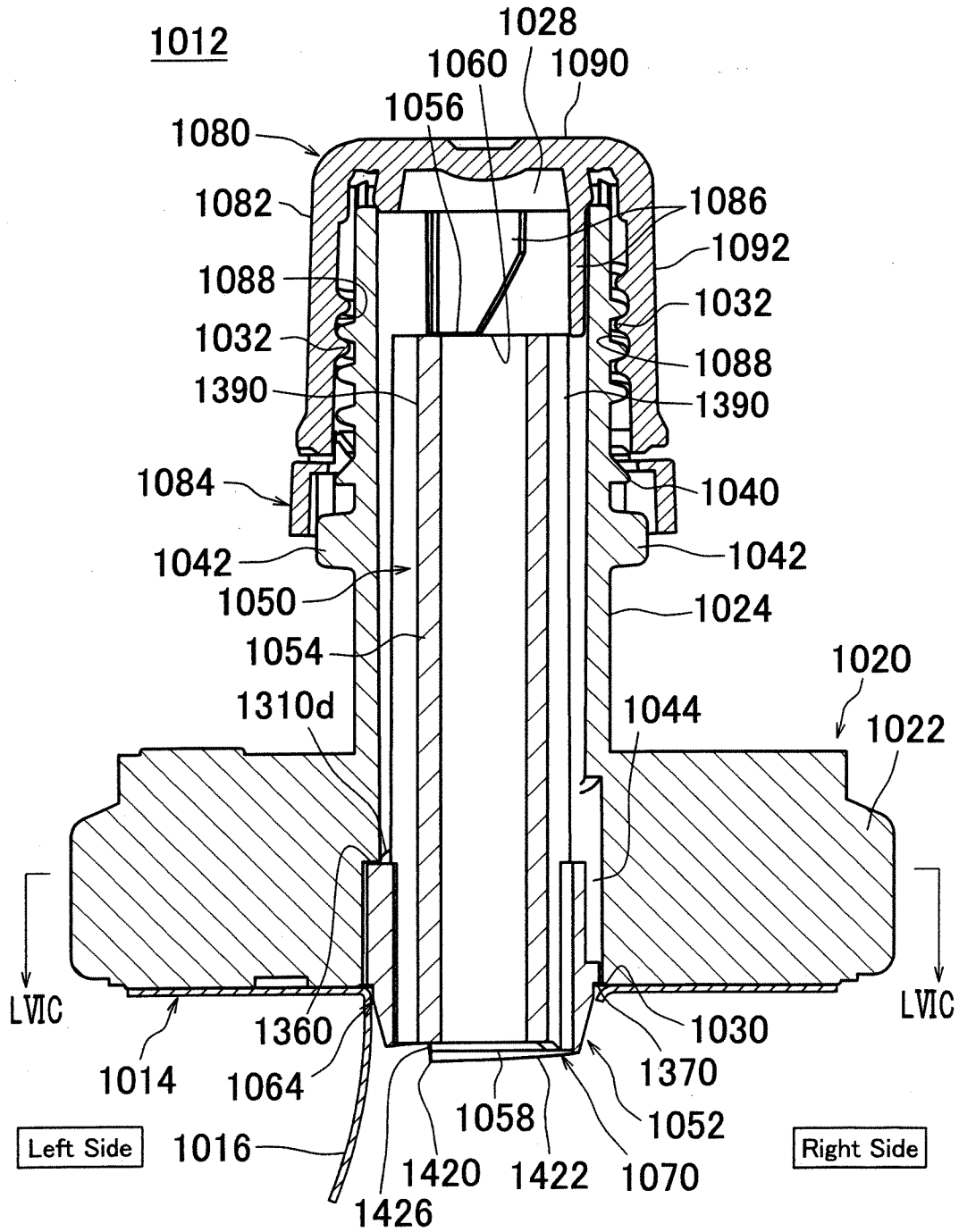
【FIG. 58】

FIG. 58



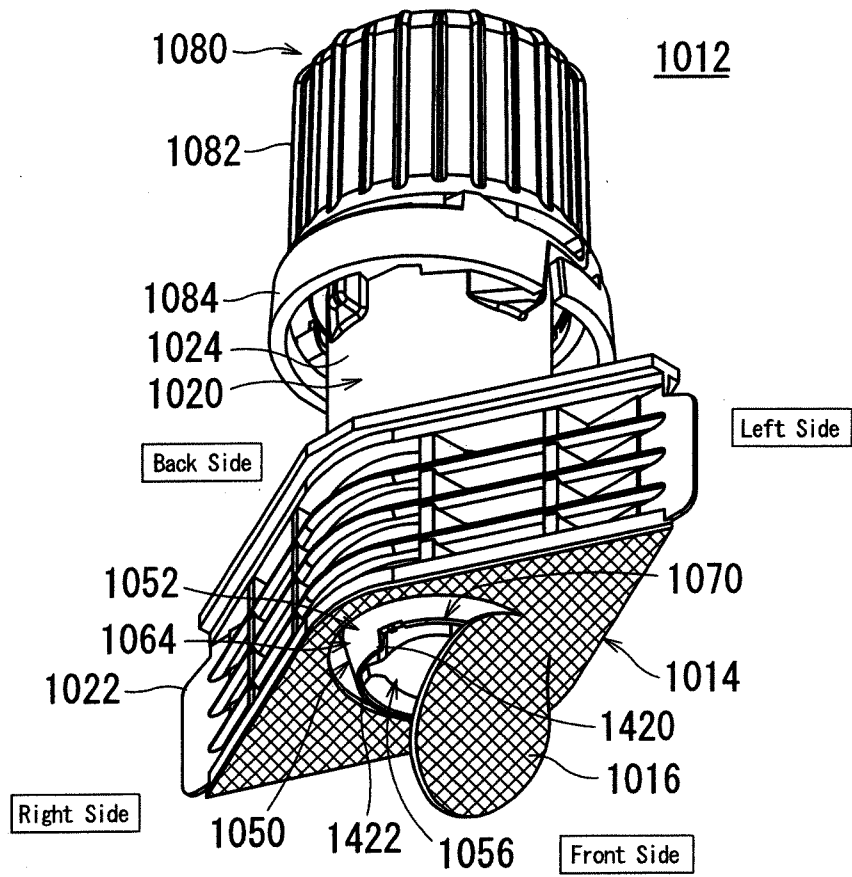
【FIG. 59】

FIG. 59



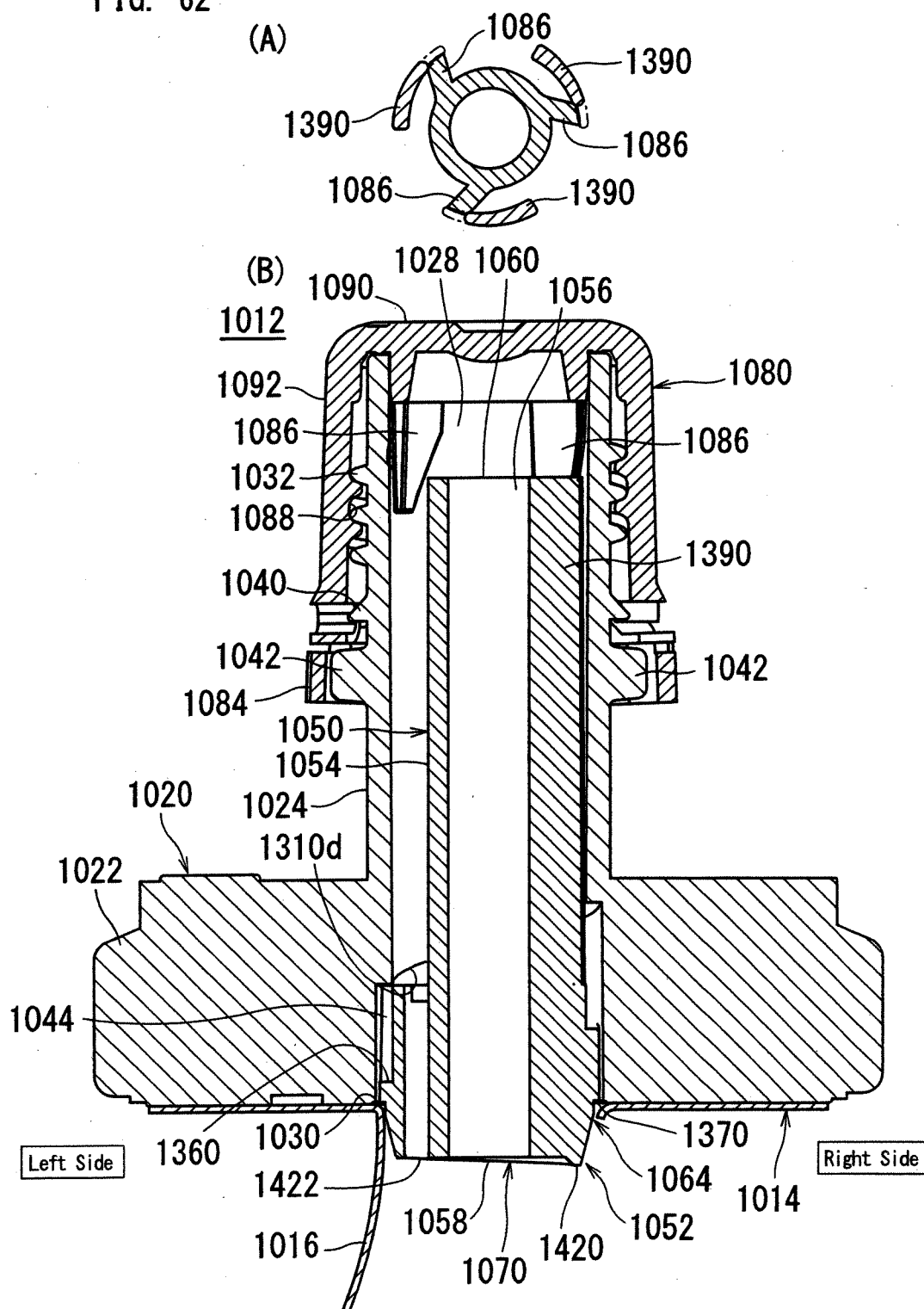
【FIG. 61】

FIG. 61



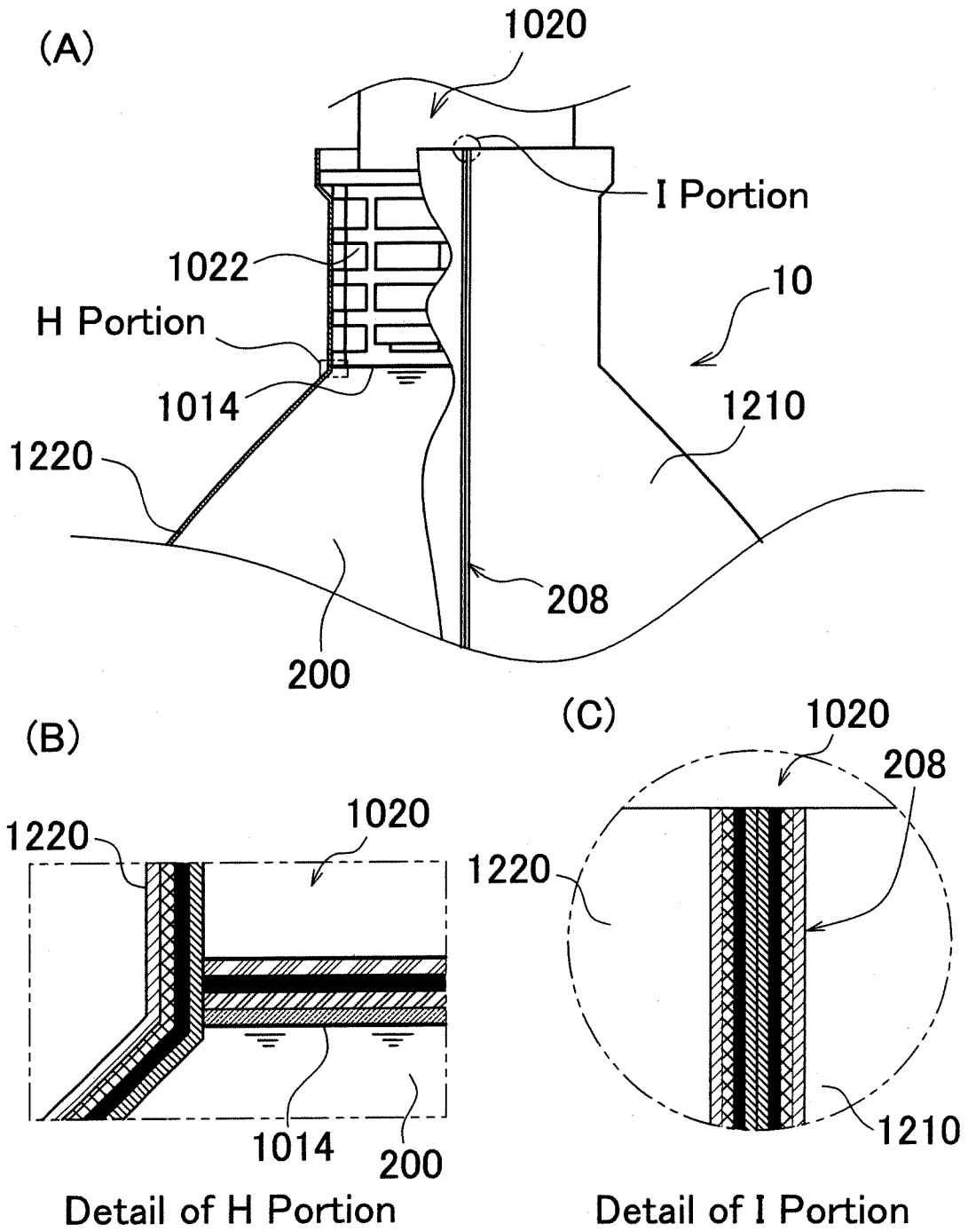
【FIG. 62】

FIG. 62



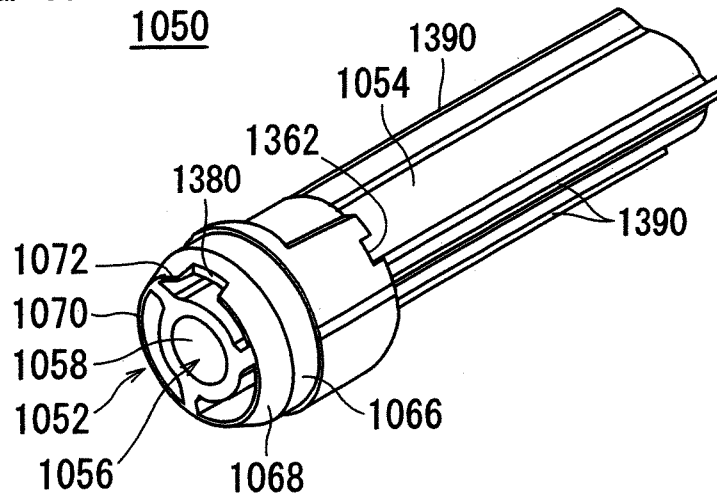
【FIG. 63】

FIG. 63



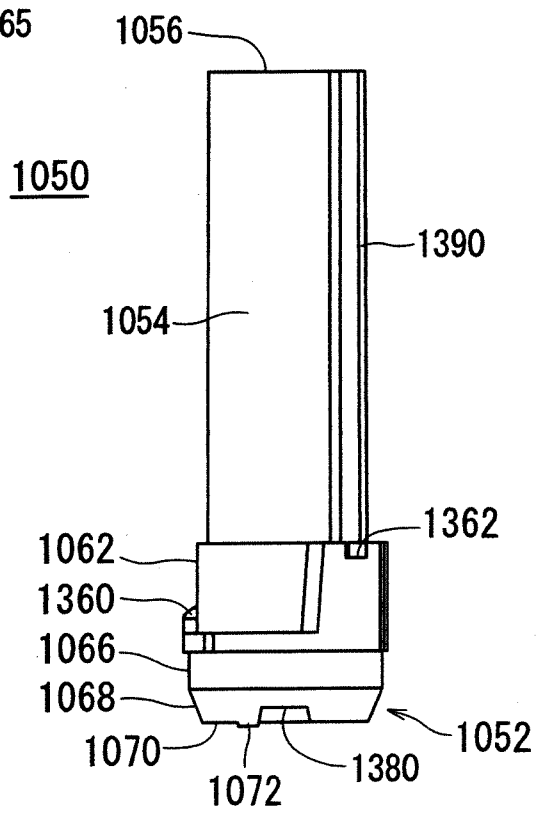
【FIG. 64】

FIG. 64



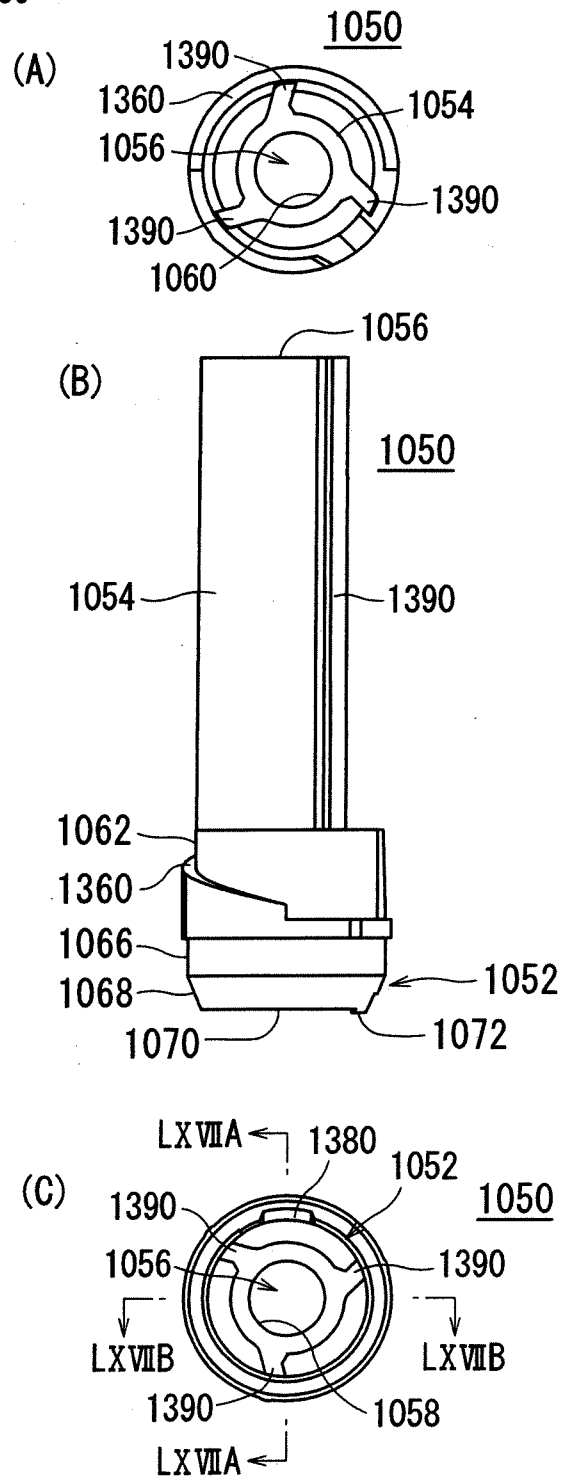
【FIG. 65】

FIG. 65



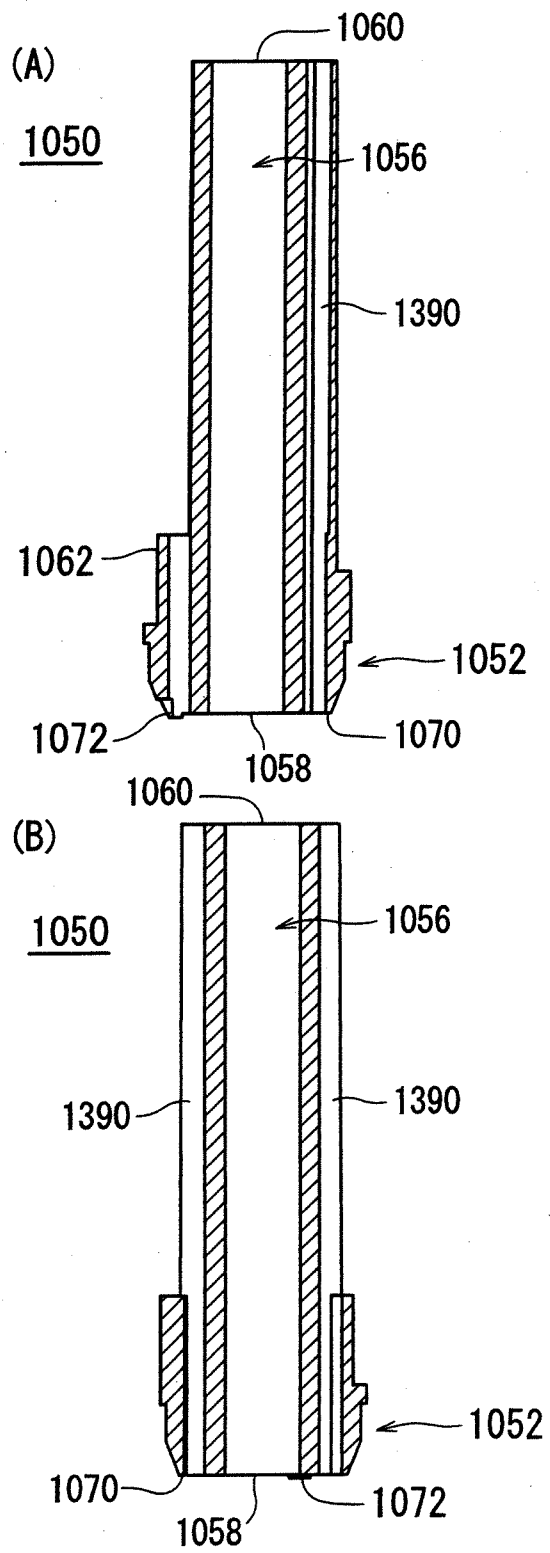
【FIG. 66】

FIG. 66



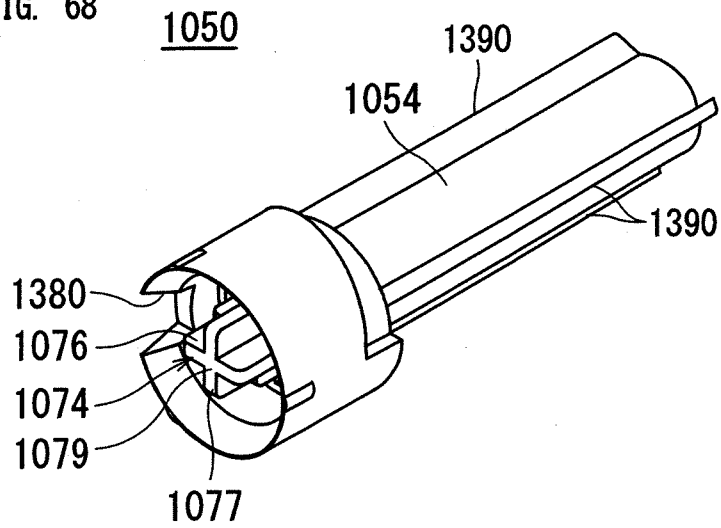
【FIG. 67】

FIG. 67



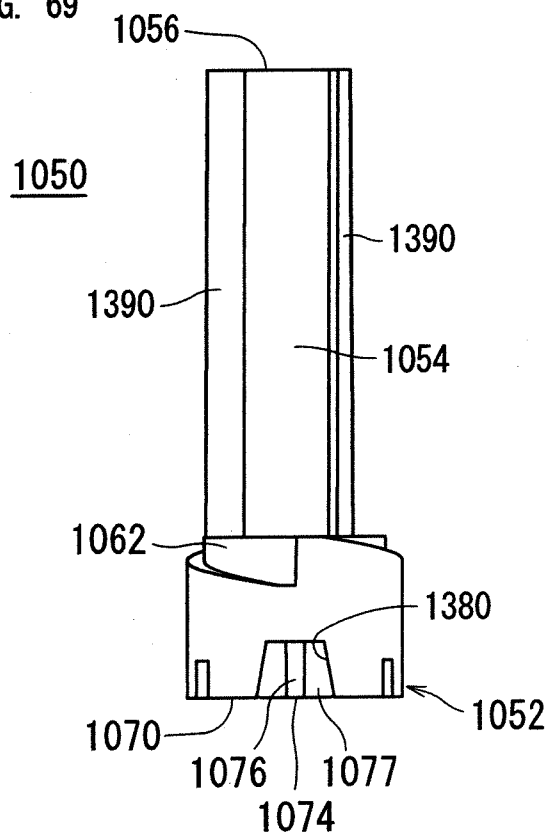
【FIG. 68】

FIG. 68



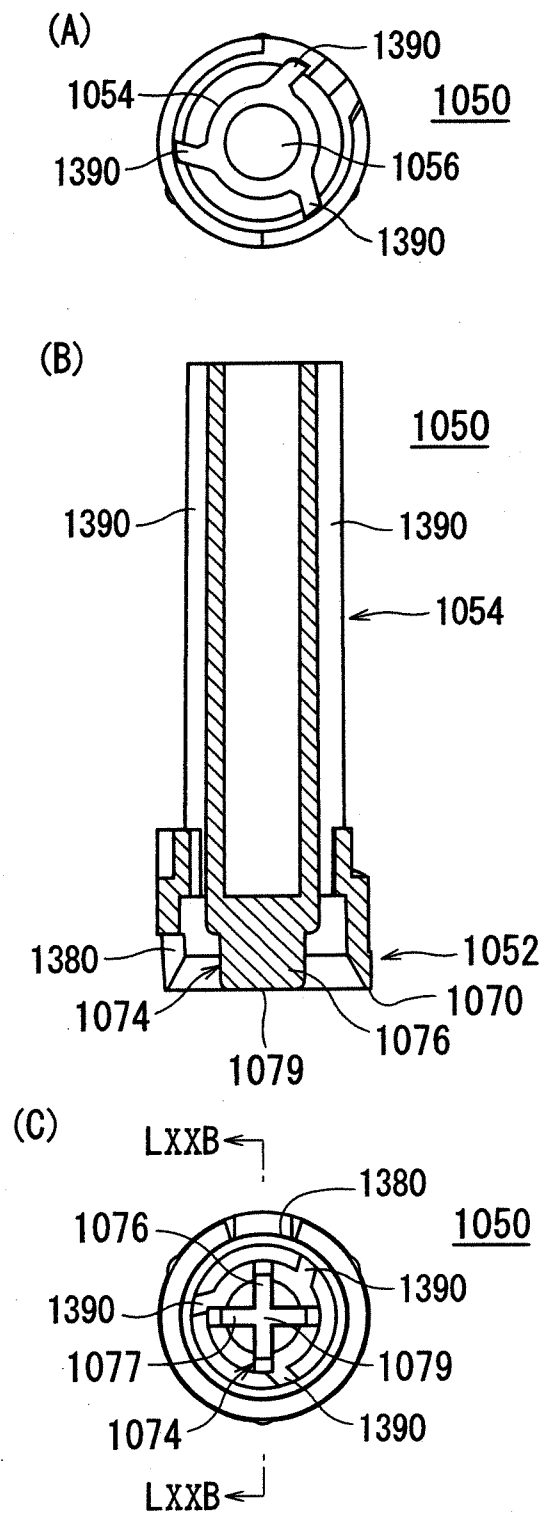
【FIG. 69】

FIG. 69



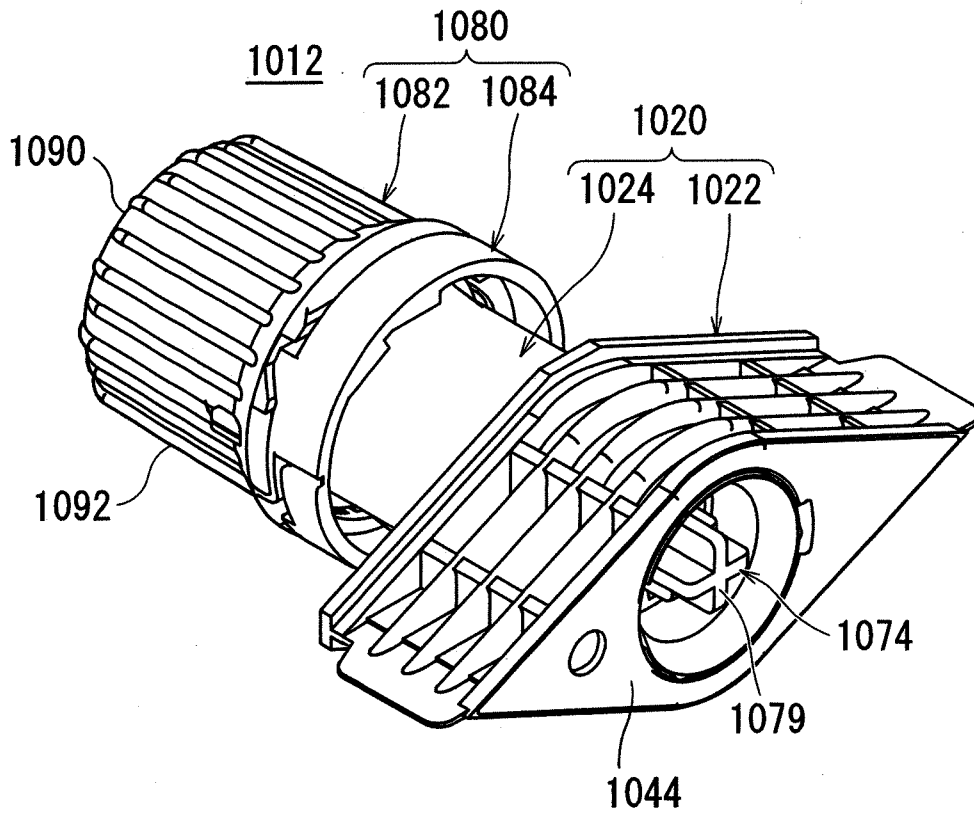
【FIG. 70】

FIG. 70



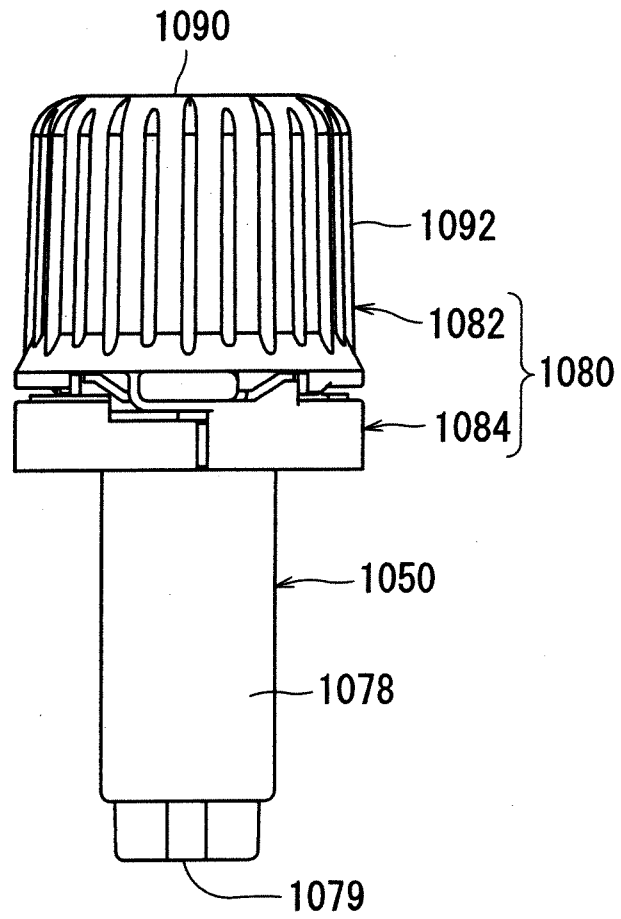
【FIG. 71】

FIG. 71



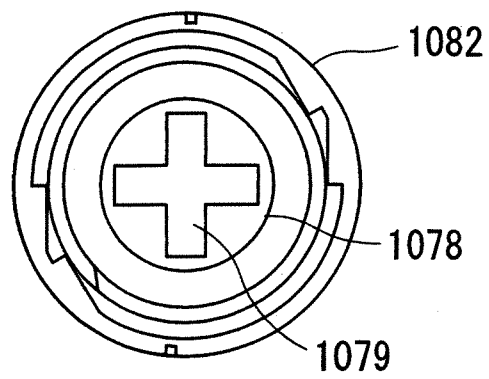
【FIG. 72】

FIG. 72



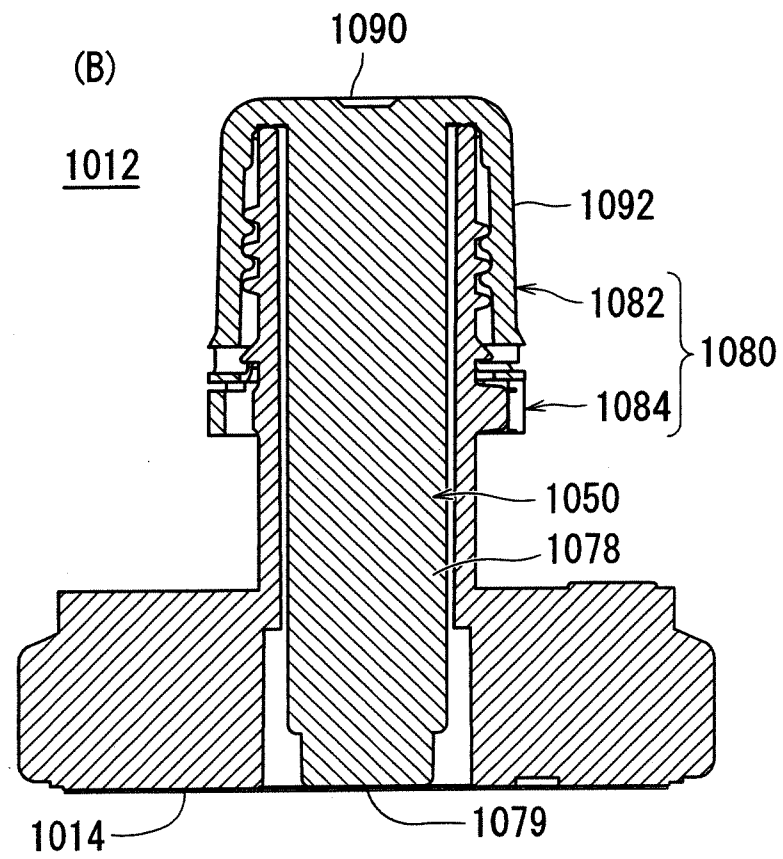
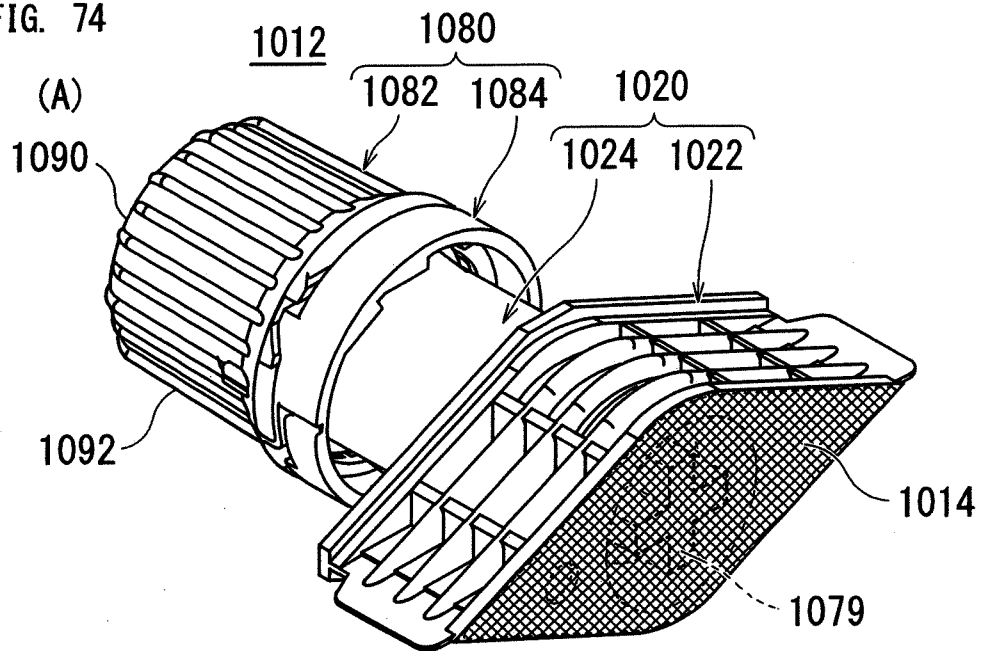
【FIG. 73】

FIG. 73

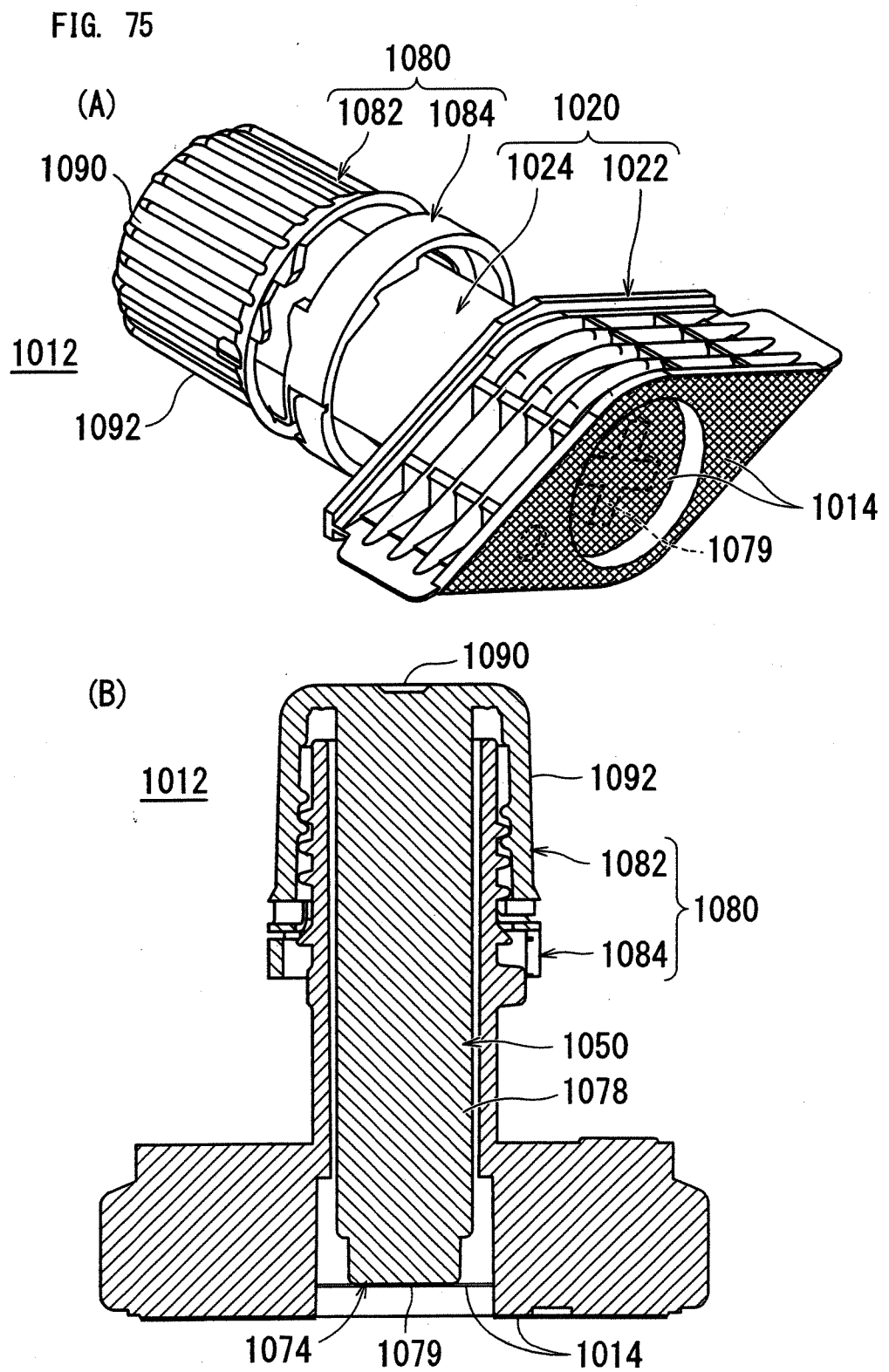


【FIG. 74】

FIG. 74

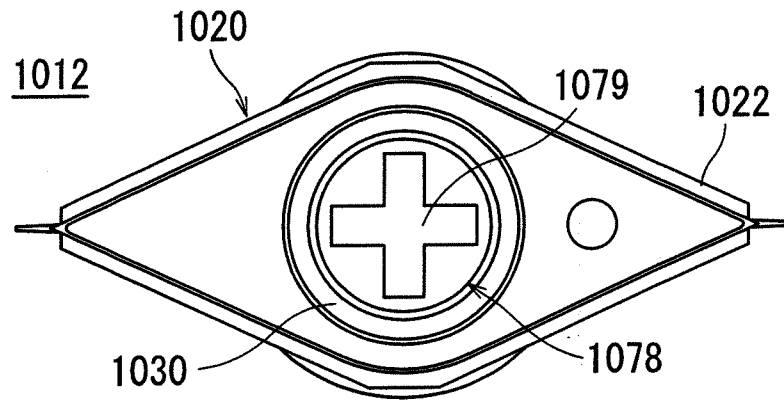


【FIG. 75】



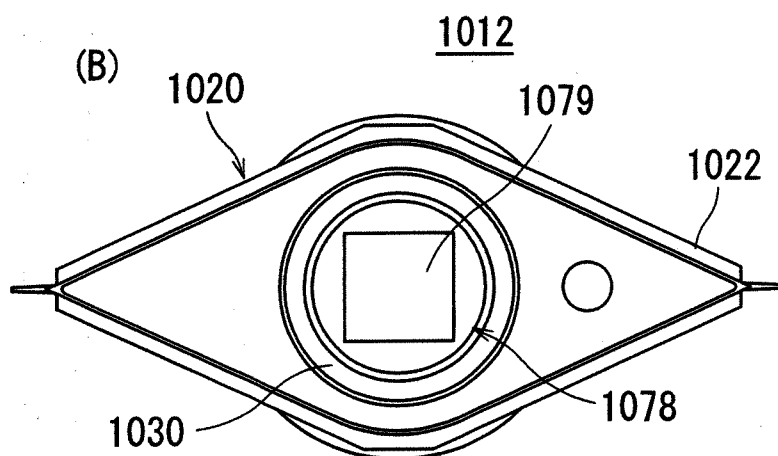
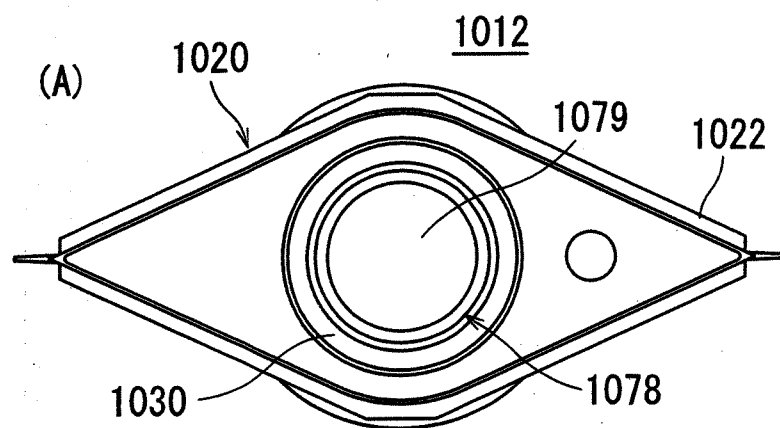
【FIG. 76】

FIG. 76



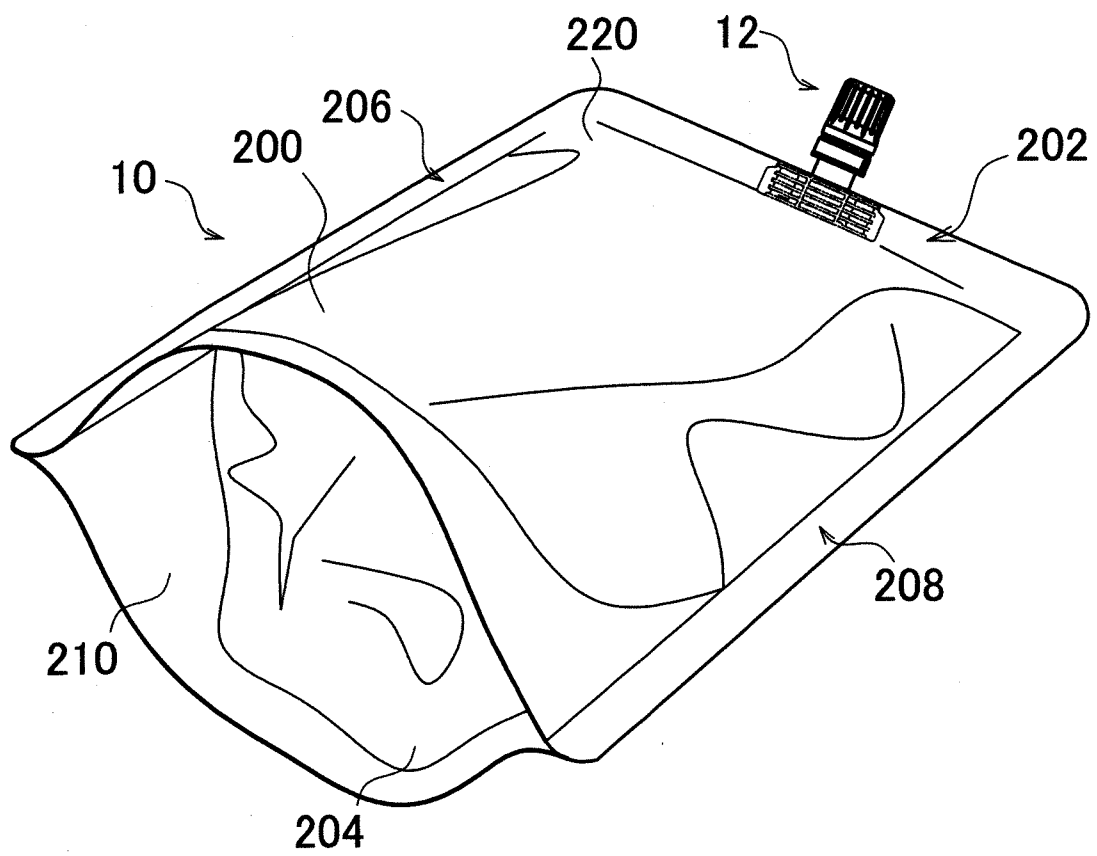
【FIG. 77】

FIG. 77



【FIG. 78】

FIG. 78



【FIG. 79】

FIG. 79

