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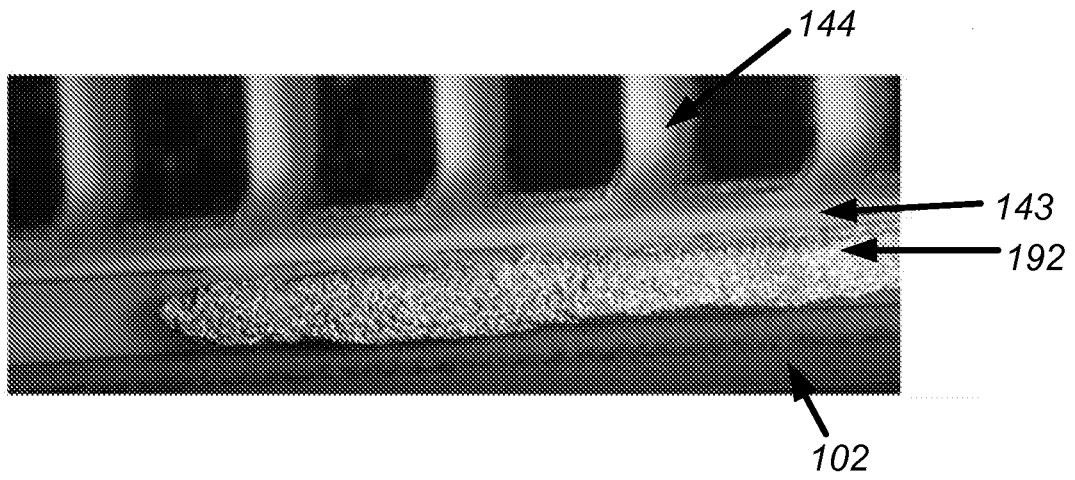


FIG. 1A-1

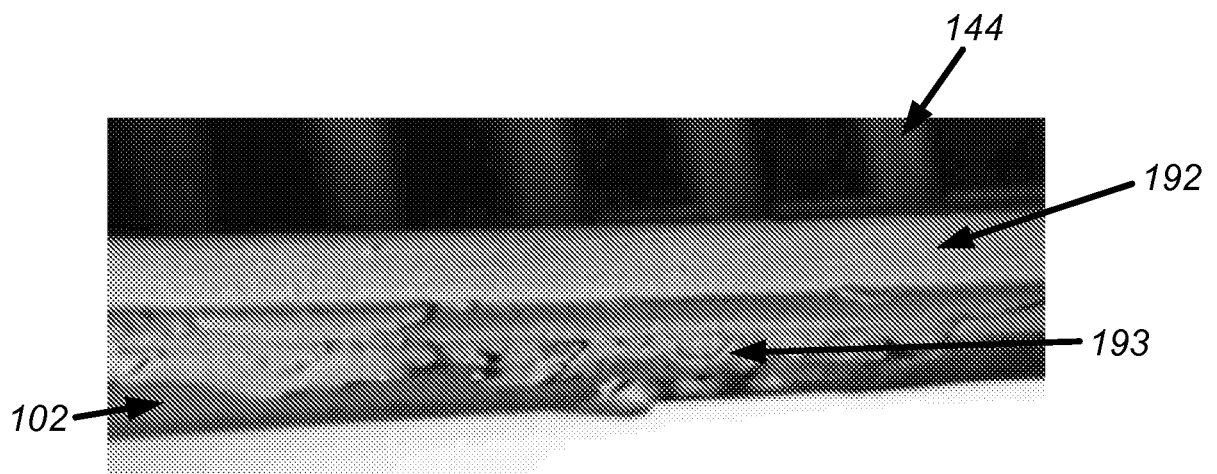


FIG. 1A-2

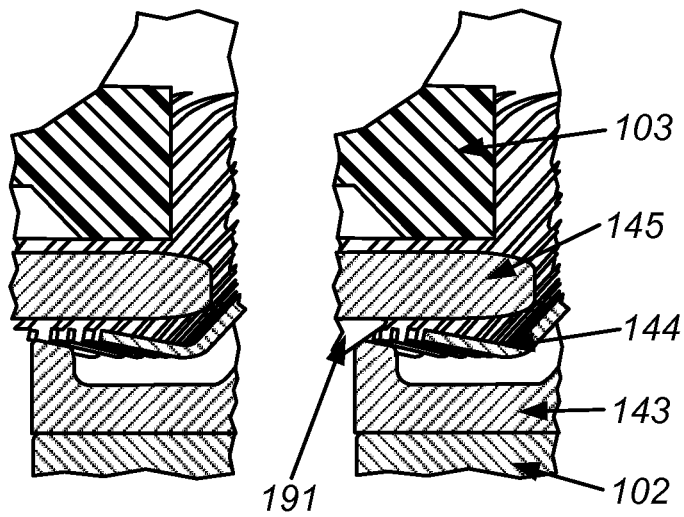


FIG. 1B-1

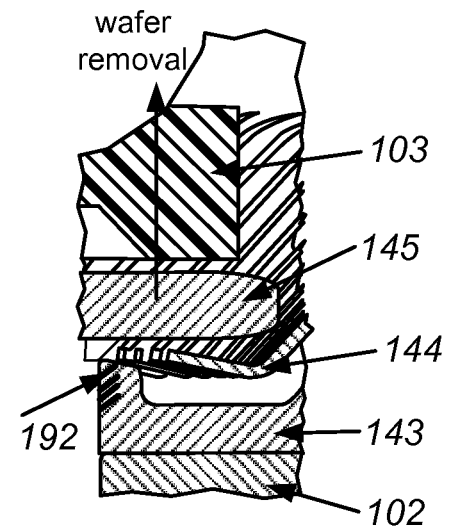


FIG. 1B-2

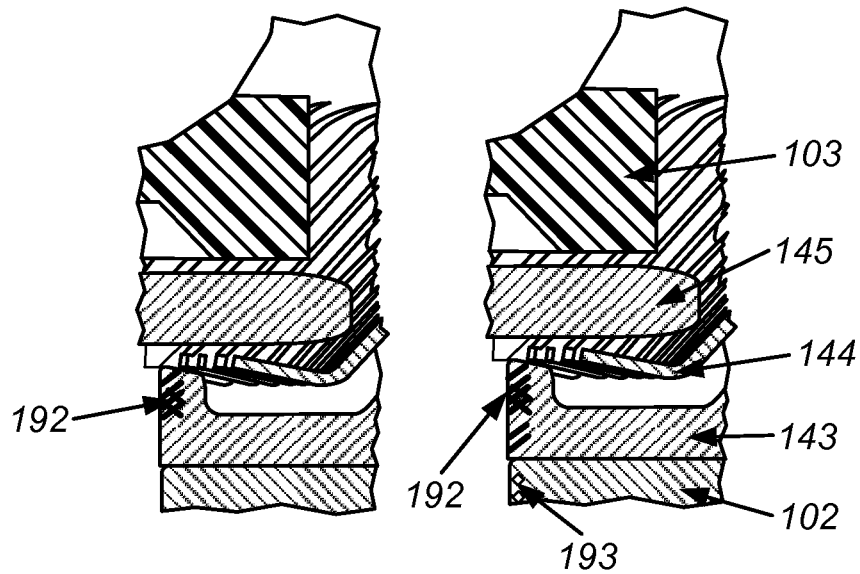
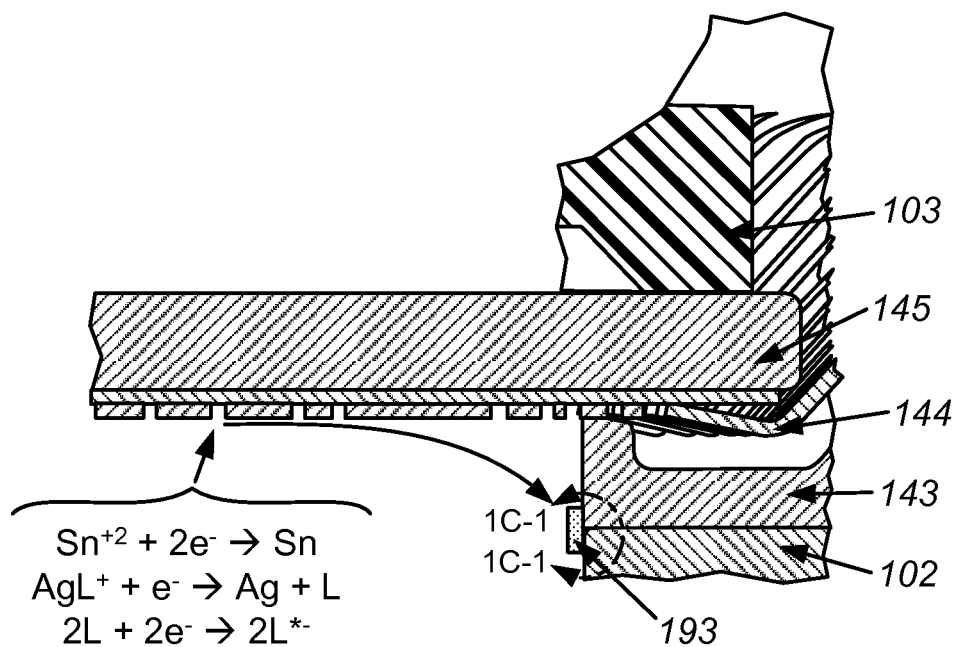
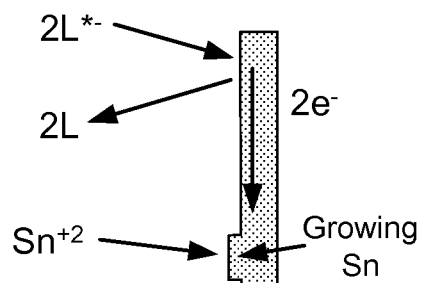


FIG. 1B-3

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**FIG. 1C****FIG. 1C-1**

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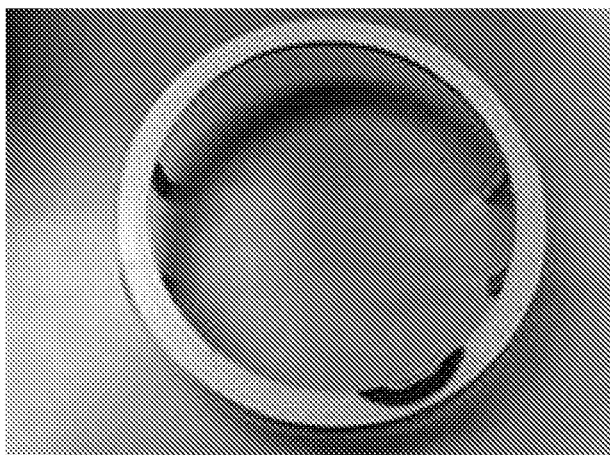


FIG. 1D-1

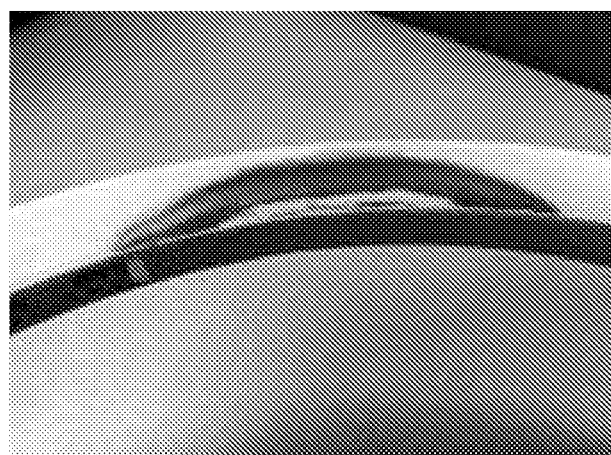


FIG. 1D-2

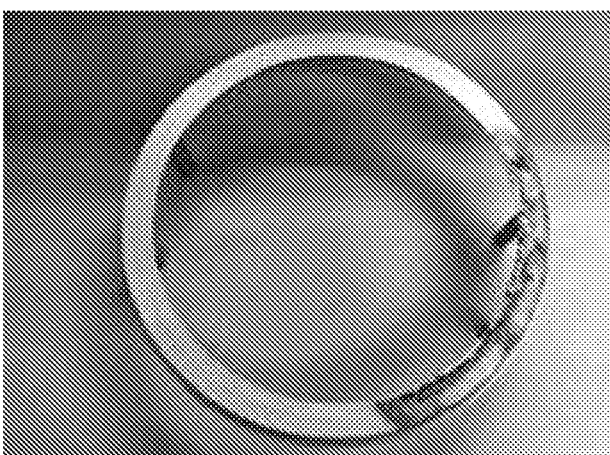


FIG. 1D-3

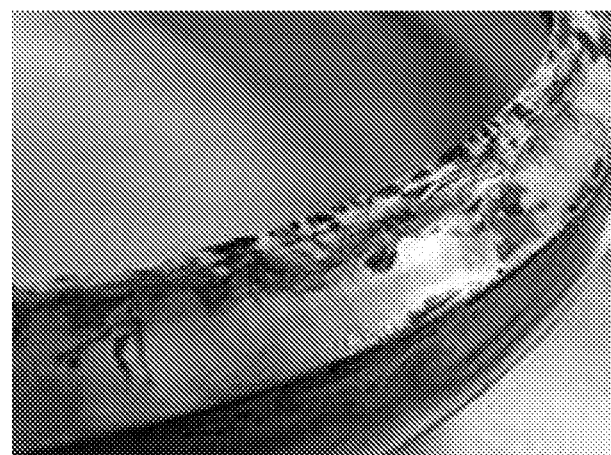


FIG. 1D-4

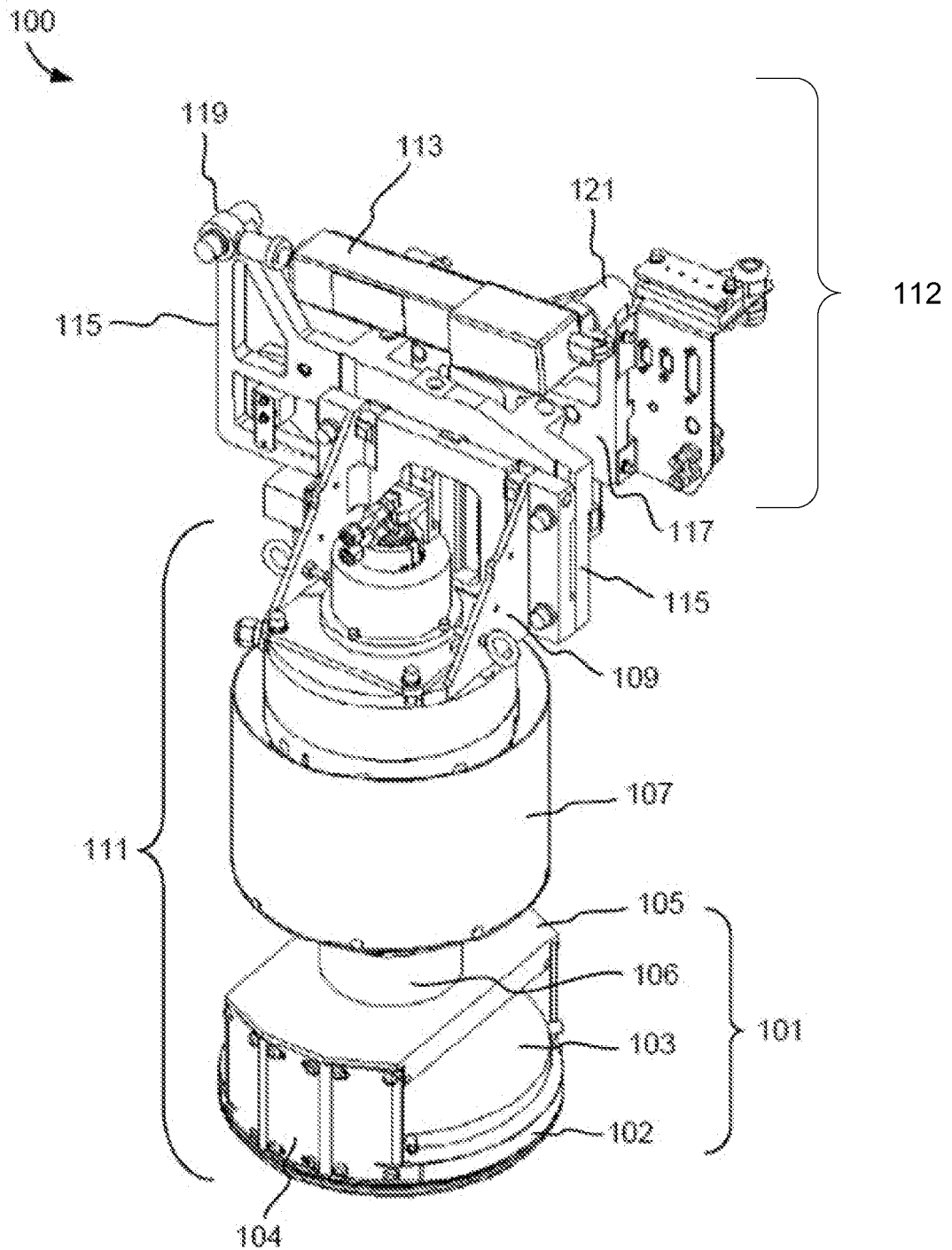


FIG. 2A

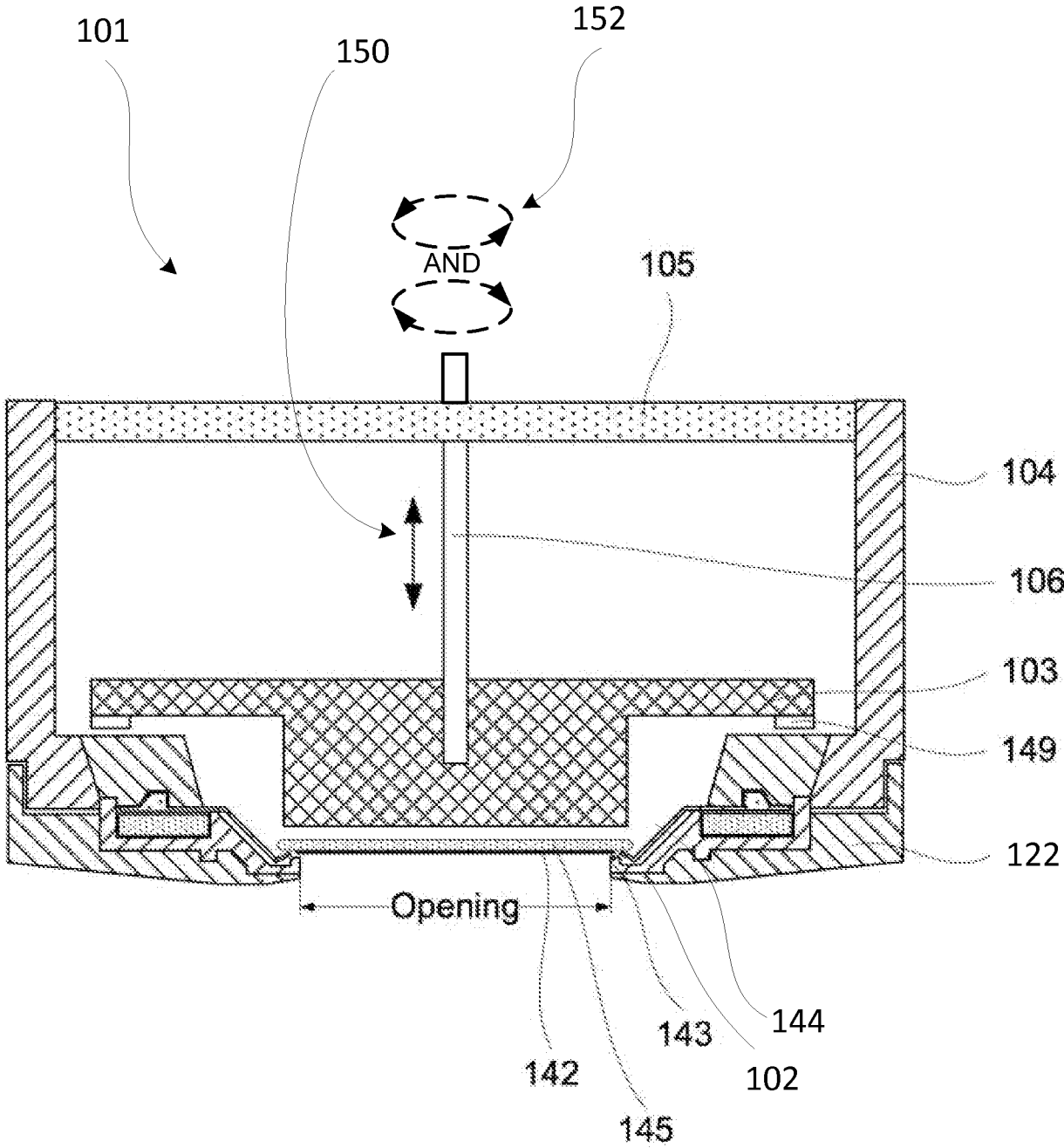


FIG. 2B

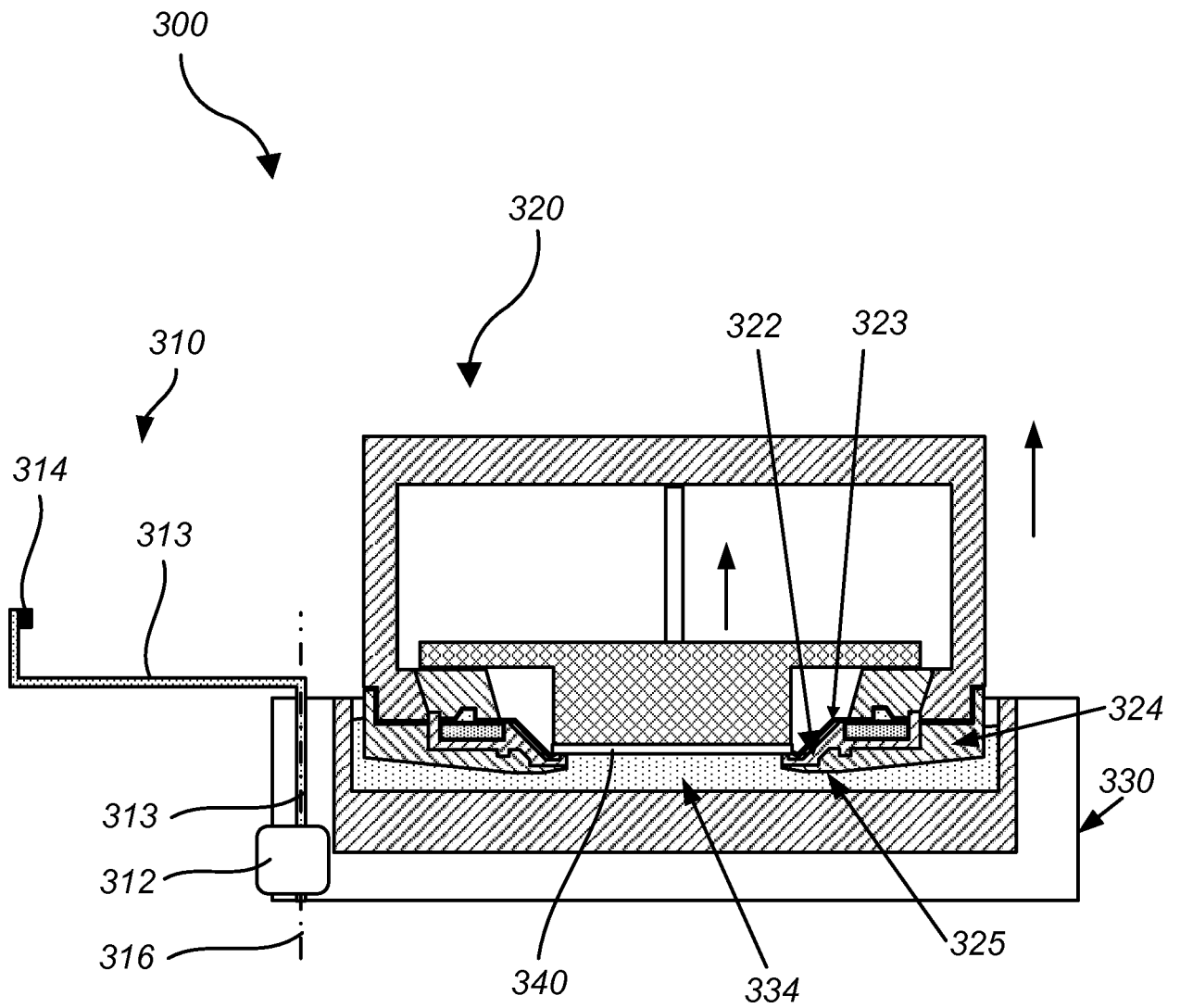
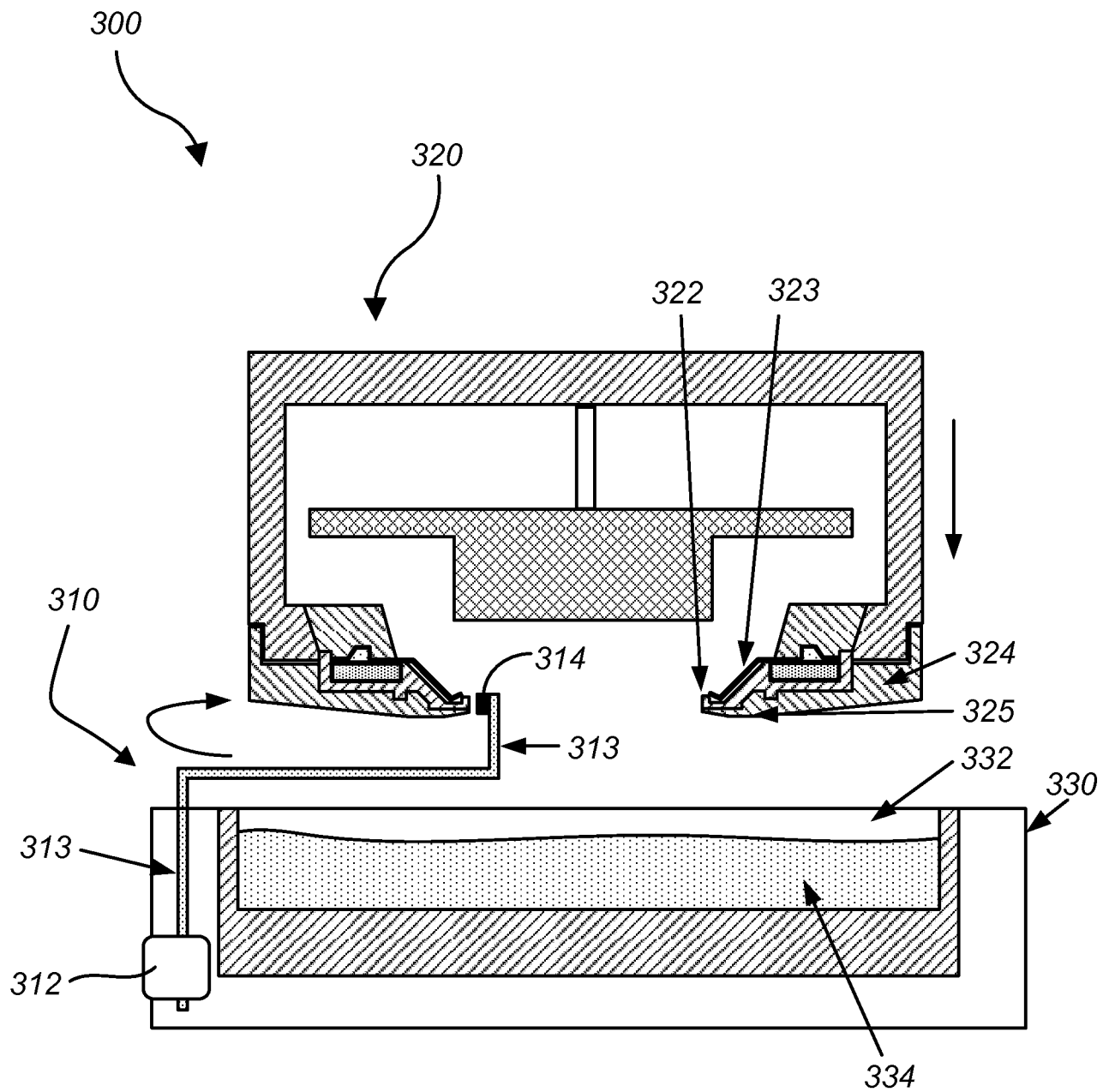


FIG. 3A

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**FIG. 3B**

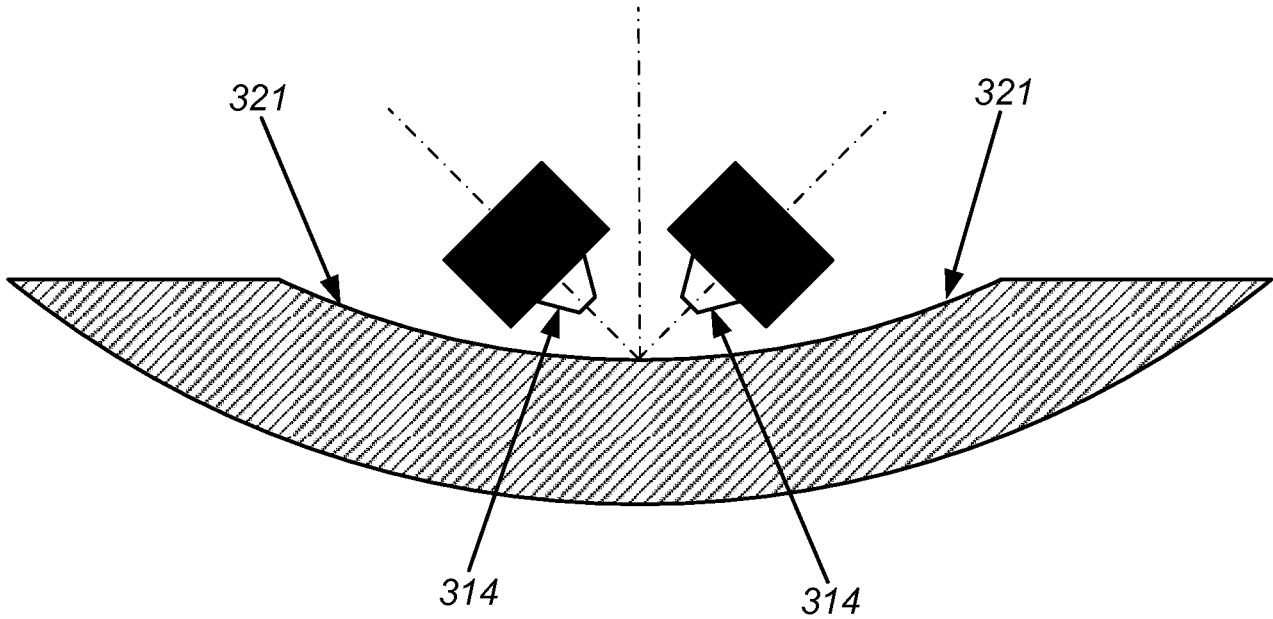


FIG. 3C

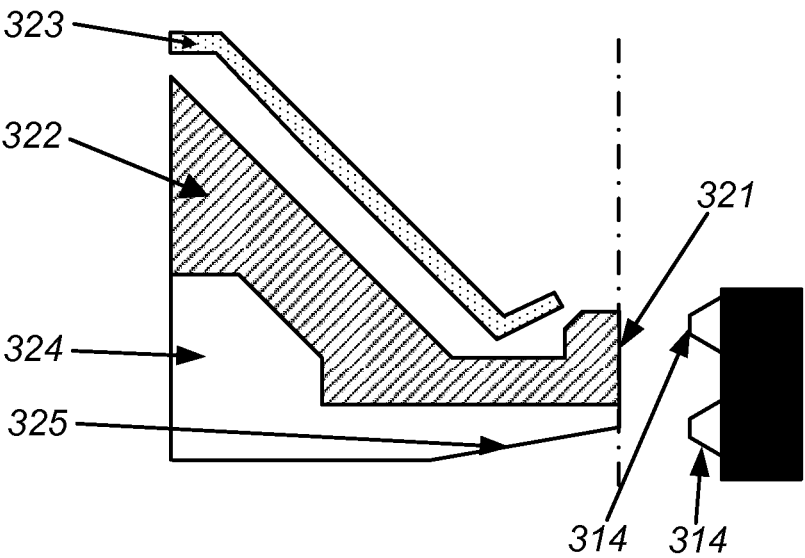


FIG. 3D

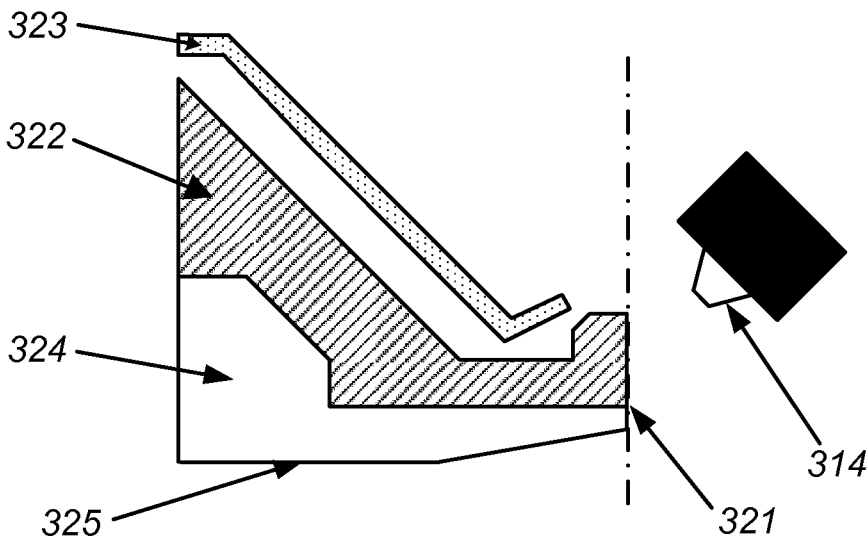


FIG. 3E

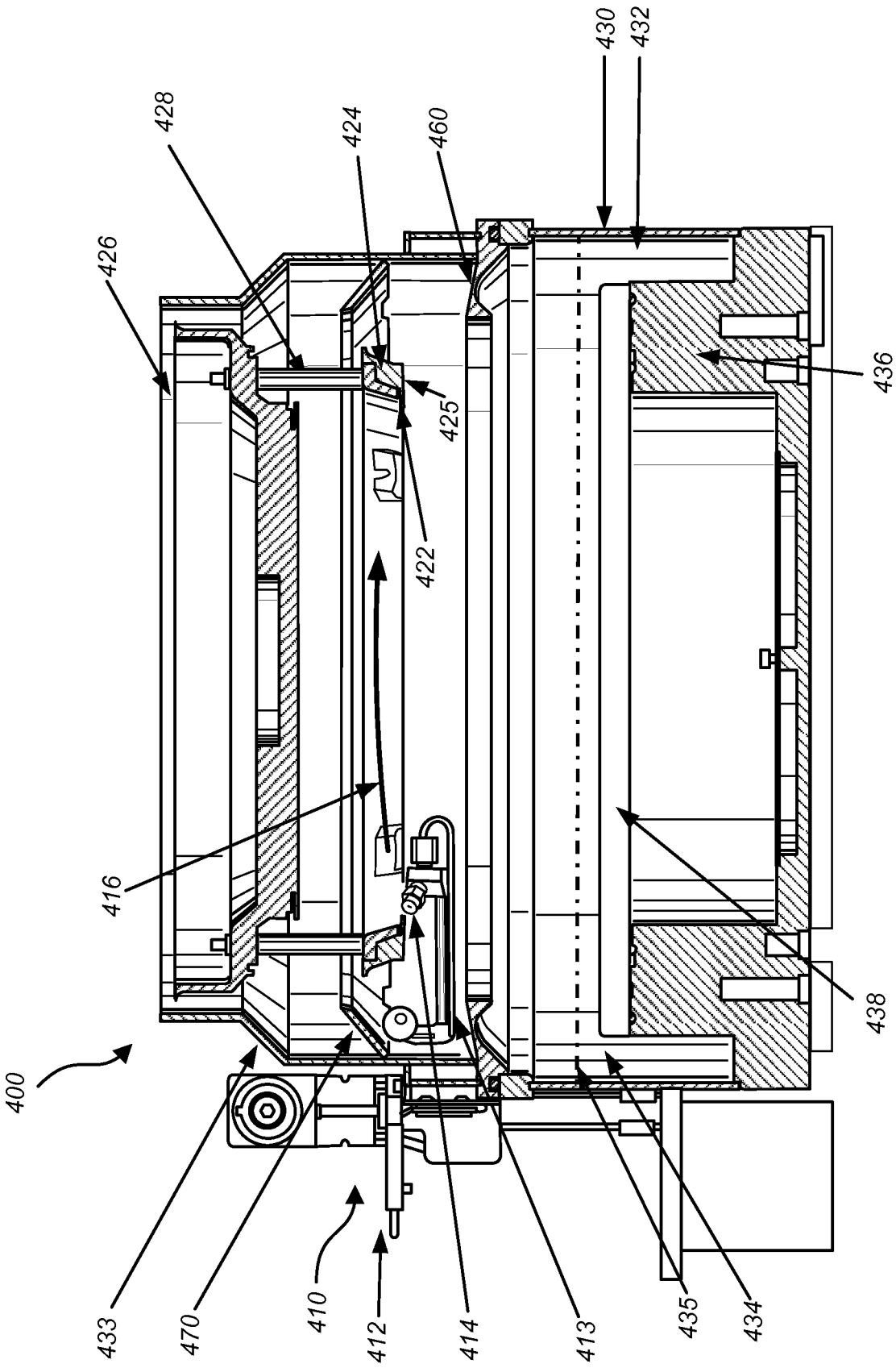


FIG. 4A

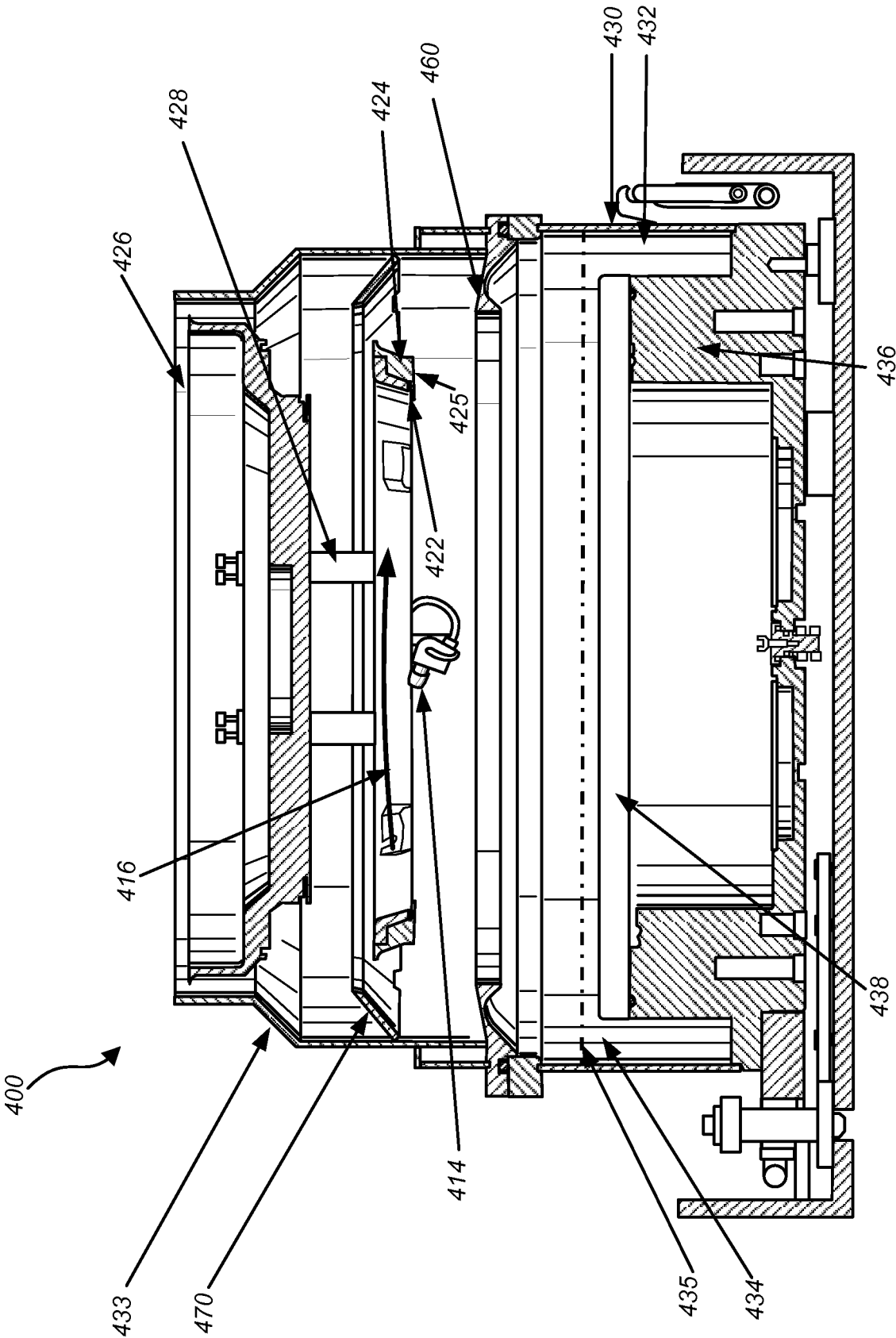
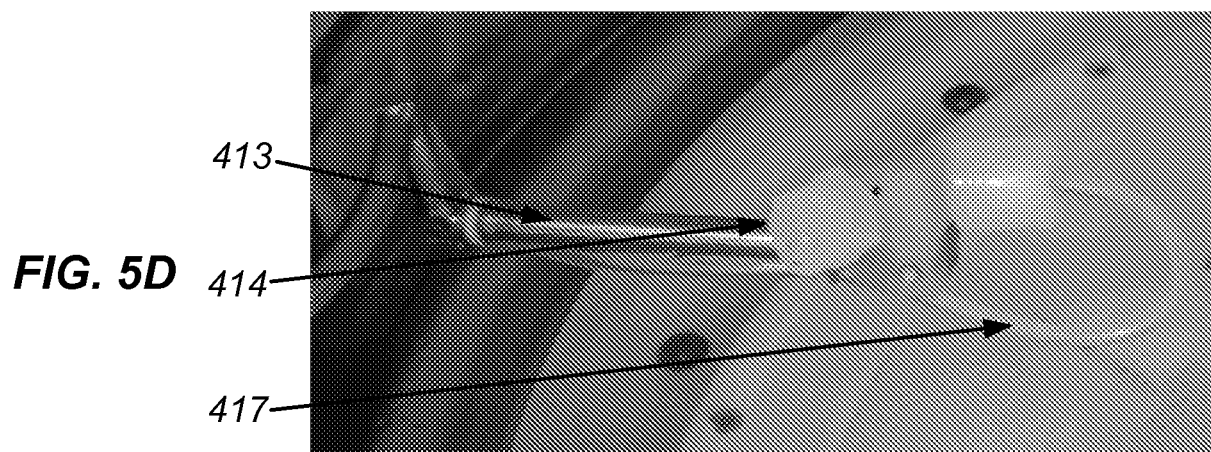
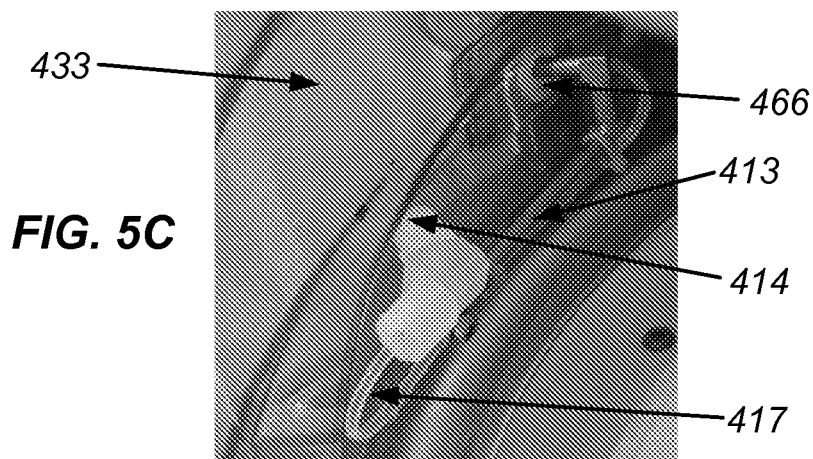
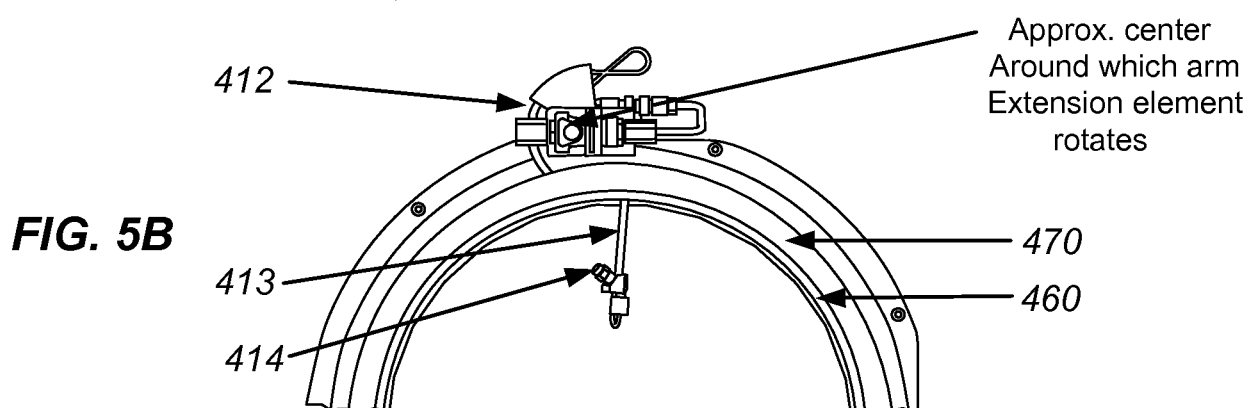
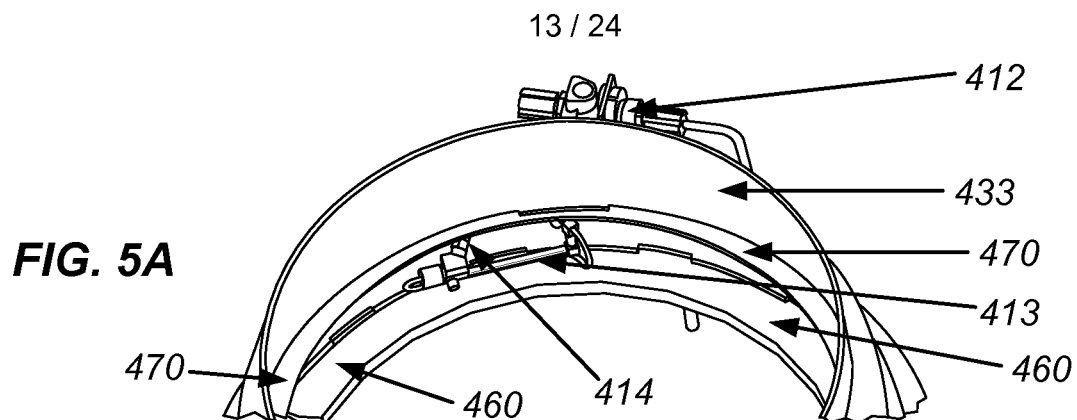


FIG. 4B



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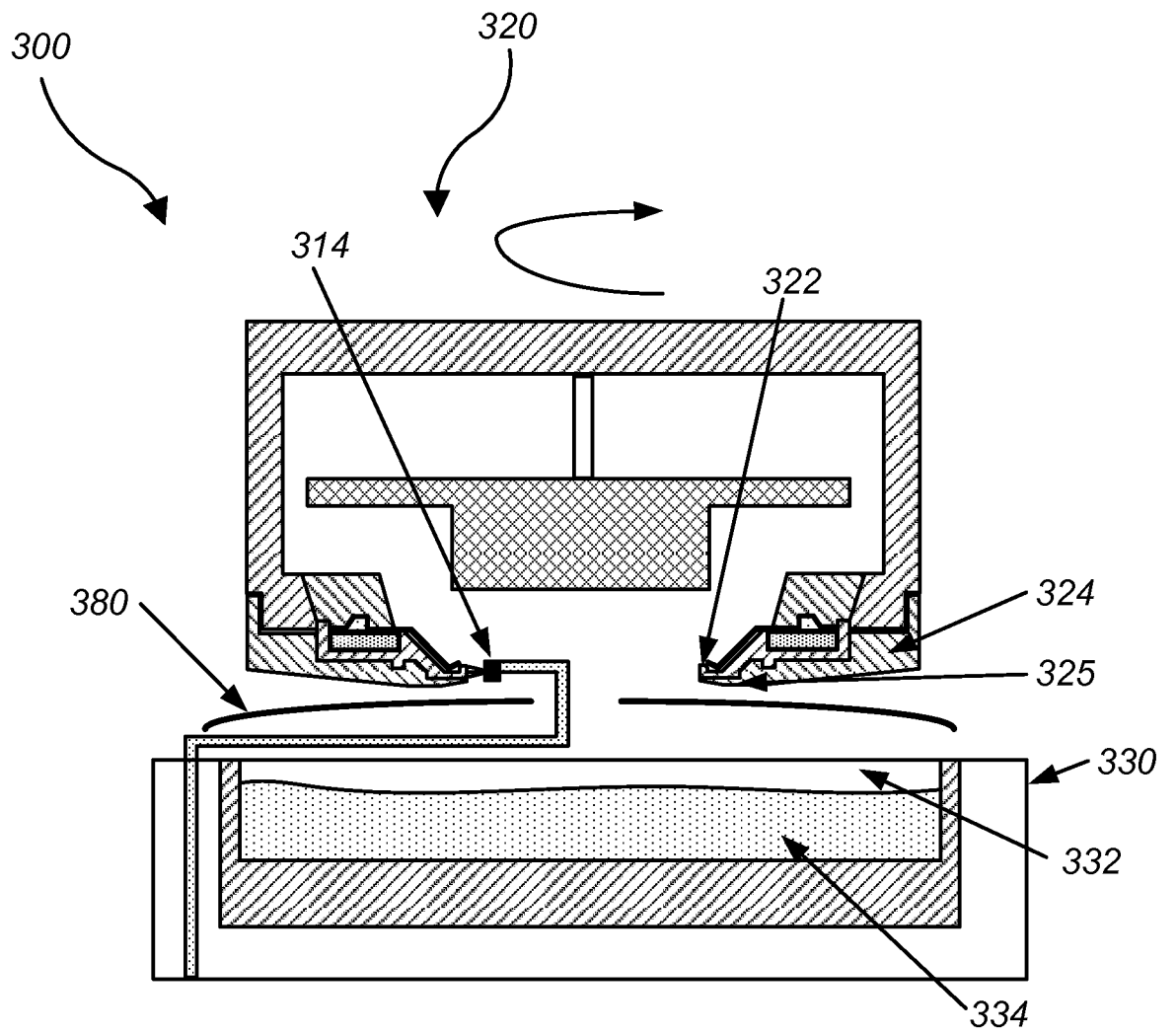


FIG. 6

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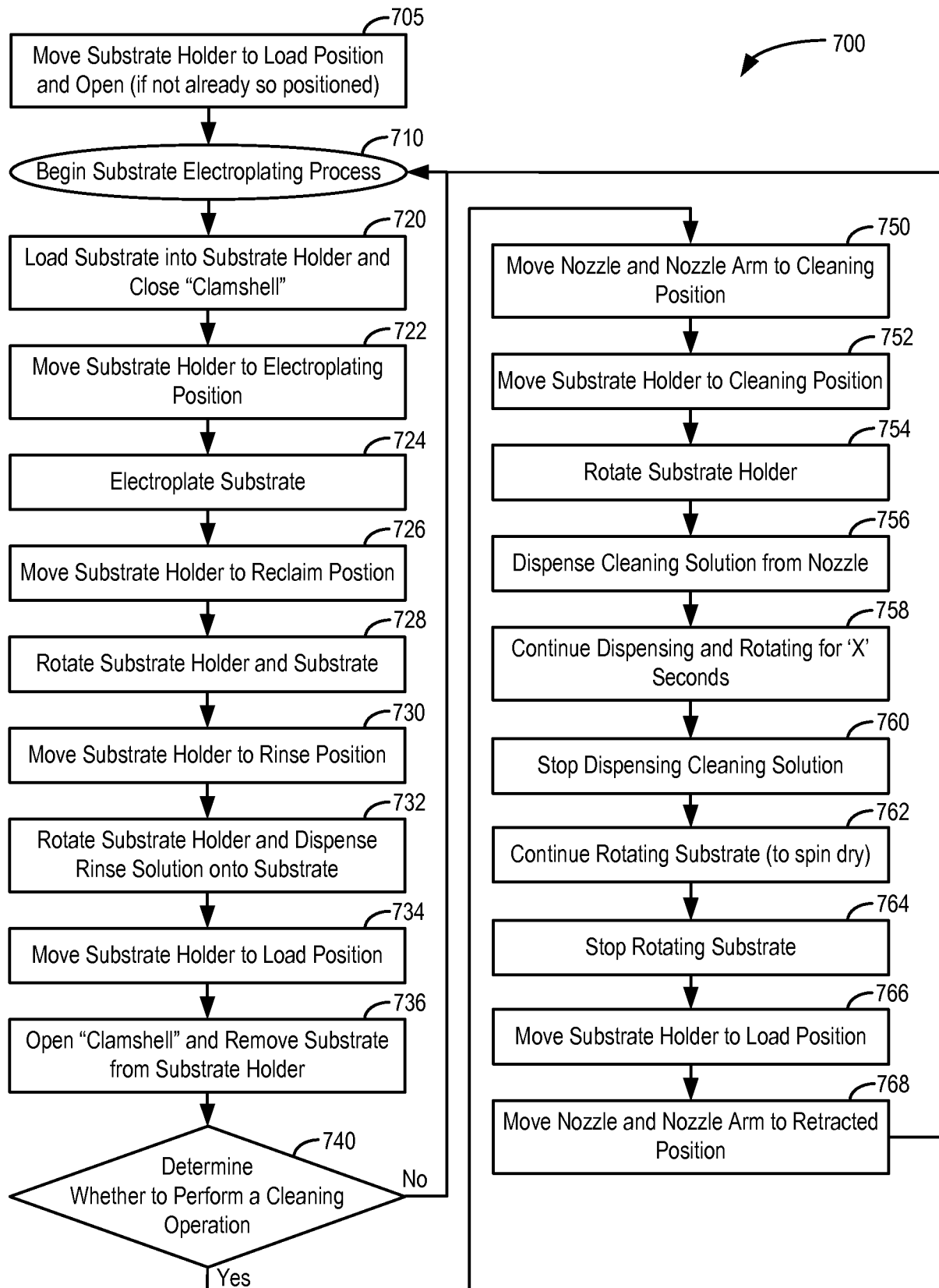


FIG. 7

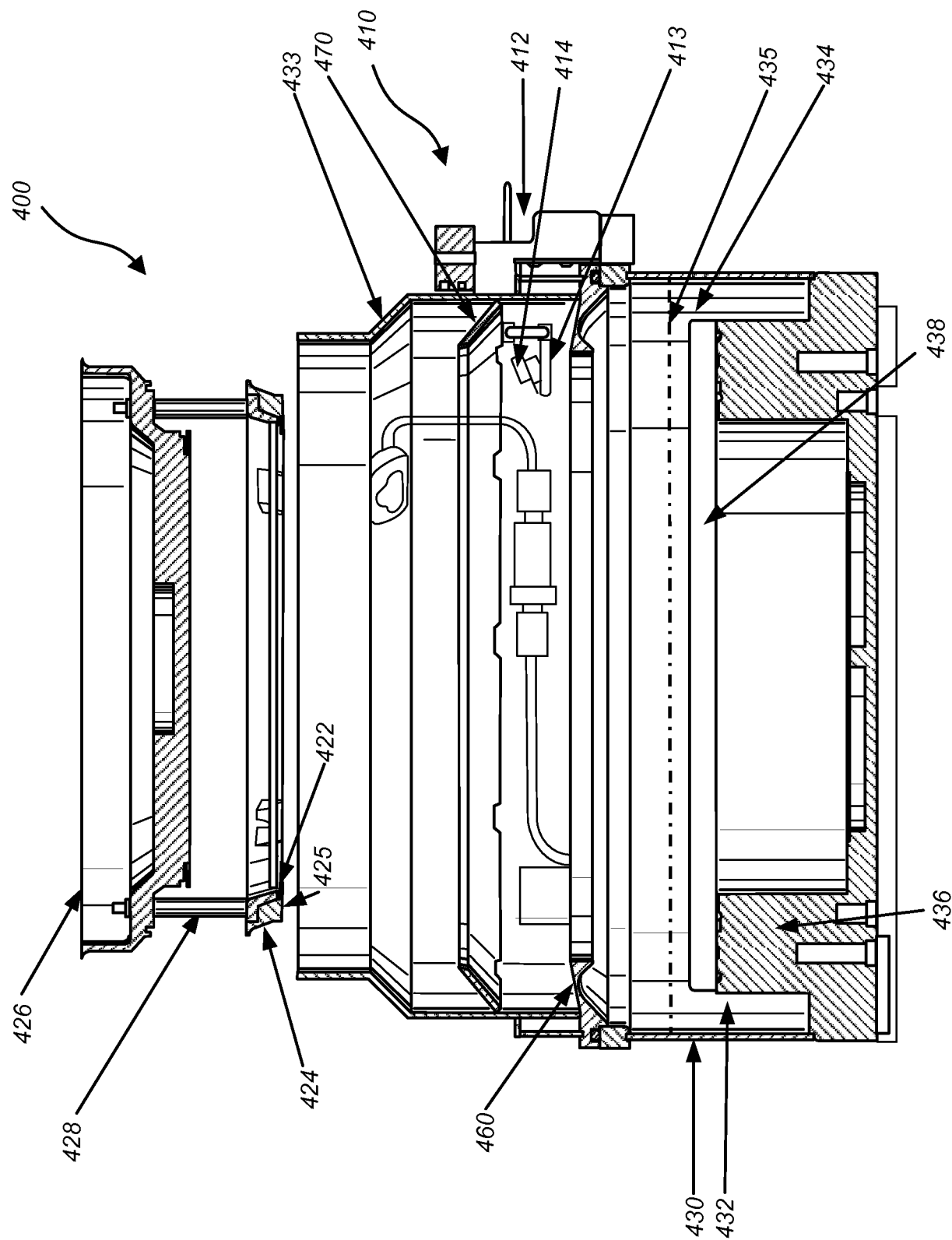


FIG. 8A

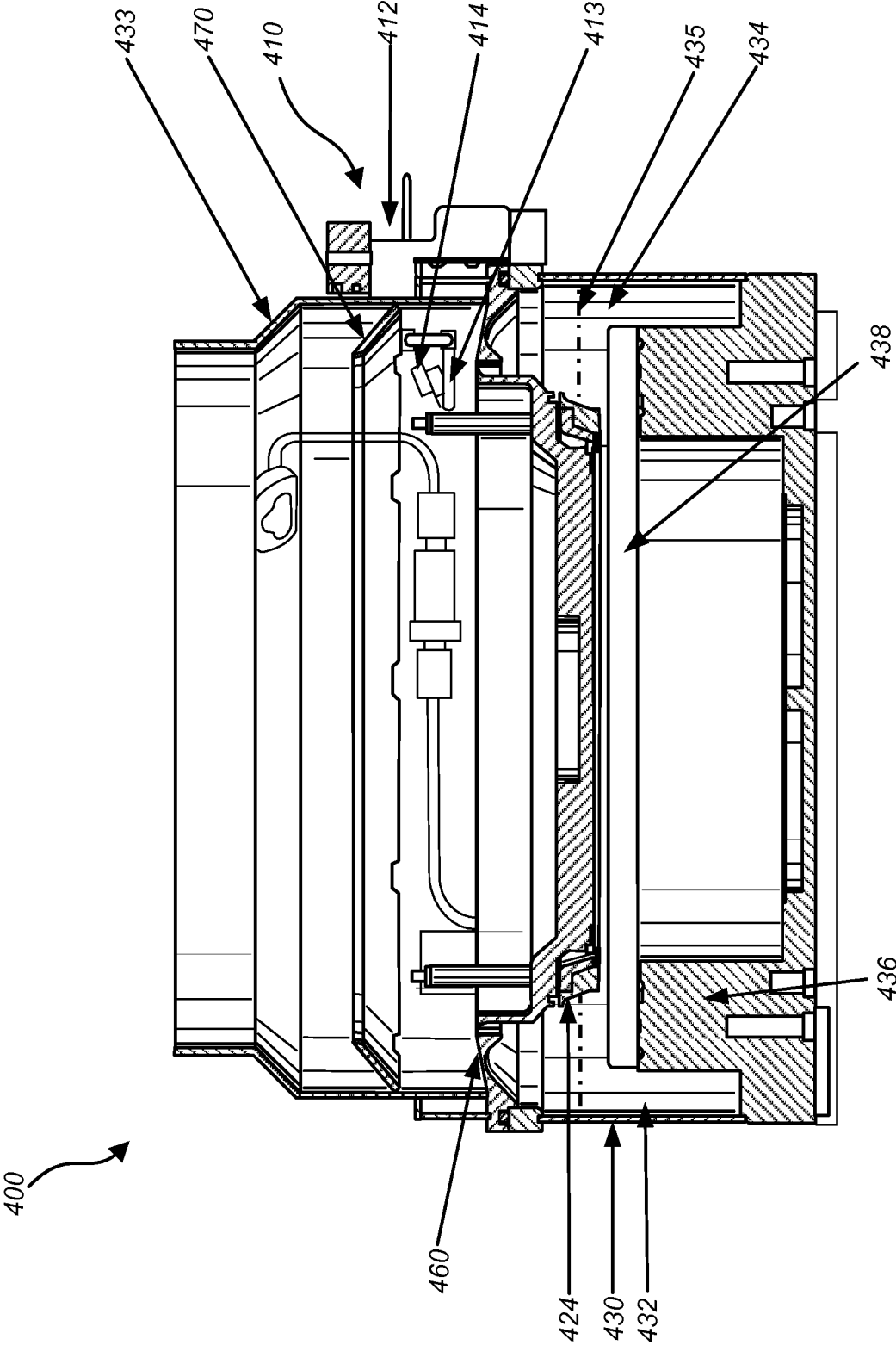


FIG. 8B

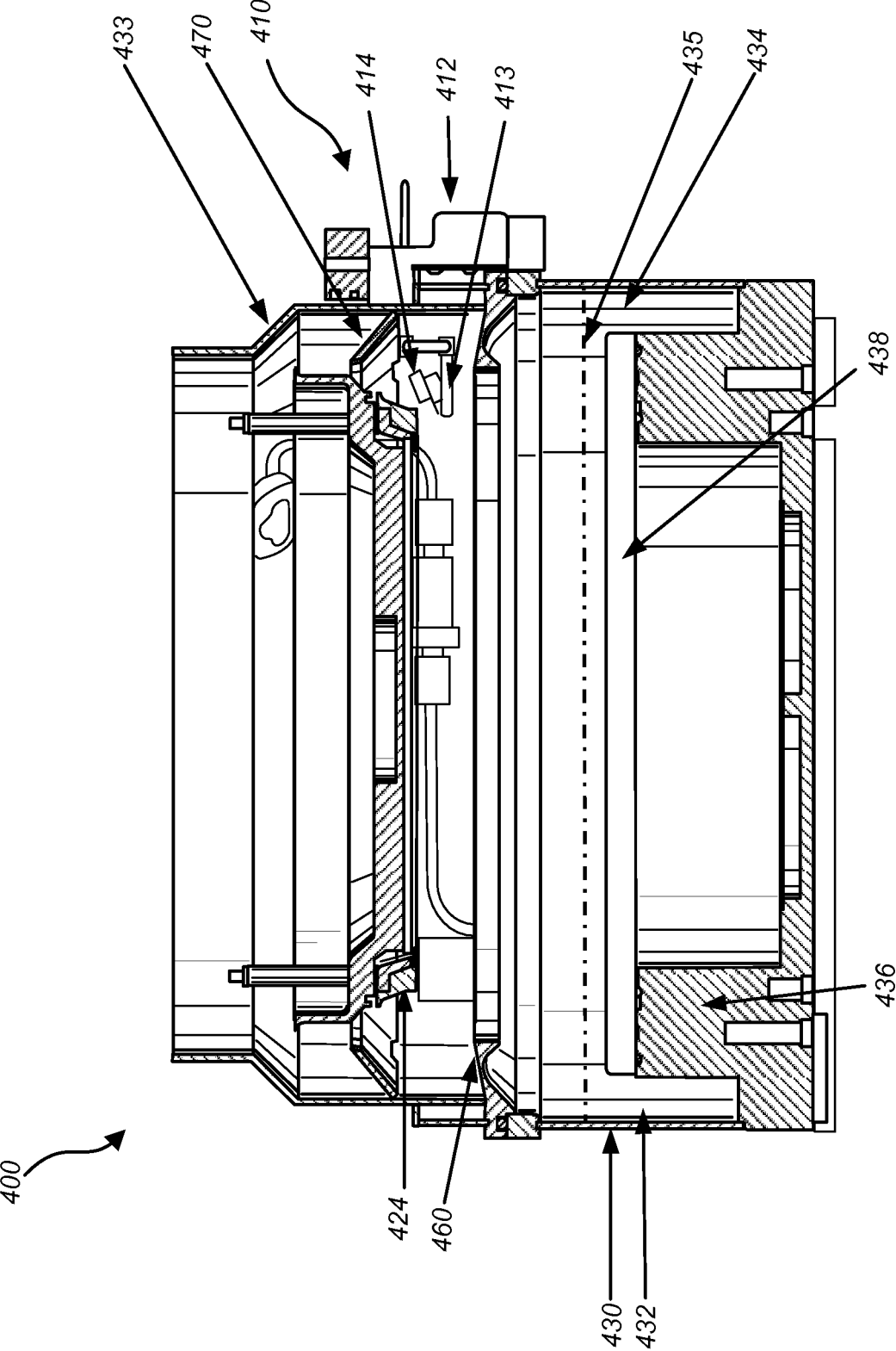


FIG. 8C

900

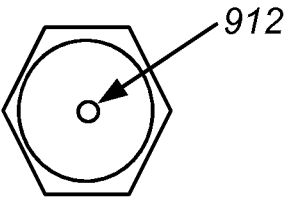


FIG. 9A

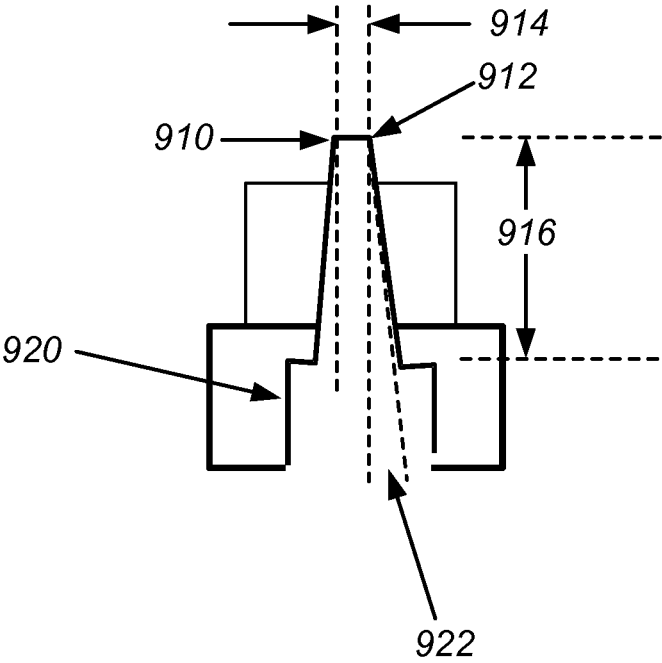
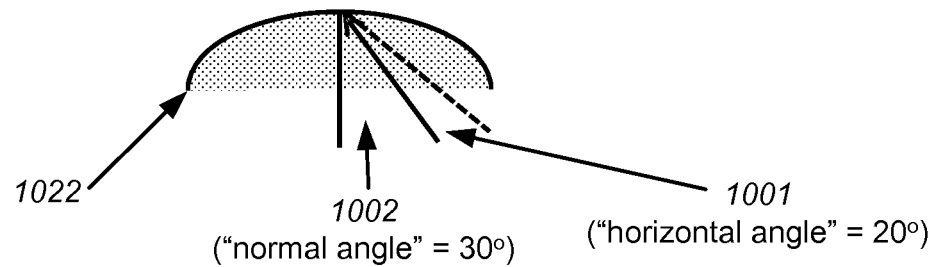
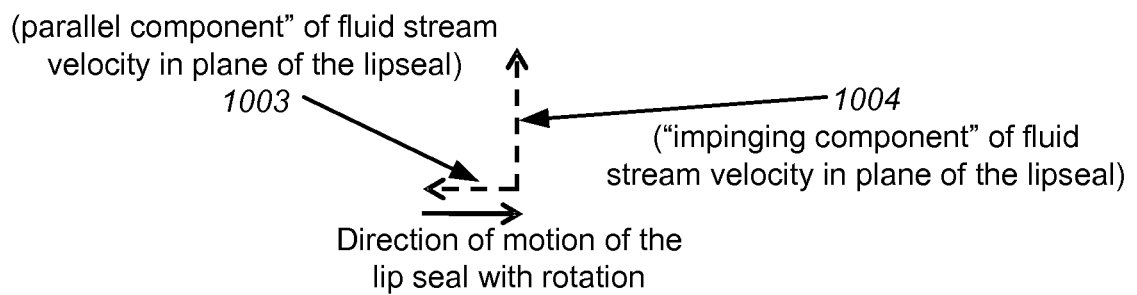
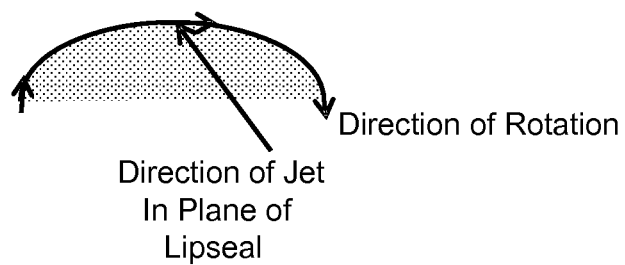


FIG. 9B

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**FIG. 10A****FIG. 10B****FIG. 10C**

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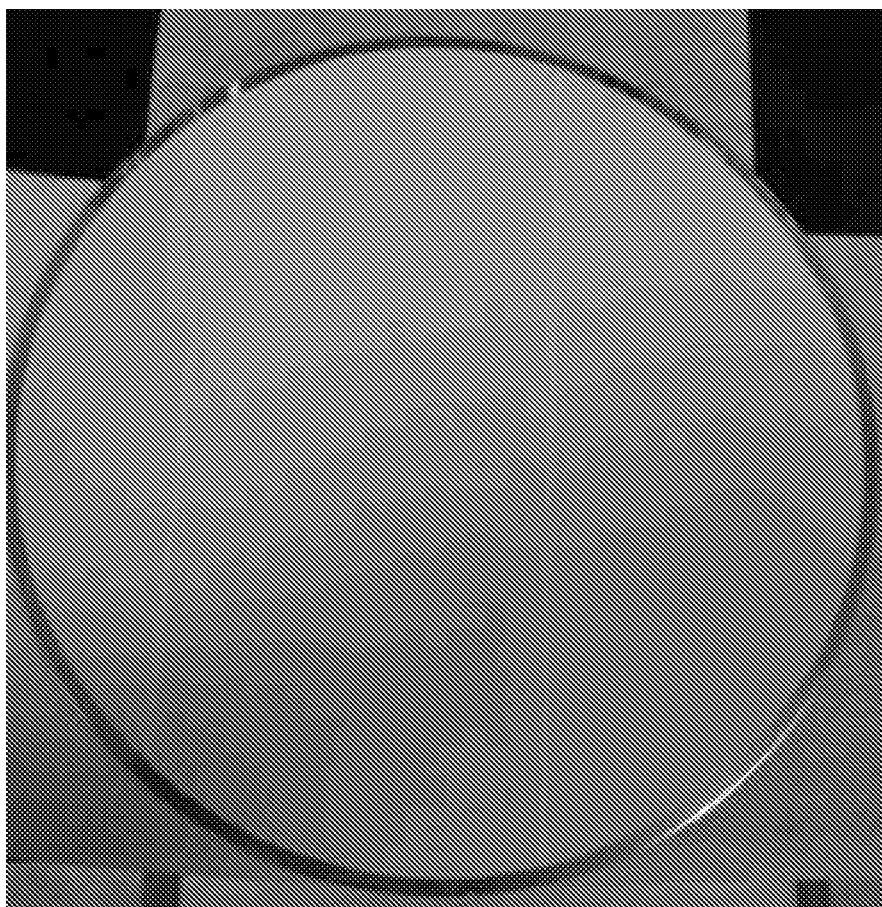


FIG. 11A

0 Wafers Plated (Pre-Marathon Test)

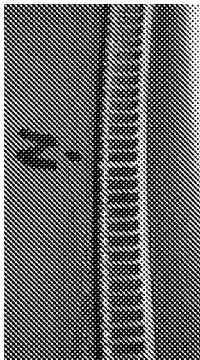


FIG. 11B-1

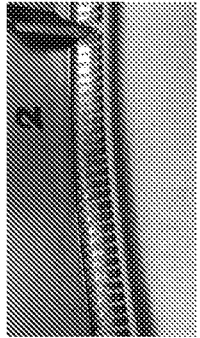


FIG. 11B-2

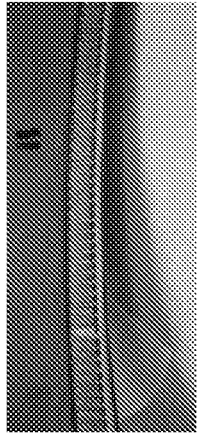


FIG. 11B-3

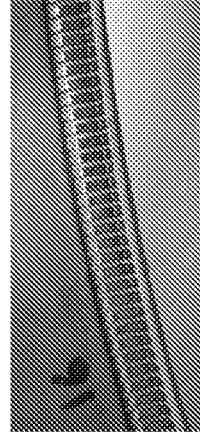


FIG. 11B-4

500 Wafers Plated; Substrate Autocleaning Enabled

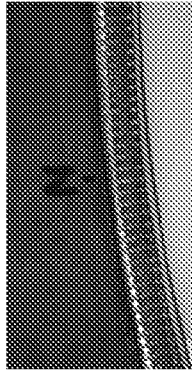


FIG. 11C-1

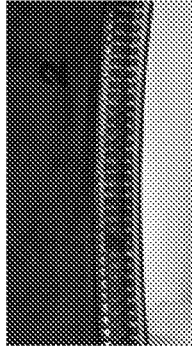


FIG. 11C-2

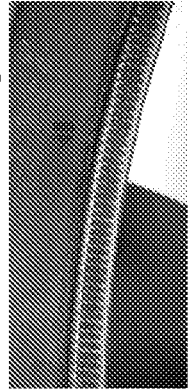


FIG. 11C-3

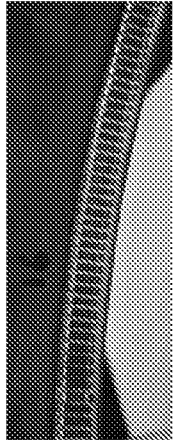


FIG. 11C-4

200 Wafers Plated; No Substrate Autocleaning

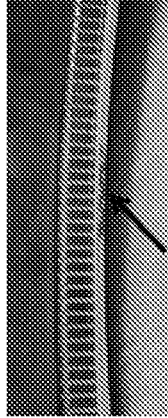


FIG. 11D-1

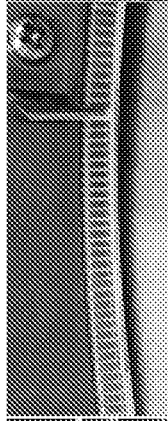


FIG. 11D-2

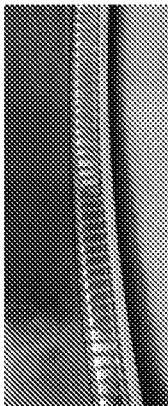


FIG. 11D-3

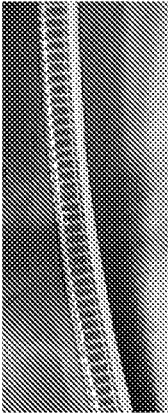


FIG. 11D-4

500 Wafers Plated; No Substrate Autocleaning

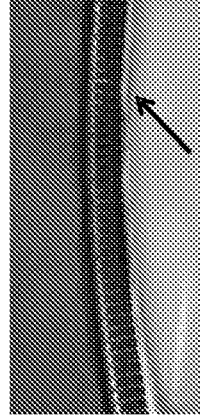


FIG. 11E-1

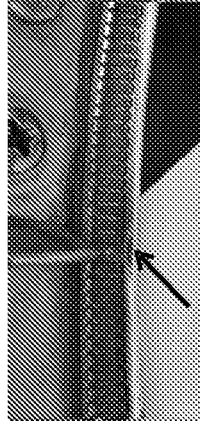


FIG. 11E-2

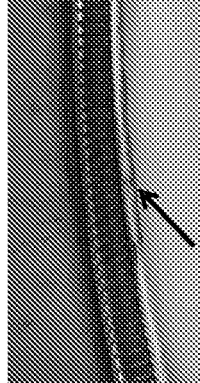


FIG. 11E-3

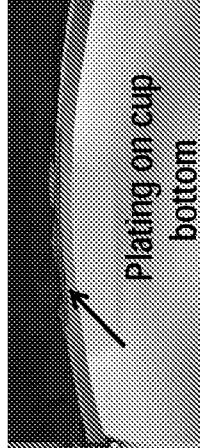
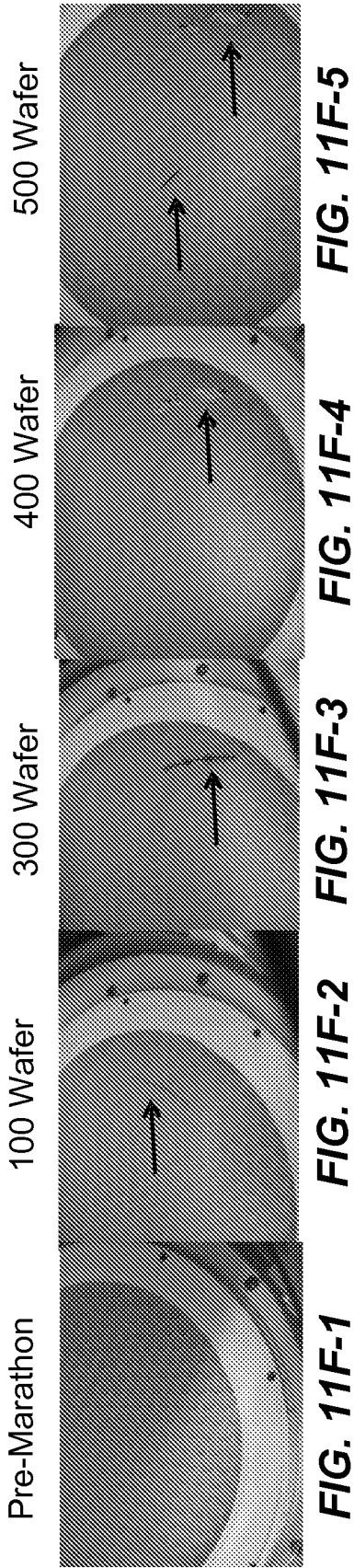


FIG. 11E-4

Plating on cup
bottom



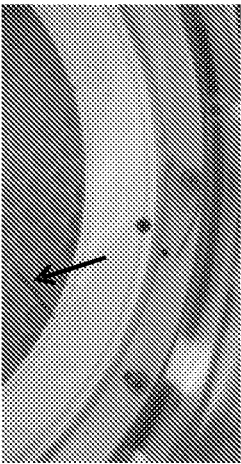


FIG. 11G-1

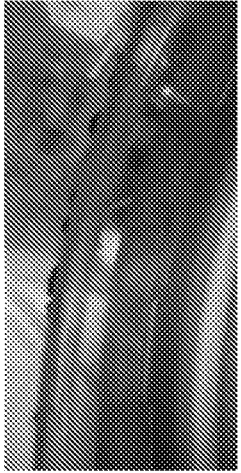


FIG. 11G-2

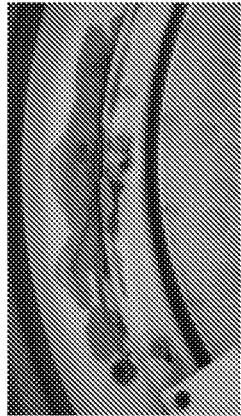


FIG. 11G-3

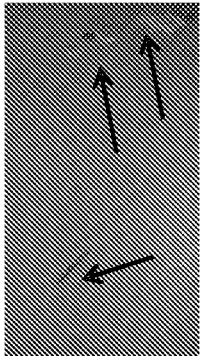


FIG. 11G-4

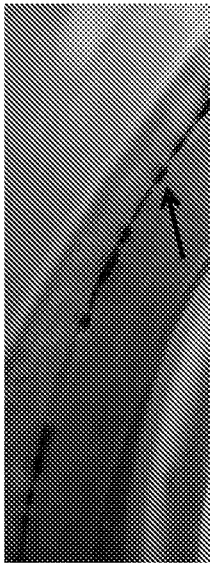


FIG. 11H-1

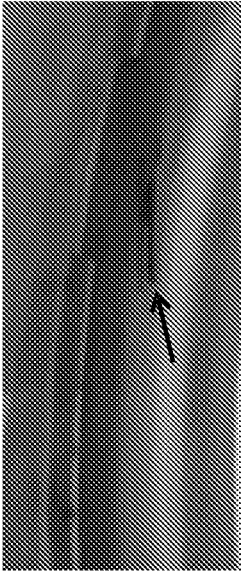


FIG. 11H-2

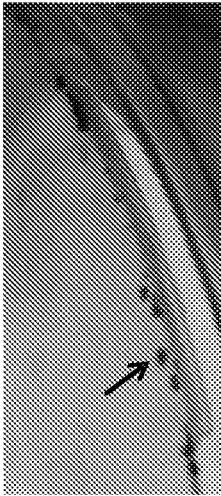


FIG. 11H-3



FIG. 11I-1

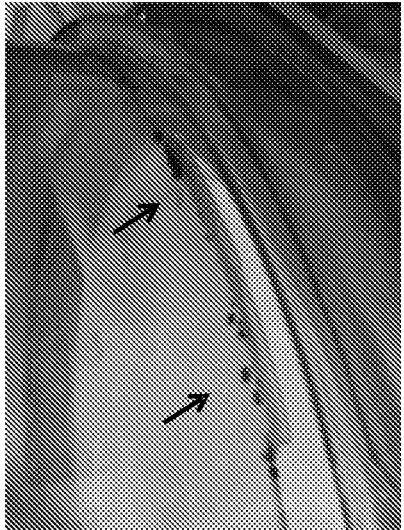


FIG. 11I-2

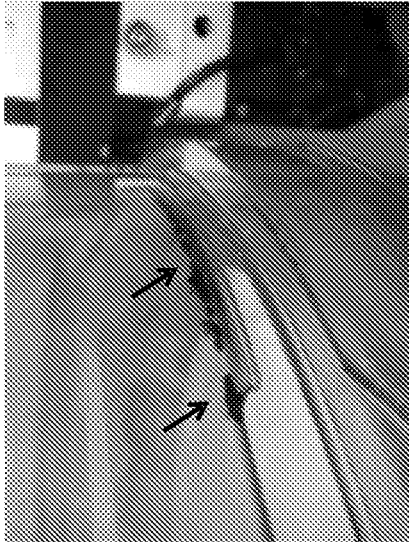


FIG. 11I-3