insulating layer (MONOS structure). The current paths of the plurality of memory cell transistors MT are connected in series between the selection transistors ST1 and ST2. The current path of the memory cell transistor MT18 on one end side of the series connection is connected to one end of the current path of the selection transistor ST1, and the current path of the memory cell transistor MT0 on the other end side is connected to one end of the current path of the selection transistor ST2.

The gates of the selection transistors ST1 in the string units SU0 to SU3 are commonly connected to selection gate lines SGD0 to SGD3, respectively. On the other hand, the gates of the selection transistors ST2 are commonly connected to the same selection gate line SGS between the plurality of string units. In addition, the control gates of the memory cell transistors MT0 to MT18 in the same block are commonly connected to word lines WL0 to WL18, respectively.

That is, the word lines WL0 to WL18 and the selection gate line SGS are commonly connected between the plurality of string units SU0 to SU3 in the same block BLK, whereas the selection gate line SGD is independently provided for each of the string units SU0 to SU3 even in the same block BLK.

In addition, of the NAND strings 111 arranged in a matrix in the memory cell array 110, the other end sides of the current paths of the selection transistors ST1 of the NAND strings 111 on the same column are commonly connected to bit lines BL (BL0 to BL(L-1), (L-1) is a natural number not less than 1). That is, the bit lines BL commonly connect the NAND strings 111 between

each of the selection gate line SGS and the word lines WL so as to surround the silicon pillar MH. The charge accumulation layer is a floating gate electrode FG formed by, for example, a conductive layer (polysilicon layer or the like). However, the charge accumulation layer may be formed by an insulating film. A gate insulating film is provided between the silicon pillar MH and the floating gate electrodes FG. In addition, a block insulating film is provided between the floating gate electrode FG and a selection gate SGS and the word lines WL.

Additionally, a trench DY extending from the word line of the uppermost layer to the source line SL is provided in the cell region. The trench DY is filled with the interlayer dielectric film 502. In the region shown in FIG. 8, each of the conductive layers functioning as the word lines WL, the selection gate line SGS, and the source line SL is divided by the trench DY into two regions. However, the regions are connected in a region not shown (a connecting portion CNCT to be described later). Additionally, a contact plug C0 connected to the interconnect M1 is provided in the trench DY.

An end of each of the selection gate line SGS and the word lines WL facing the lane R has a step shape. That is, the ends of the selection gate line SGS and the word lines WL are processed so as not to overlap the interconnects (word lines WL) on the above layer. In this region, contact plugs CC are formed on the selection gate lines SGS and SGD and the word lines WL.

In the lane R or C, the contact plug C0 connected to the interconnect M1 is formed in the interlayer dielectric film 502.

the word lines WL in the hook-up region WLHU which belong to the same block BLK. Note that the width of the connecting portion CNCT along the X direction is made smaller than the width of the cell portion CEL along the X direction. Hence, the trench DY exists between the cell portion CEL and the hook-up portion WLHU in the same block BLK as well. In other words, in a given cell unit CU, of the two ends of the cell portion CEL along the Y direction, the end facing the hook-up portion WLHU belonging to the block BLK different from that of the cell portion CEL wholly faces the trench DY. On the other hand, the end facing the hook-up portion WLHU belonging to the same block BLK as that of the cell portion CEL (in other words, the hook-up portion physically connected to the cell portion CEL by the connecting portion CNCT) only partially faces the trench DY (the remaining region is connected to the connecting portion CNCT). In other words, the structure of the block BLK viewed on the X-Y plane has a shape constricted in the connecting portion CNCT.

In each cell region, the plurality of cell units CU each having the above-described structure are physically separated by slits SLT1 provided along the Y direction. The slit SLT1 has a structure in which an insulating layer is buried in a trench extending through the selection gate lines SGS and SGD and the word lines WL, and is provided from the end of the hook-up portion WLHU of one block BLK in the cell unit CU to the end of the hook-up portion WLHU of the other block BLK through the cell portion CEL. Note that the trench DY is formed to extend from the selection gate line SGD through the source line SL. However,

Y direction between the cell regions.

In addition, a region in which the source line SL, the selection gate lines SGS and SGD, and the word lines WL are removed is provided between the cell regions adjacent in the Y direction as well, and an insulating layer is buried in the removed region. This region is the lane R. The lane R is provided along the X direction between the cell regions.

The planar structure of the cell region will be described in more detail with reference to FIGS. 10 and 11. FIG. 10 shows the planar layout of two cell units CU, and FIG. 11 shows interconnect layers formed by interconnects above cells in FIG. 10. Note that in FIG. 10, contact plugs CP12 formed in the trenches DY are not illustrated.

The cell portion CEL will be described first. As shown in FIGS. 10 and 11, in the cell portion CEL, the selection gate line SGS and the word lines WL each having a flat plate shape spreading on the X-Y plane are stacked, and the word line WL18 is provided in the uppermost layer of the stacked structure of the word lines WL. The selection gate lines SGD (SGD0 to SGD3) each having a stripe shape whose longitudinal direction is parallel to the Y direction are provided on the word line WL18. Each side surface of the selection gate lines SGD has an uneven shape on the X-Y plane and, more specifically, a wavy shape.

The silicon pillars MH described with reference to FIG. 8 are formed on each selection gate line SGD. The silicon pillars MH are formed to extend from the selection gate line SGD to the source line SL. Additionally, as shown in FIG. 10, the silicon

the word lines WL9, WL11, WL13, WL15, and WL17 are exposed. In a column (this will be referred to as a fourth column) adjacent to the first column across the second column, the upper surfaces of the word lines WL10, WL12, WL14, WL16, and WL18 are exposed.

Additionally, in each column, the interconnect layer located on the upper layer is exposed in a region closer to the connecting portion CNCT. That is, in the row closest to the connecting portion CNCT, the upper surfaces of the word lines WL7, WL8, WL17, and WL18 are exposed. In the row farthest from the connecting portion CNCT, the upper surfaces of the selection gate line SGS and the word lines WL0, WL9, and WL10 are exposed.

A contact plug CP11 is formed on each of the (5 × 4) regions. The contact plugs CP11 are connected to metal interconnect layers IC2 formed using the interconnects D1 above the cells. The metal interconnect layers IC2 are extracted from the hook-up portion WLHU to the lane R. The metal interconnect layers IC2 are then connected to the transistors 50 of the row decoder RD in the lane R (this will be described later).

<Planar Structure of Lane R>

Details of the planar structure of the lane R will be described next with reference to FIGS. 12 and 13. FIGS. 12 and 13 show the planar layout (X-Y plane) of three cell portions CEL and two lanes R located between them. The dot dashed line at the end in the Y-axis direction in FIG. 12 and the dot dashed line at the end in the Y-axis direction in FIG. 13 represent the same position.

As described with reference to FIG. 9, in the lane R, the

SL is provided on the interlayer dielectric film that covers the row decoder 120 and the sense amplifier 140, the selection gate line SGS is formed above the source line SL, and the plurality of word lines WL are stacked above the selection gate line SGS, as in the cell portion CEL. In the hook-up portion WLHU, the end of each of the selection gate line SGS and the word lines WL facing the lane R has a step shape. That is, the interconnects in the lower layer is long along the Y direction and has a region that does not overlap the interconnects in the upper layer.

FIGS. 16, 17, 18, 19, and 20 show this state. FIGS. 16, 17, 18, 19, and 20 are sectional views taken along a line 16 - 16, a line 17 - 17, a line 18 - 18, a line 19 - 19, and a line 20 - 20 in FIG. 11. As shown in FIGS. 16, 17, 18, 19, and 20, the regions where the interconnects in the lower layer and the interconnects in the upper layer do not overlap correspond to the (5 × 4) regions described with reference to FIG. 10 where the contact plugs CP11 are formed. Note that although not illustrated in FIGS. 16, 17, 18, 19, and 20, an insulating layer is buried around the contact plugs CP11, and the contact plugs CP11 are electrically insulated from each other.

The trench DY will be described next. As shown in FIG. 13, the trench DY physically separates the source line SL, the selection gate line SGS, and the word lines WL between the cell portion CEL and the hook-up portion WLHU. As described above, an insulating layer is buried in the trench DY. The contact plugs CP12 are formed in the insulating layer. The contact plugs CP12

above-described forms, and various modifications can be made. For example, in the above embodiments, a case in which the number of stacked word lines WL is 19 has been described as an example. However, the number is not limited to this, and is 2^n (n is a natural number) in general. Additionally, in the above embodiments, a case in which the memory holes MH are arranged in a staggered pattern, as shown in FIG. 10 or the like, has been described as an example. However, the silicon pillars MH may be arranged in a line in the Y-axis direction.

In FIGS. 12 and 13 described in the first embodiment, a case in which the contact plugs CP21 in the lane R are arranged on a straight line along the X-axis direction has been described as an example. However, as shown in FIG. 27, the contact plugs CP21 may be provided so as to be arranged on the X-Y plane in an oblique direction with respect to the X-axis direction and the Y-axis direction. In this case, as shown in FIG. 28, the directions in which the contact plugs CP21 corresponding to the plurality of blocks BLK adjacent to each other in the X direction are arranged may be opposite to each other. In other words, the contact plugs CP21 may be arranged such that the line that connects them may be bent at the boundaries of the blocks BLK.

In addition, the arrangement shown in FIG. 25 described in the third embodiment may be an arrangement shown in, for example, FIGS. 29, 30, and 31. That is, the stacked structure 700 faces the trenches DY at two surfaces facing in the X direction. At this time, the stacked structure 700 may face, at one surface, the trench DY between the hook-up portion WLHU

an eighth width larger than the seventh width along the second direction, and being adjacent to the seventh region in the first direction; and

a ninth region spreading along the first plane, having a ninth width smaller than the seventh width along the second direction, and located between the seventh region and the eighth region to connect the seventh region and the eighth region,

the seventh region, the eighth region, and the ninth region include a plurality of third word lines stacked along the third direction, and the seventh region further includes a third selection gate line provided above a third word line of an uppermost layer,

the memory cell array further includes:

a fourth insulating layer buried in a fourth trench between the seventh region and the eighth region and being in contact with the ninth region in the second direction;

a third contact plug provided in the fourth insulating layer and electrically connected to the row decoder; and

a third interconnect configured to connect the third selection gate line and the third contact plug,

the second region and the eighth region are adjacent to each other in the second direction across a fifth insulating layer buried in a fifth trench between the second region and the eighth region, and

the first trench and the fourth trench are located on the same line along the second direction.

4. The semiconductor memory device according to claim 3, further comprising:

a plurality of stripe-shaped bit lines along the second direction, which are provided above the first region, the fourth region, and the seventh region in the third direction; and

a fourth contact plug provided in the fifth insulating layer buried in the fifth trench and connected to a bit line,

wherein the bit line is electrically connected to a sense amplifier via the fourth contact plug.

5. The semiconductor memory device according to claim 2, wherein the memory cell array further includes a third block,

the third block includes:

a seventh region spreading along the first plane and having a seventh width along the second direction;

an eighth region spreading along the first plane, having an eighth width larger than the seventh width along the second direction, and being adjacent to the seventh region in the first direction; and

a ninth region spreading along the first plane, having a ninth width smaller than the seventh width along the second direction, and located between the seventh region and the eighth region to connect the seventh region and the

eighth region,

the seventh region, the eighth region, and the ninth region include a plurality of third word lines stacked along the third direction, and the seventh region further includes a third selection gate line provided above a third word line of an uppermost layer,

the memory cell array further includes:

a fourth insulating layer buried in a fourth trench between the seventh region and the eighth region and being in contact with the ninth region in the second direction;

a third contact plug provided in the fourth insulating layer and electrically connected to the row decoder; and

a third interconnect configured to connect the third selection gate line and the third contact plug, and

the second region and the eighth region are adjacent to each other in the first direction across a fifth insulating layer buried in a fifth trench between the second region and the eighth region.

6. The semiconductor memory device according to claim 5, wherein the memory cell array further includes:

a fourth contact plug provided in the fifth insulating layer; and

a fifth interconnect connected to the fourth contact plug and having a longitudinal direction along the first direction,

the first block further includes a fifth contact plug

provided on the first word line in the second region,

the third block further includes a sixth contact plug provided on the third word line in the eighth region,

the fifth interconnect is extracted to the second region and the eighth region and connected to the fifth contact plug and the sixth contact plug, and

the first word line and the third word line are electrically connected to the row decoder via the fifth interconnect and the fourth contact plug.

7. The semiconductor memory device according to claim 6, wherein the second region includes a plurality of step surfaces along the first direction, and has a shape that decreases a height as a distance to the fifth insulating layer from the step surfaces becomes small,

one of the first word lines is exposed to one of the step surfaces,

the eighth region includes a plurality of step surfaces along the first direction, and has a shape that decreases a height as a distance to the fifth insulating layer from the step surfaces becomes small, and

one of the third word lines is exposed to one of the step surfaces.

8. The semiconductor memory device according to claim 1, further comprising a second interconnect provided in a region between the semiconductor substrate and the

memory cell array,

wherein, one of the first word lines which is in a lowermost layer is provided above a source line,

the first trench is formed from an upper surface of the first word line of the uppermost layer to at least a depth reaching a bottom surface of the source line, and

the first contact plug is formed from the first interconnect to a depth reaching the second interconnect.

9. The semiconductor memory device according to claim 2, wherein, one of the first word lines which is in a lowermost layer is provided above a first source line,

one of the second word lines which is in a lowermost layer is provided above a second source line, and

the first source line and the second source line are commonly connected to a region immediately under the third trench.

10. The semiconductor memory device according to claim 3, wherein, one of the first word lines which is in a lowermost layer is provided above a first source line,

one of the third word lines which is in a lowermost layer is provided above a third source line, and

the first source line and the third source line are commonly connected in a region immediately under the fifth trench.

11. The semiconductor memory device according to claim 4, further comprising a fourth interconnect provided in a region between the semiconductor substrate and the memory cell array,

wherein, one of the first word lines which is in a lowermost layer is provided above a first source line,

one of the third word lines which is in a lowermost layer is provided above a third source line,

the fifth trench is formed from upper surfaces of the first word line and the third word line of the uppermost layer to at least a depth reaching bottom surfaces of the first source line and the third source line, and

the fourth contact plug is formed from the bit line to a depth reaching the fourth interconnect.

12. The semiconductor memory device according to claim 6, further comprising a sixth interconnect provided in a region between the semiconductor substrate and the memory cell array,

wherein, one of the first word lines which is in a lowermost layer is provided above a first source line,

one of the third word lines which is in a lowermost layer is provided above a third source line,

the fifth trench is formed from upper surfaces of the first word line and the third word line of the uppermost layer to at least a depth reaching bottom surfaces of the first source line and the third source line, and

the fourth contact plug is formed from the fifth interconnect to a depth reaching the sixth interconnect.

13. A semiconductor memory device comprising:

a row decoder provided on a semiconductor substrate including a first surface; and

a memory cell array provided above the row decoder and including a set of cell regions arranged in a matrix, the memory cell array including an interconnect connected to the row decoder and overlapping the row decoder on a plane along the first surface;

wherein the row decoder includes a first transistor provided outside an outer periphery of the set of the cell regions on the plane along the first surface.

14. The semiconductor memory device according to claim 13, wherein the row decoder further includes a second transistor overlapping the memory cell array on the plane along the first surface, and

the semiconductor memory device further comprises a sense amplifier provided on the semiconductor substrate and overlapping the memory cell array on the plane along the first surface.

15. The semiconductor memory device according to claim 13, further comprising a first connecting portion provided between the first transistor and one cell region

of the set of the cell regions and including a first contact plug configured to connect the interconnect and the row decoder.

16. The semiconductor memory device according to claim 15, wherein the set of the cell regions includes a first cell region and a second cell region which are adjacent to each other,

the first transistor is located outside an outer periphery of the first cell region on the plane along the first surface, and

the semiconductor memory device further comprises a dummy region provided outside an outer periphery of the second cell region on the plane along the first surface and including an active region and a conductor.

17. The semiconductor memory device according to claim 16, wherein the first connecting portion is provided between the first cell region and the first transistor,

the interconnect of the first cell region is electrically connected to the first transistor via the first connecting portion, and

the semiconductor memory device further comprises a second connecting portion provided between the second cell region and the dummy region and including a second contact plug configured to connect the interconnect of the second cell region to the row decoder located immediately under

the second cell region.

18. A semiconductor memory device comprising:

a memory cell array including a source line provided above a first surface of a semiconductor substrate, and a word line provided above the source line;

a wall surrounding the memory cell array in a plane along the first surface, including a plurality of conductive layers arranged in a direction crossing the first surface of the semiconductor substrate from a layer of the source line to a layer of the word line, and including a recess at an inner surface extending from an upper surface to a lower surface; and

an insulating layer provided from a position of the upper surface of the wall to a position of the lower surface and being in contact with the inner surface of the wall in the recess.

19. The semiconductor memory device according to claim 18, wherein the memory cell array comprises:

a selection gate line provided above the word line;

a first region and a second region which are adjacent to each other along a first direction and include the word line and the selection gate line; and

a third region in which the selection gate line in the first region is connected to an interconnect, and

the recess is provided in a region of the inner

surface of the wall, facing the third region.

20. The semiconductor memory device according to claim 19, wherein the memory cell array includes a plurality of interconnects stacked in a direction crossing the first surface of the semiconductor substrate between the source line and the selection gate line, and

the plurality of conductive layers of the wall are located at the same layers as the plurality of interconnects, respectively.